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28-29 SEPTEMBER 2021

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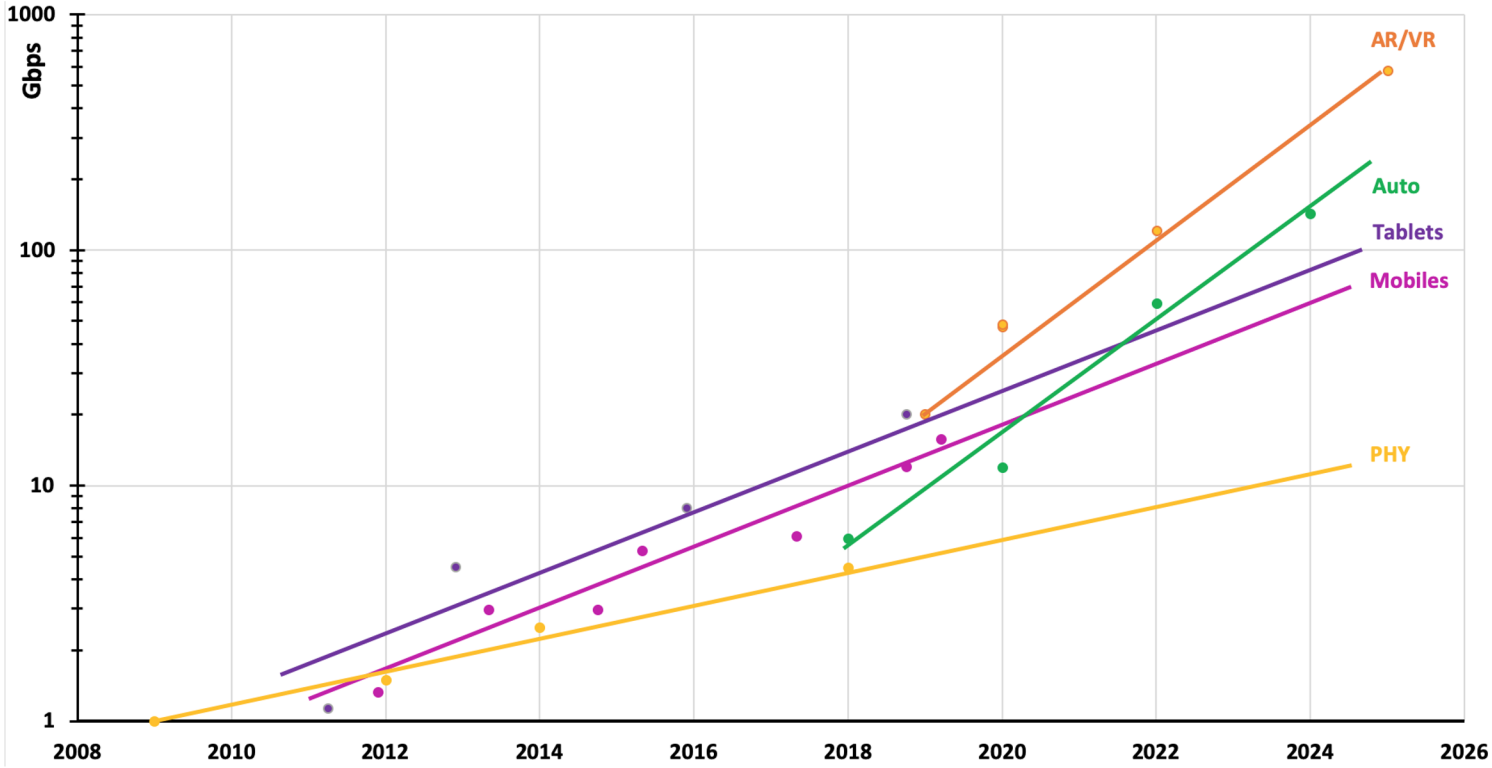
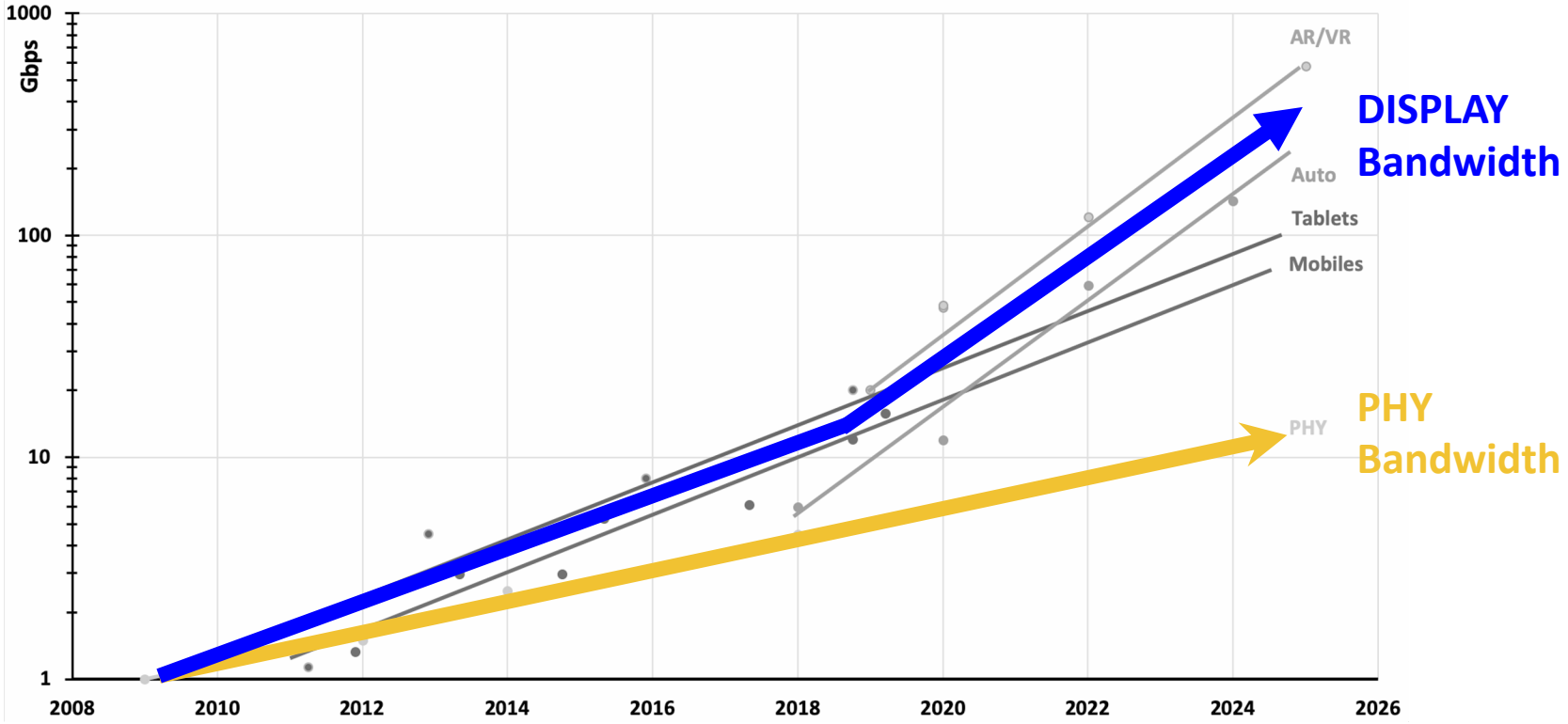
Meeting the Needs of Next-Generation Displays with a High-Performance MIPI DSI-2℠ Subsystem Solution

Bandwidth Challenge for Video Connectivity



Bandwidth Challenge for Video Connectivity



Some Applications Require Even More Bandwidth

Mobile Displays

- Need to support gaming
- Need to be “AR/VR ready”
- Foldable displays
- Require higher display resolutions and frame rates

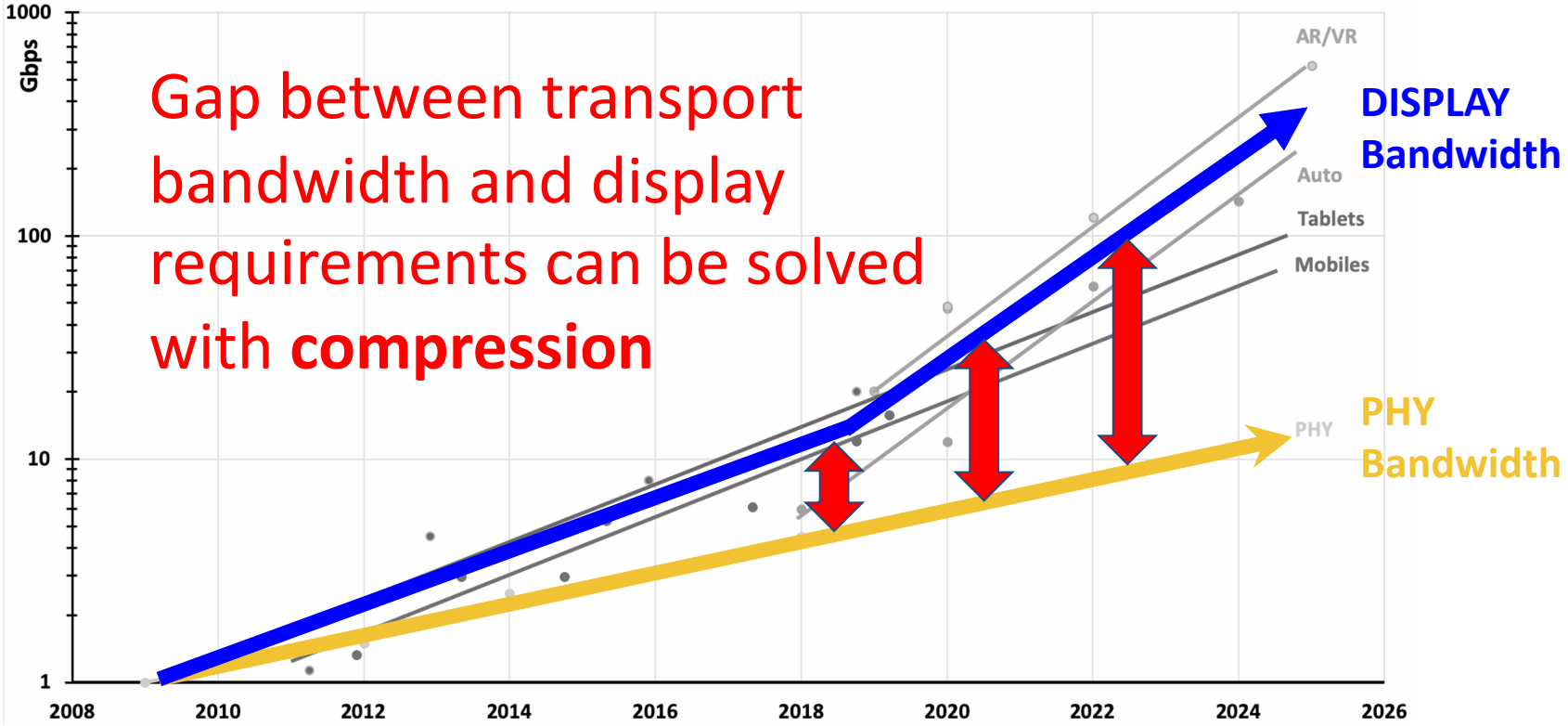
AR/VR Displays

- Need to drive two displays
- Require higher pixel density (ppi), higher pixel resolutions (bpc) and frame rates

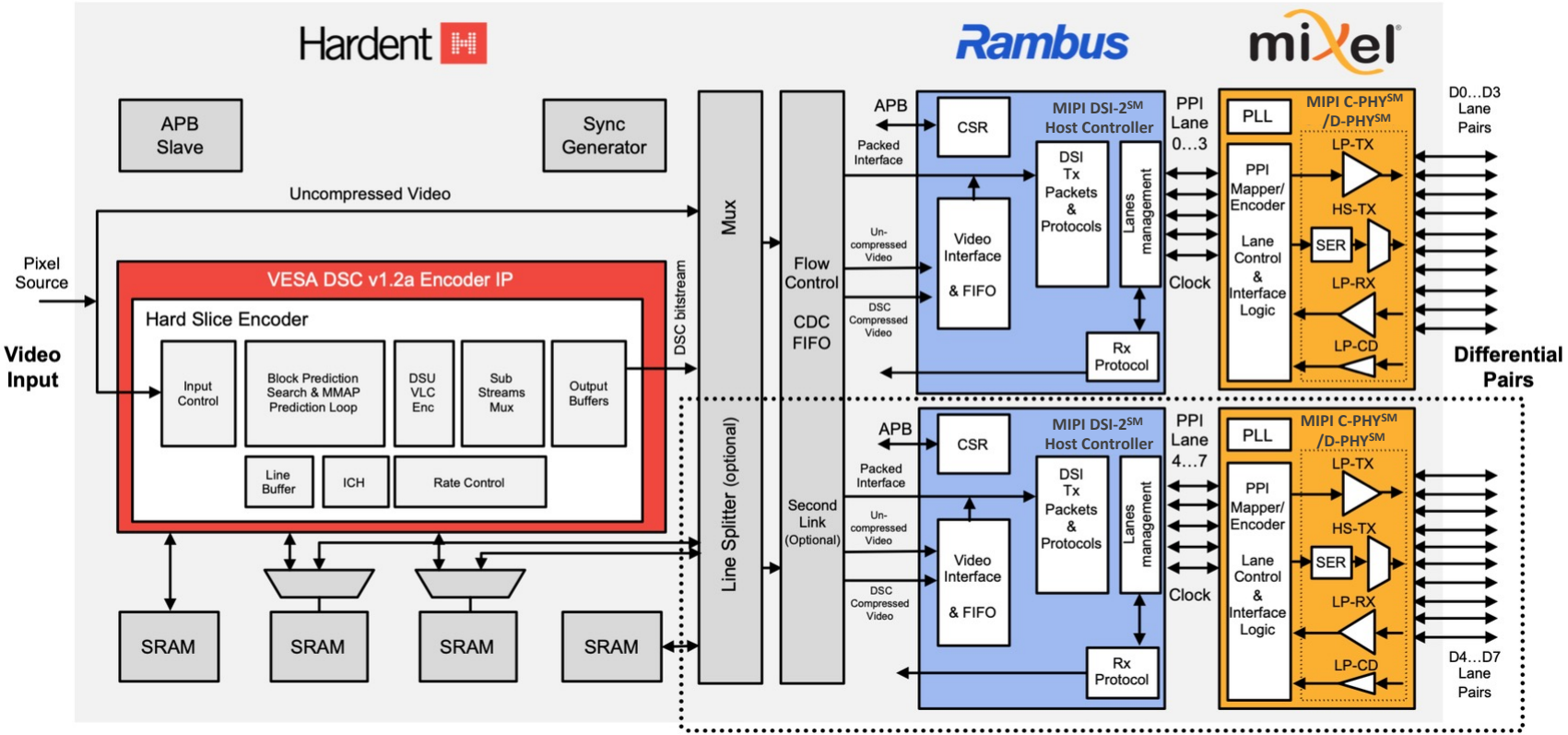
Automotive Displays

- More displays
- Require higher resolutions
- Multiple input sensors

Bandwidth Challenge for Video Connectivity



Host IP Subsystem Integration



Dual link configuration shown; single link also supported. Dotted line shows second link.

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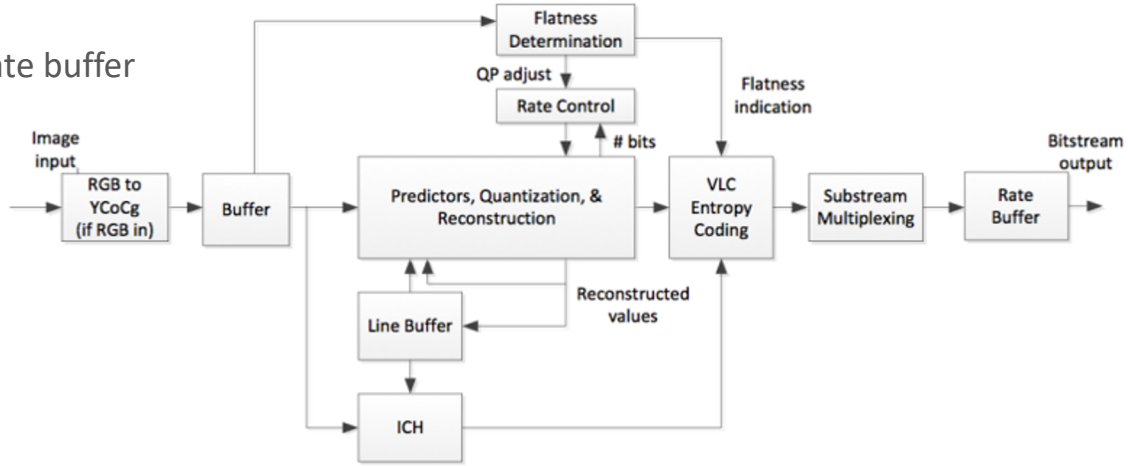
Hardent VESA DSC Compression IP

About Hardent

- First IP provider to bring VESA DSC IP cores to market in 2014
- VESA DSC IP cores are silicon proven
  - Over 100 design wins across a wide range of industries
- Active contributor to industry standards organizations
  - VESA member since 2013
  - MIPI Alliance member since 2015

VESA DSC Algorithm Overview

- Visually lossless video compression standard
- Compression as low as 8bpp without any perceptible differences
- Extremely low latency
- Video quality **excellent** with **all types of content**
  - Natural and test images, text, and graphics
- Requires a single line of pixel storage + rate buffer
- Intra-frame Variable Bit Rate Encoder
- Constant Bit Rate (CBR) transmission
- Based on Delta Pulse Code Modulation (DPCM)
- Mid Point (MPP), Block Predictor (BP)
- Modified Median Adaptive Predictor (MMAP)
- Indexed Color History (ICH)



Source diagram: VESA DSC white paper

Applications Using VESA DSC

- Mobiles
- Tablets
- Test Equipment
- GPUs
- AR/VR head-mounted displays
- In-car video systems
- Video transport
- 8K TVs
- DTV STBs
- High-res. monitors

Hardent DSC 1.2a IP: Key Features

- Backward compatible with DSC v1.1
- Supports all DSC mandatory and optional encoding mechanisms
  - Modified Median Adaptive Predictor (MMAP), Block Predictor (BP), Mid Point (MPP) and Indexed Color History (ICH)
- Transport stream agnostic
- Scalable number of parallel hard slice instances (1, 2, 4, and 8)
- RGB 4:4:4, YCbCr 4:2:0, and YCbCr 4:2:2 native coding
- 8, 10, 12, 14 and 16-bit video components
- 3 pixels / clock internal processing decoder architecture
- 1 pixel / clock internal processing encoder architecture
- Optional DSC features can be disabled to improve area (decoder only)
- Verified against VESA DSC C-model using comprehensive test image library

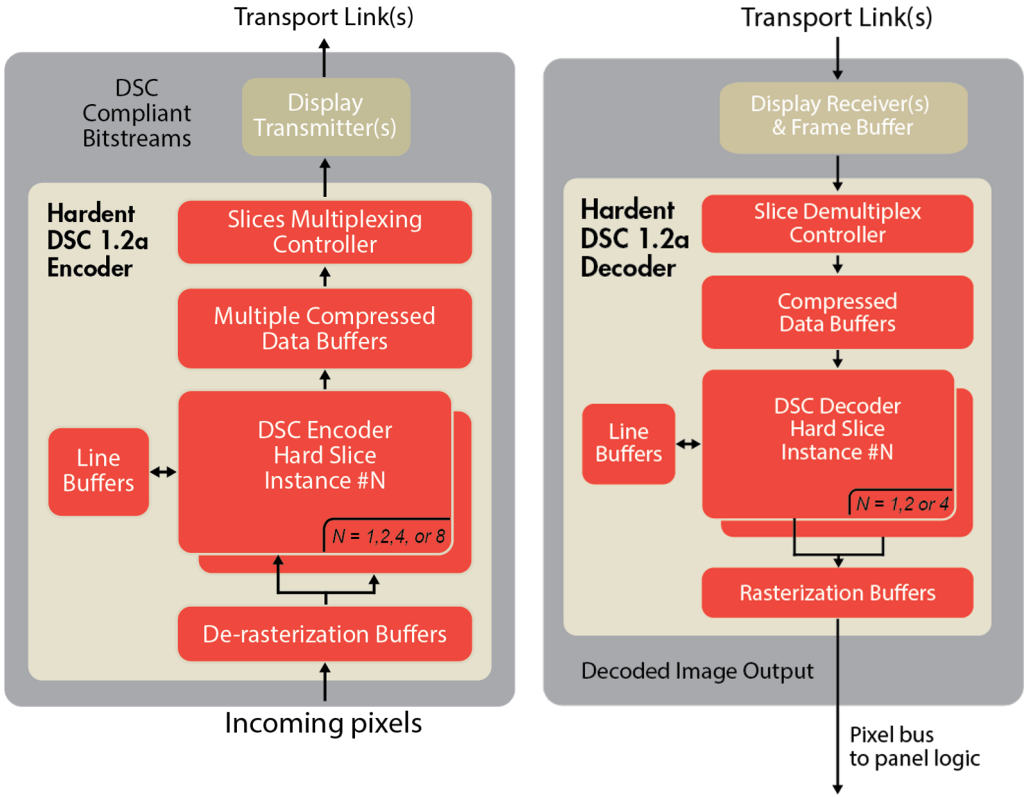
Hardent DSC 1.2a IP: Key Features

Hardent DSC v1.2a Decoder IP

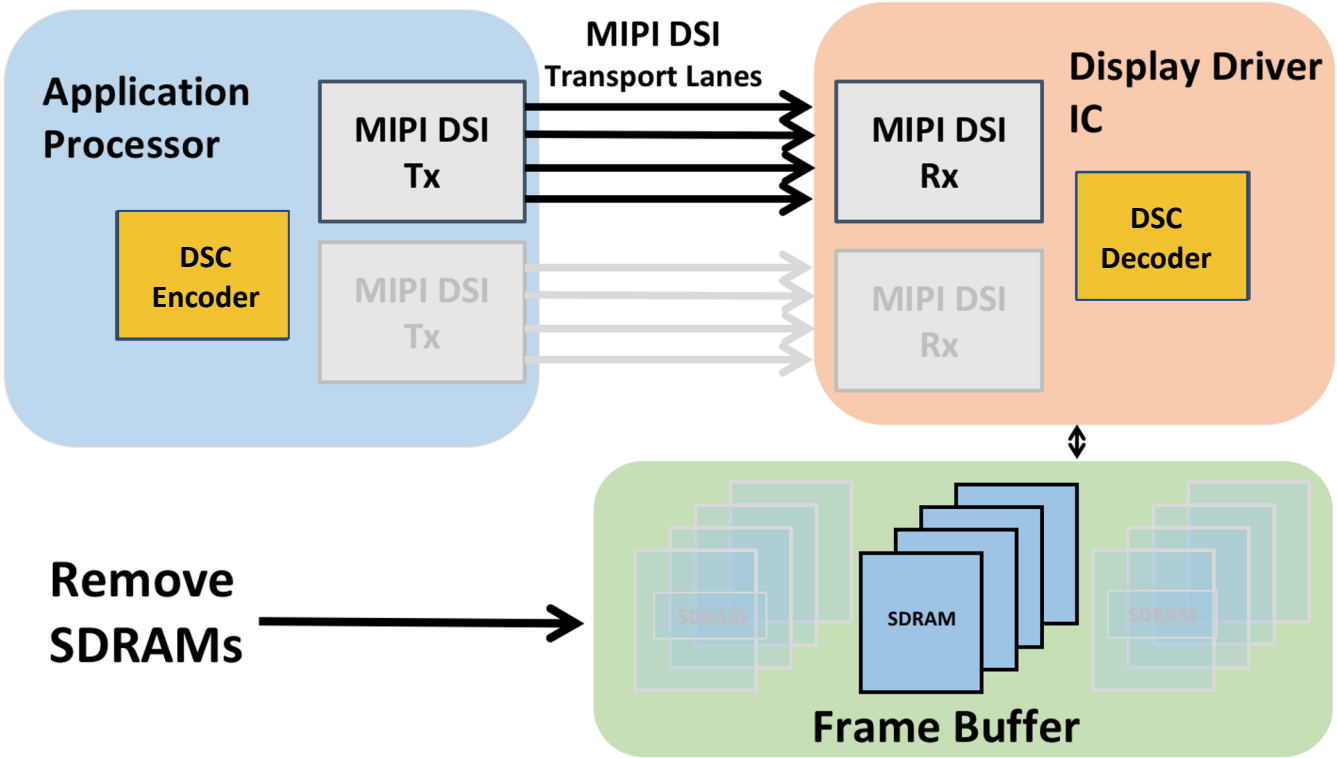
- Multiple parallel decoder instances
- Single or multiple inputs
- Rasterized output
- Error resilience
- Low power & high performance

Hardent DSC v1.2a Encoder IP

- Multiple parallel encoder instances
- Single input with de-rasterization or multiple inputs
- Single multiplexed output or multiple outputs
- Synchronous or asynchronous dataflow
- MIPI DSI command mode supported
- Low power & high performance



DSC Helps Save Power, Area, and Cost



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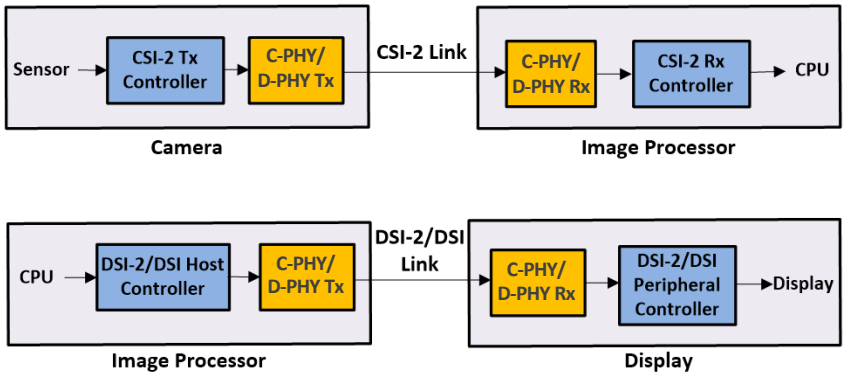
Rambus MIPI DSI-2SM Controller

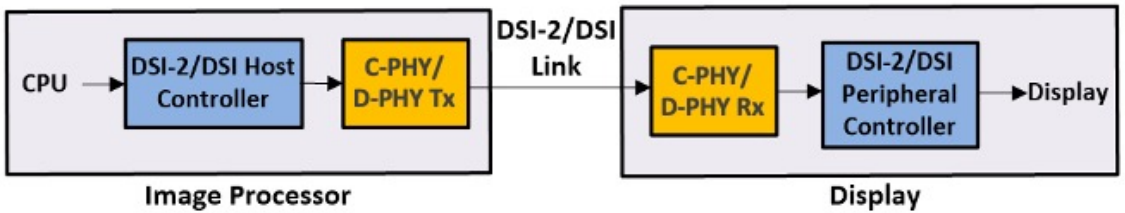
Rambus is a Leading Provider Of MIPI Controller Cores

- Rambus has been supplying MIPI Controller cores since 2010
  - Optimized 2nd generation CSI-2 and DSI-2 Controllers available
  - Fast deployment of new standards
  - Full featured
  - Full support for C-PHY/D-PHY
  - Full support for DSC
- MIPI Controller Cores widely used in ASIC and FPGA
  - 100+ ASIC design wins
  - 130+ FPGA design wins
- Delivered fully integrated and verified with ASIC PHY
  - Comprehensive PHY integration and validation process



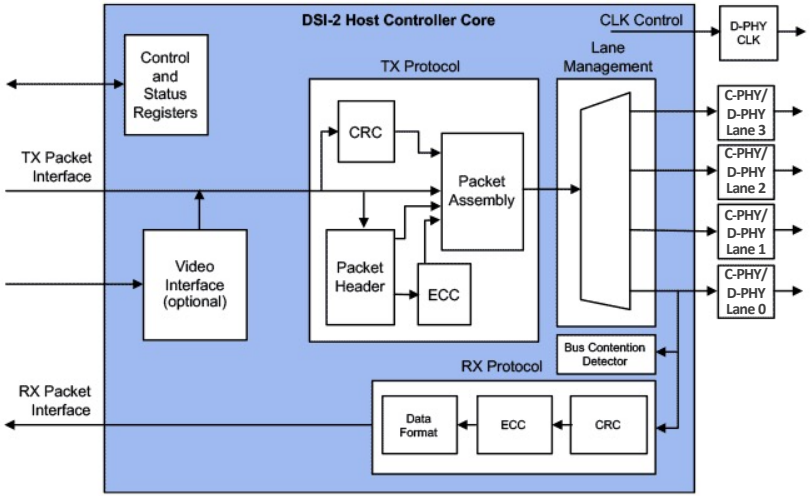
DSI-2 Controller Core Key Features

- Fully DSI-2 Specification compliant
- PHY Support
  - 1-4 D-PHY lanes
  - 1-4 C-PHY lanes
- 32 and 64-bit core width versions
  - Support for all data types
- Flexible packet interface
- Support for extended virtual channels
  - Optional DSI-2 Video Interface
- Support for Hardent DSC
- Delivered fully integrated with target MIPI PHY
- Minimal ASIC gate count
- Provided with expert technical support
- Provided with a DSI-2 Testbench
- Customization and integration services available
- Support for FPGA prototyping
  - Off the shelf or with PHY test IC



DSI-2 Video Interface

- DPI-2SM standard was established prior to the MIPI DSI standard
  - Hsync/Vsync style interface
  - Single pixel per clock
  - Limited data types (RGB 16/18/24 bit)
- DSI-2 Video Interface is a superset of DPI-2 Interface
  - Multiple pixel per clock support
  - All DSI-2 data types (RGB, YUV, etc.)
  - Minimized FIFO size relative to DPI-2 Interface
  - Enhanced sync retiming support
- Enables Hardent DSC integration



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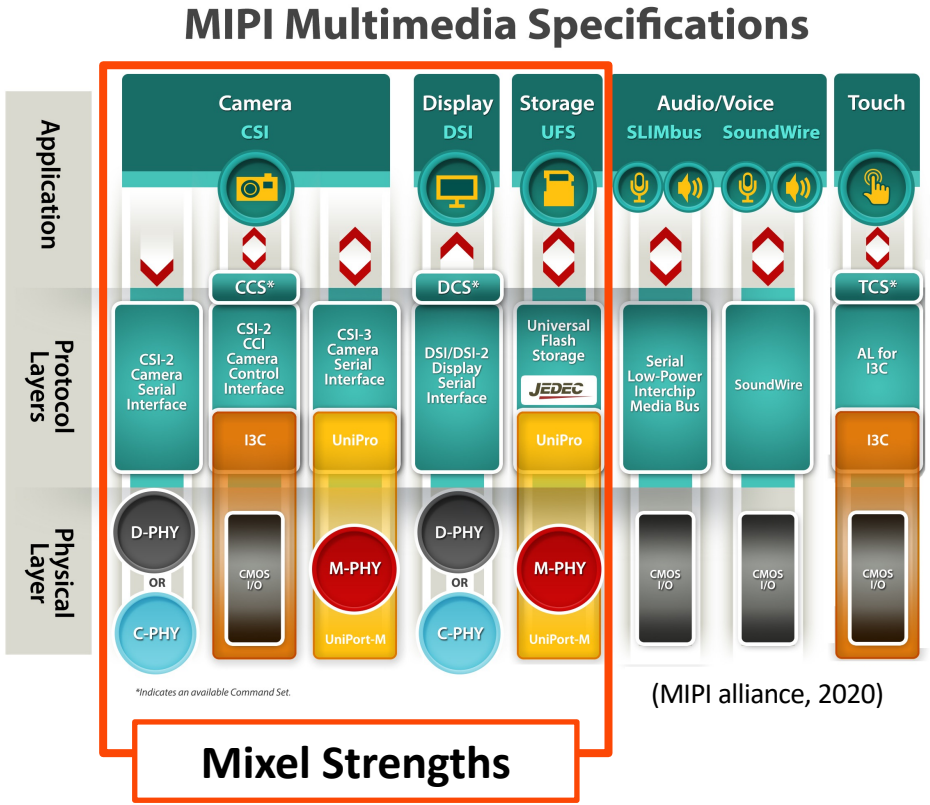
Mixel MIPI C-PHY℠/D-PHY℠

About Mixel

- Leading provider of mixed-signal IP since 1998 with emphasis on PHY including:
  - MIPI PHY: D-PHY, C-PHY, M-PHY®
  - LVDS SerDes
  - Multi-standard SerDes: C-PHY/D-PHY, LVDS/D-PHY
- Industry leader in MIPI® interfaces and contributing member of the MIPI Alliance since 2006
- Complete integrated solution includes PHY, controller, and platform
- First IP provider to demonstrate silicon-proven D-PHY, C-PHY, and M-PHY
- Widest coverage of process nodes and foundries: silicon-proven in **11** different nodes and **8** different foundries

MIPI PHY Applications

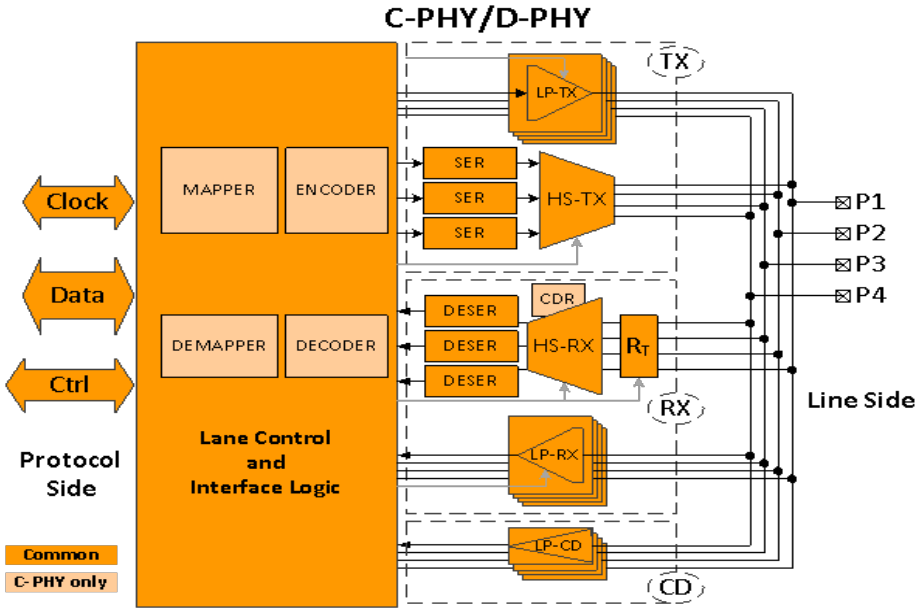
- Requiring high bandwidth, low power and minimal area:
  - Mobile
  - Automotive
  - IoT/Sensor
  - VR/AR/MR
  - Other consumer electronics



(MIPI alliance, 2020)

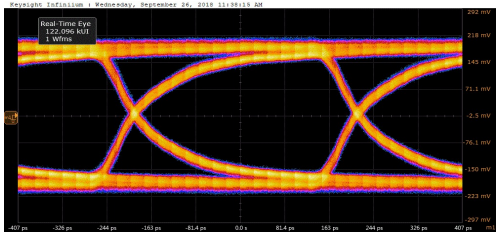
Mixel MIPI C-PHY/D-PHY Combo

- Combo PHY can be configured as either a C-PHY or D-PHY
- Configurable for transmit (TX) and receive (RX), plus additional optimized configurations for TX and RX provide smaller area and higher performance
- Supports Camera Serial Interface (MIPI CSI-2) and Display Serial Interface (DSI, DSI-2)
- MIPI D-PHY mode supports MIPI D-PHY v2.5 Specification
- Up to 4.5 Gbps data rate per lane with De-skew calibration
- Up to 4 lanes, 18 Gbps aggregate bandwidth
- MIPI C-PHY mode supports MIPI C-PHY v2.0
- 80 Msps to 4.5 Gsps symbol rate per lane in high-speed mode
- Up to 3 trios, 13.5 Gsps/30.78 Gbps aggregate bandwidth

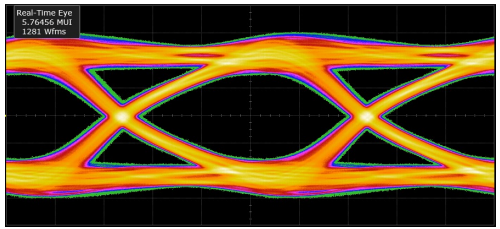


Multiple Generations of Mixel MIPI IP

Mixel MIPI D-PHY

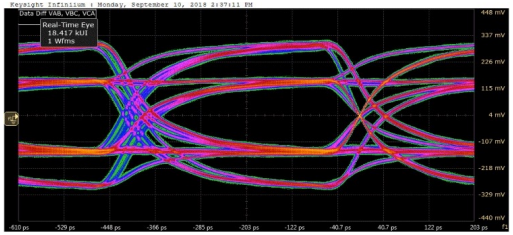


D-PHY @ 2.5 Gbps

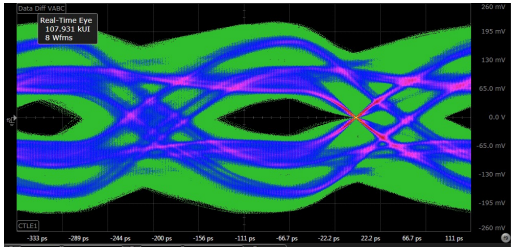


D-PHY @ 4.5 Gbps

Mixel MIPI C-PHY



C-PHY @ 2.5 Gsps



C-PHY @ 4.5 Gsps

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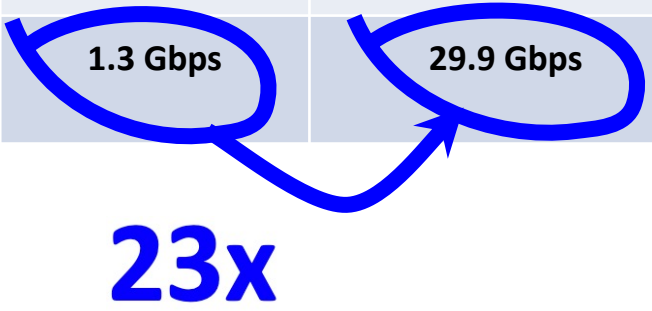
Use Cases: Mobile, AR/VR & Automotive

Mobile Market Trends

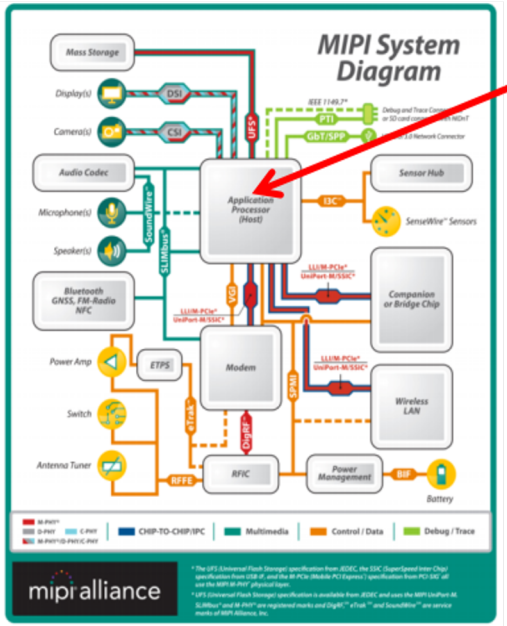
- Mobile devices need to be XR-ready
- Movement from LCD to OLED displays with sub-pixel rendering
  - Ultra-high resolutions and pixel density (up to 1500 ppi)
  - High dynamic range (HDR)
  - Higher frame rate
  - Optical compensation
  - Foldable, rollable displays
  - Lower power consumption
  - Non-uniformity compensation
- DDIC frame buffer going from 10 to 100 Mbits

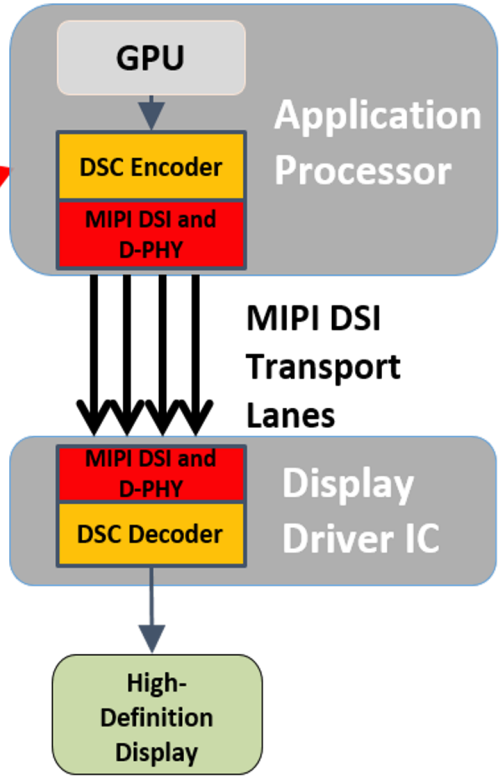
	2010	2020
Display Resolution	**1280 x 720 HD**	**3840 x 2160 4K**
Frame Rate	**60 fps**	**120 fps**
Pixel Depth	**24 bits**	**30 bits**
Interface	**0.5 Gbps / lane**	**2.0 Gbps / lane With DSC**
Display Bandwidth	**1.3 Gbps**	**29.9 Gbps**



Use Case: Mobile and Tablet Applications

- Benefits
  - Reduce bandwidth
  - Save power
  - Lower EMI
  - Lower cost
  - Smaller footprint
  - Less pins
  - Lower switching frequencies





D-PHY Speed/Display Resolution

D-PHY v1.1 1.5 Gbps / lane

Resolution	FHD (1080x1920)	WQHD (1440x2560)	WQXGA (1600x2560)	UHD (2160x3840)	WQUXGA (2400x3840)	5K (2880x5120)	8K (4320x8192)
Bandwidth	3.58Gbps	6.37Gbps	7.08Gbps	14.33Gbps	15.93Gbps	25.49Gbps	61.16Gbps
No compression	3 lanes	6 or 8 lanes	6 or 8 lanes	N/A	N/A	N/A	N/A
2x compression	2 lanes	3 lanes	3 lanes	8 or 6 lanes	8 or 6 lanes	N/A	N/A
3x compression	1 lane	2 lanes	2 lanes	4 lanes	4 lanes	8 lanes	N/A

D-PHY v1.2 2.5 Gbps / lane

Resolution	FHD (1080x1920)	WQHD (1440x2560)	WQXGA (1600x2560)	UHD (2160x3840)	WQUXGA (2400x3840)	5K (2880x5120)	8K (4320x8192)
Bandwidth	3.58Gbps	6.37Gbps	7.08Gbps	14.33Gbps	15.93Gbps	25.49Gbps	61.16Gbps
No compression	2 lanes	3 lanes	3 lanes	8 or 6 lanes	8 lanes	N/A	N/A
2x compression	1 lane	2 lanes	2 lanes	3 lanes	4 lanes	8 or 6 lanes	N/A
3x compression	1 lane	1 lane	1 lane	2 lanes	3 lanes	4 lanes	N/A

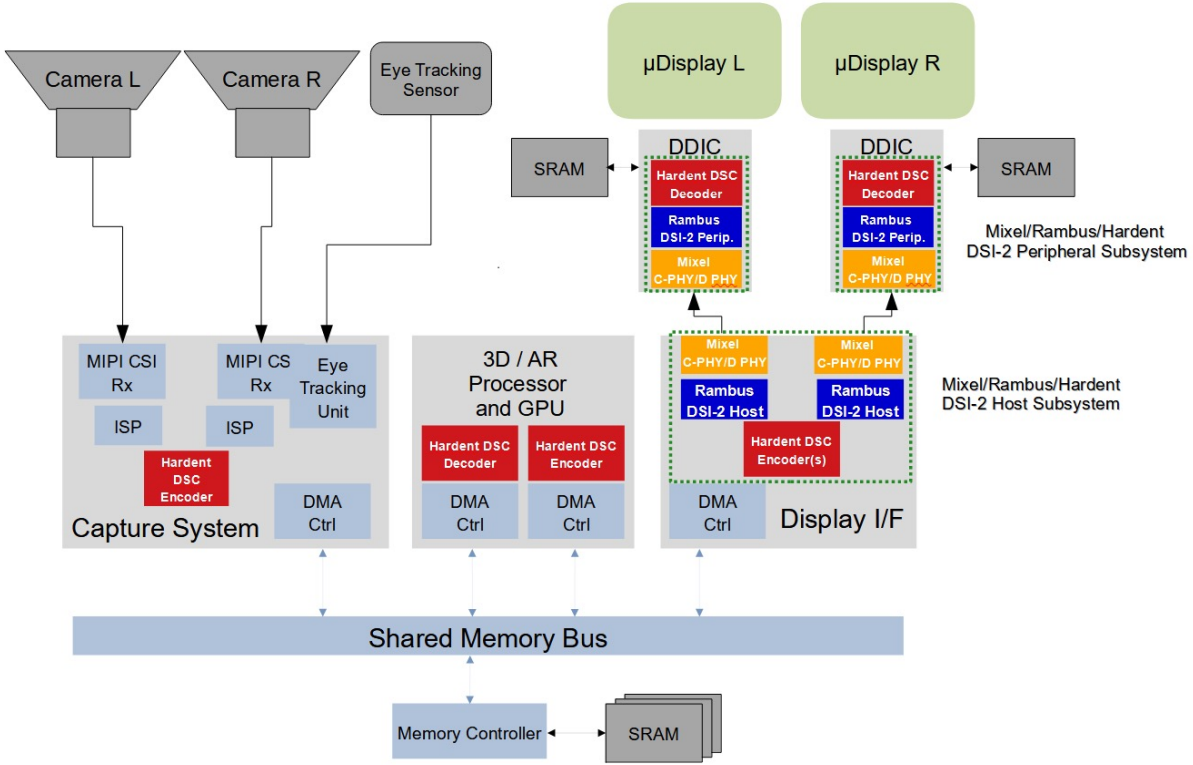
AR/VR Market

- Challenges
  - Requires 2 displays at higher resolution, higher PPI, higher refresh rates
  - Tethered HMD
    - Cables are running out of bandwidth

  - Wireless HMD
    - Bandwidth, power management, and miniaturization are huge obstacles

Use Case: AR Head-Mounted Display (HMD)

HMD AR System With Frame Buffer



Applications

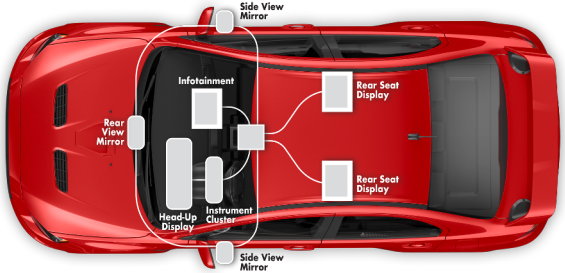
- Images captured by 3D camera
- Video and graphics processed by AR processor and GPU
- L/R video streams sent to micro-displays (DSI-2 Link)
- Video stored inside micro-display driver IC (Frame Buffer)

Benefits

- Lower bandwidth
- Smaller RAM buffer
- Power and $ savings
- Low latency

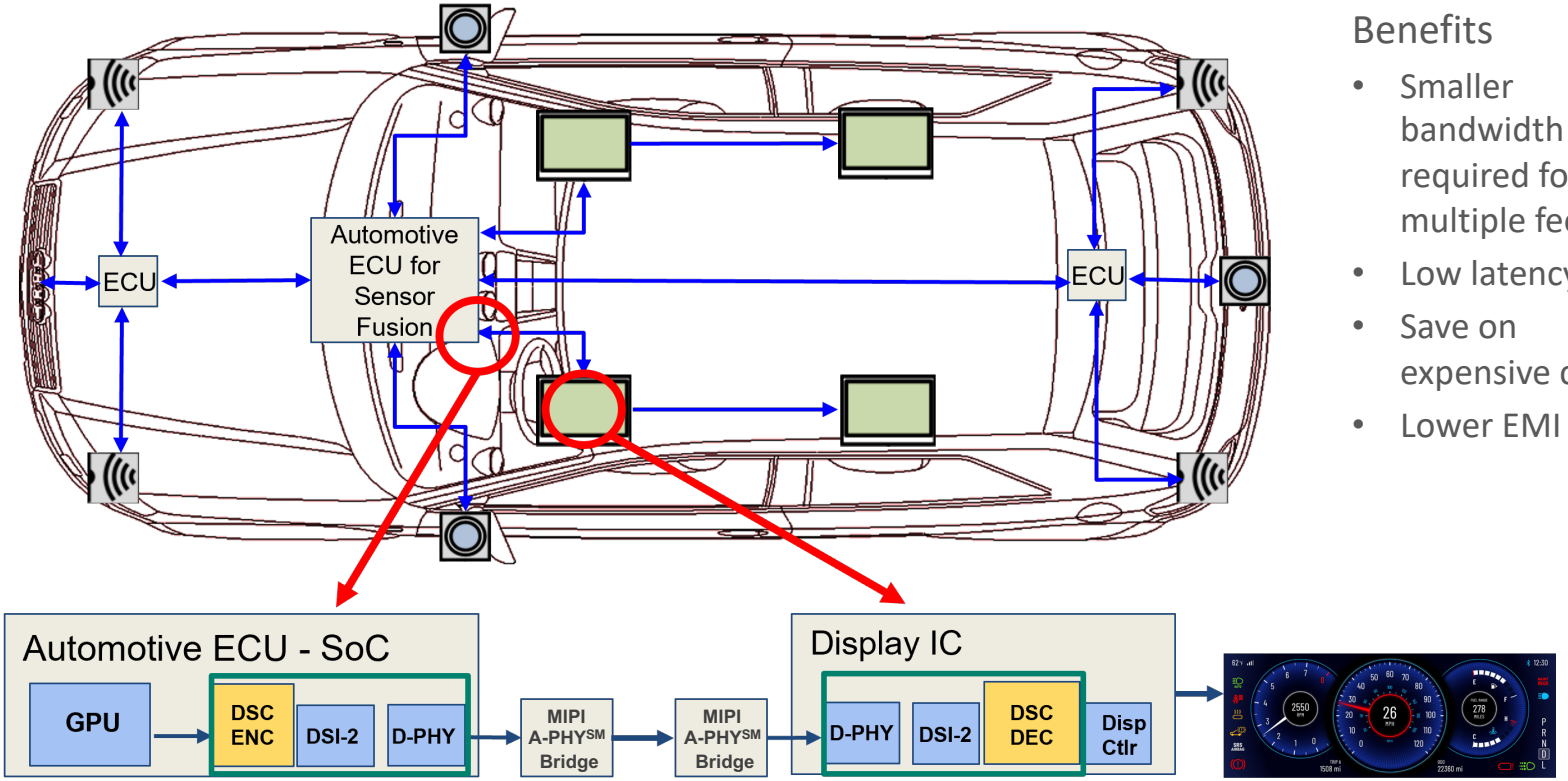
Automotive Market

- The number of displays and cameras in cars is increasing rapidly
  - ADAS, ACAS, infotainment, control panels, rear seat displays, head-up displays, side and rearview mirrors, …
    - 1-3 displays → 10-12 displays
    - 1 camera → 5-10 cameras
    - 2-5 sensors → 10-20 sensors



Display Type	Spatial Resolution		DPI (pix / inch)	Bandwidth Req. @ 60 Hz refresh
Mid-range car	HD	1280 x 720	100	1.8 Gbps
High-end car	FHD	1920 x 1080	200	3.6 Gbps
Next-gen. car	UHD	3860 x 2160	400	14.4 Gbps

Automotive Video Applications



Benefits

- Smaller bandwidth required for multiple feeds
- Low latency
- Save on expensive cabling
- Lower EMI

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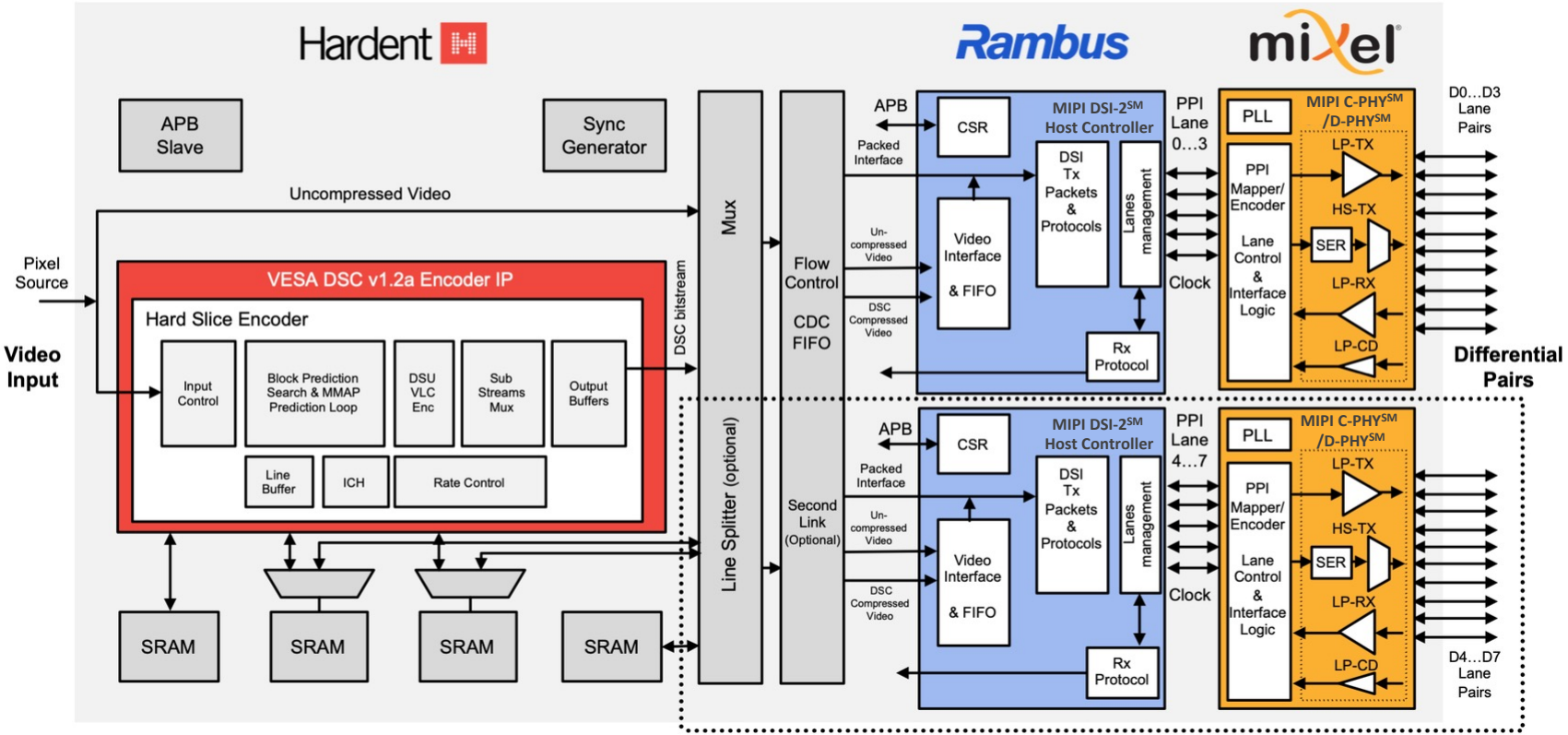
Integrated IP Subsystem Solution

Host IP Subsystem Integration



Dual link configuration shown; single link also supported. Dotted line shows second link.

DSI-2 DSC IP Subsystem Deliverables

DSI-2 Controller Core Deliverables

- DSI-2 Controller Core – Source Code
  - Fully configured for application
  - Fully integrated and verified with D/C-PHY
  - User Guide, integration guide, timing constraints
  - Optional FPGA prototyping
- Testbench – Source Code
  - DSI-2 Peripheral or Host Testbench with DSI-2 Host or DSI-2 Peripheral BFM and C-PHY/D-PHY Behavioral Model
- Expert Technical Support
  - One year of expert technical support
  - Optional services available (IP customization, logic development, etc.)

DSC 1.2a IP Core Deliverables

- Encrypted synthesizable RTL code
- 100% verification coverage using a comprehensive UVM verification environment
- Functional and structural verification coverage reports
- IP testbench for post-synthesis verification
- Comprehensive integration guide
- Technical support

C-PHY / D-PHY IP Core Deliverables

- Data Sheet/Specifications
- Integration guidelines
- GDS II data base
- LEF file
- LVS netlist
- Timing model
- Verilog model
- IBIS model
- RTL
- Test Benches
- First-class customer support through production

IP Integration Benefits and Conclusion

- Lower project risk with a fully integrated and verified IP solution
- Maximized functionality and availability of all MIPI DSI-2 operating modes
- Optimized for ASIC design performance (PPA)
- Accelerate ASIC and SoC time to market
- Immediate availability

Demo

View a demo of the IP subsystem later today

08:05 to 08:15 PDT

More Information

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