



mipi[®]
DEVCON

Yafit Snir
Arindam Guha

Cadence Design Systems, Inc.

**Accelerating System level Verification of SOC
Designs with MIPI Interfaces**



2017
MIPI ALLIANCE
DEVELOPERS
CONFERENCE

HSINCHU CITY, TAIWAN
MIPI.ORG/DEVCON

Agenda

- Overview: MIPI Verification approaches and challenges
- Acceleration methodology overview and advantages
- Accelerated verification IP Architecture
- Migration guidelines: from simulation to acceleration
- Virtual emulation using MIPI virtual device models
- Demonstration

Cadence Design Systems

Agenda

- Overview: MIPI Verification approaches and challenges
- Acceleration methodology overview and advantages
- Accelerated verification IP Architecture
- Migration guidelines: from simulation to acceleration
- Virtual emulation using MIPI virtual device models
- Demonstration

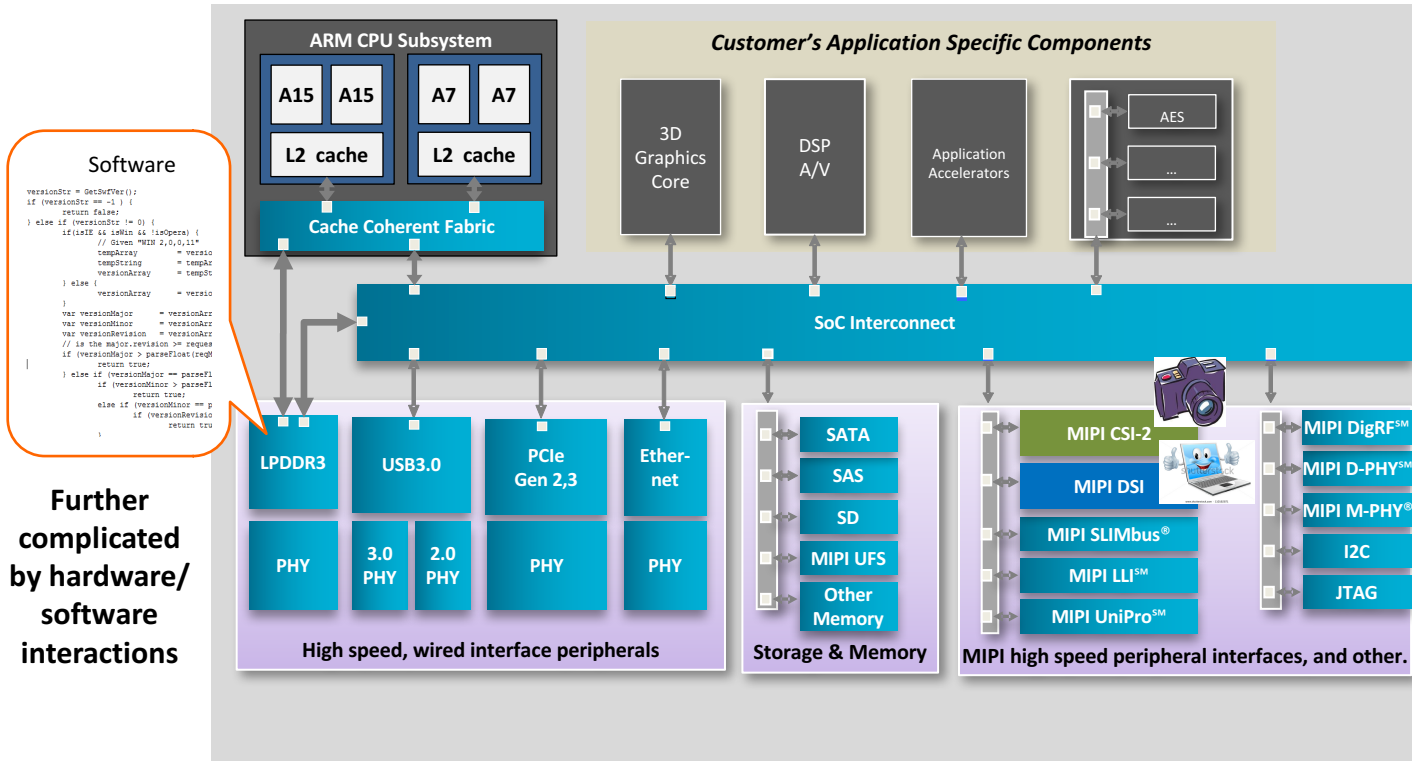
Cadence Design Systems

MIPI CSI-2SM & MIPI DSISM

- Widely adopted serial *high-speed protocols*.
- Implemented in complex systems, for a variety of applications in different markets:
 - Mobile
 - Automotive
 - Multimedia
 - Virtual reality, augmented reality and others

Cadence Design Systems

MIPI Interfaces usage example in Complex/Large SOC's



System Level Verification Challenges

- Complex and Large Designs.
 - Long simulation time
 - Need to reach system coverage goals prior to RTL freeze.
- Time to market: Requires parallel development of hardware and software design, early in development cycle..
- Validating software and hardware integration.
- Create and validate real world scenarios in a pre-silicon environment.

Cadence Design Systems

Overview of Current verification approaches

- Pure Simulation verification
 - Full controllability and coverage collection.
 - Acceptable performance for module/sub system.
- Hardware assisted verification
 - Enables High performance for sub system/system verification.
 - Enables pre-silicon HW/SW verification.
 - Enables running longer tests, with high throughput to reach interesting system scenarios, and validate performance.

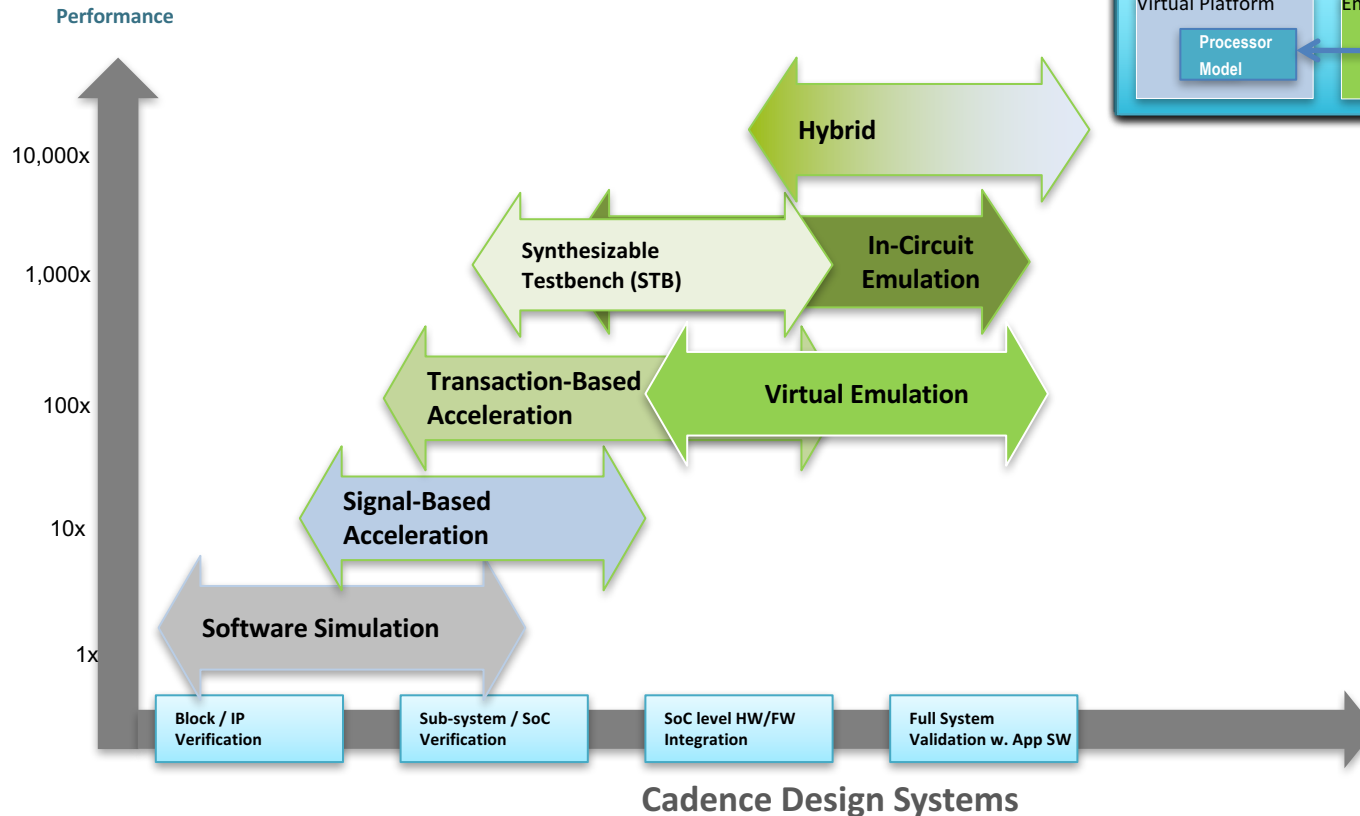
Cadence Design Systems

Overview of hardware assisted verification methods

- Simulation Acceleration
 - Accelerating hardware verification.
- Virtual Emulation
 - SW Driven HW Verification, SW/HW Validation
- In-Circuit Emulation
 - Enables real device connection
- FPGA Prototyping

Cadence Design Systems

Emulator Use Modes

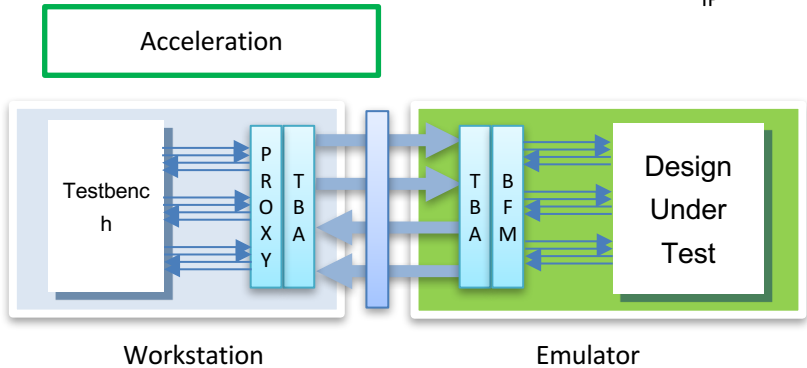
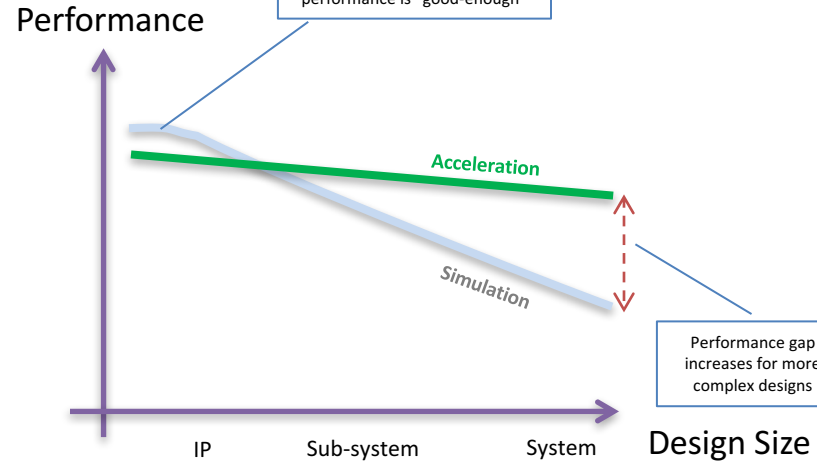
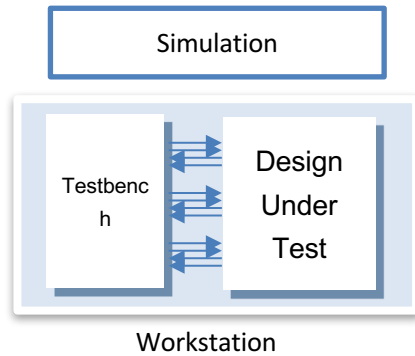


Agenda

- Overview: MIPI Verification approaches and challenges
- **Acceleration methodology overview and advantages**
- Accelerated verification IP Architecture
- Migration guidelines: from simulation to acceleration
- Virtual emulation using MIPI virtual device models
- Demonstration

Cadence Design Systems

Simulation vs. Acceleration

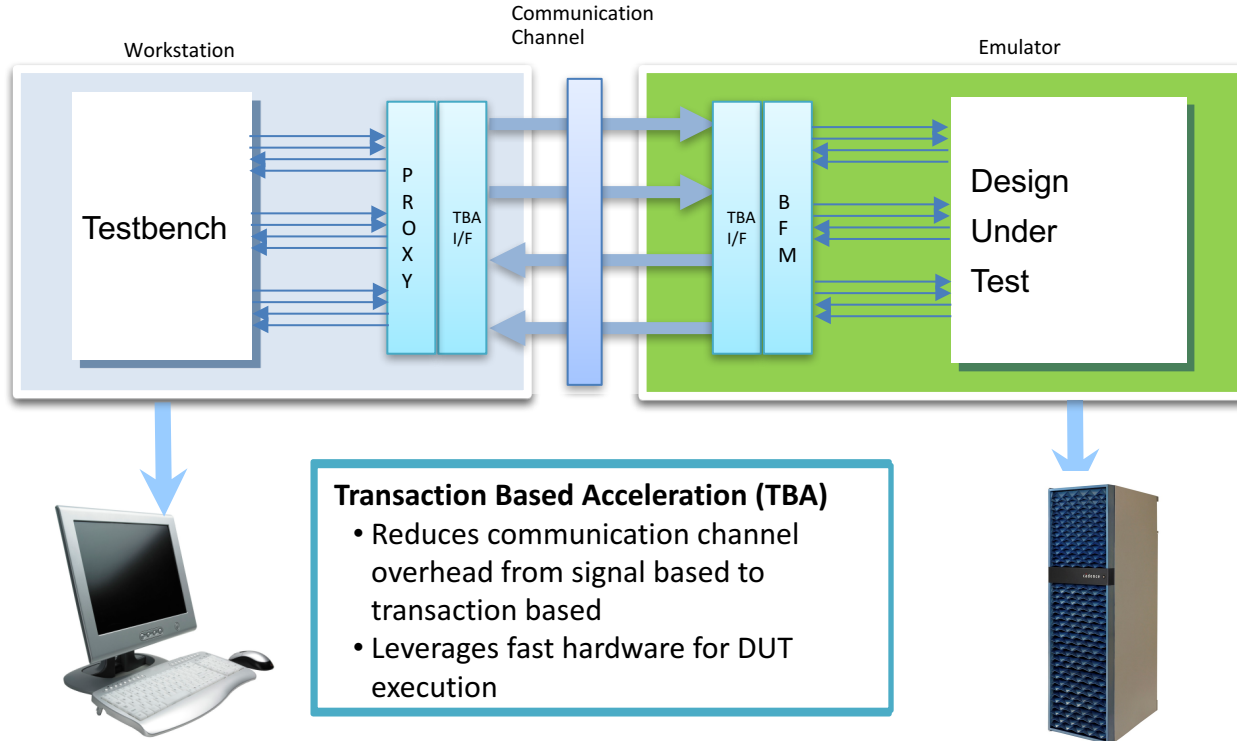


- Simulation-Acceleration mode**
- DUT runs at higher speeds than in general purpose CPU
 - Acceleration factor determined by TB time and synchronizations between TB and Emulator

Cadence Design Systems

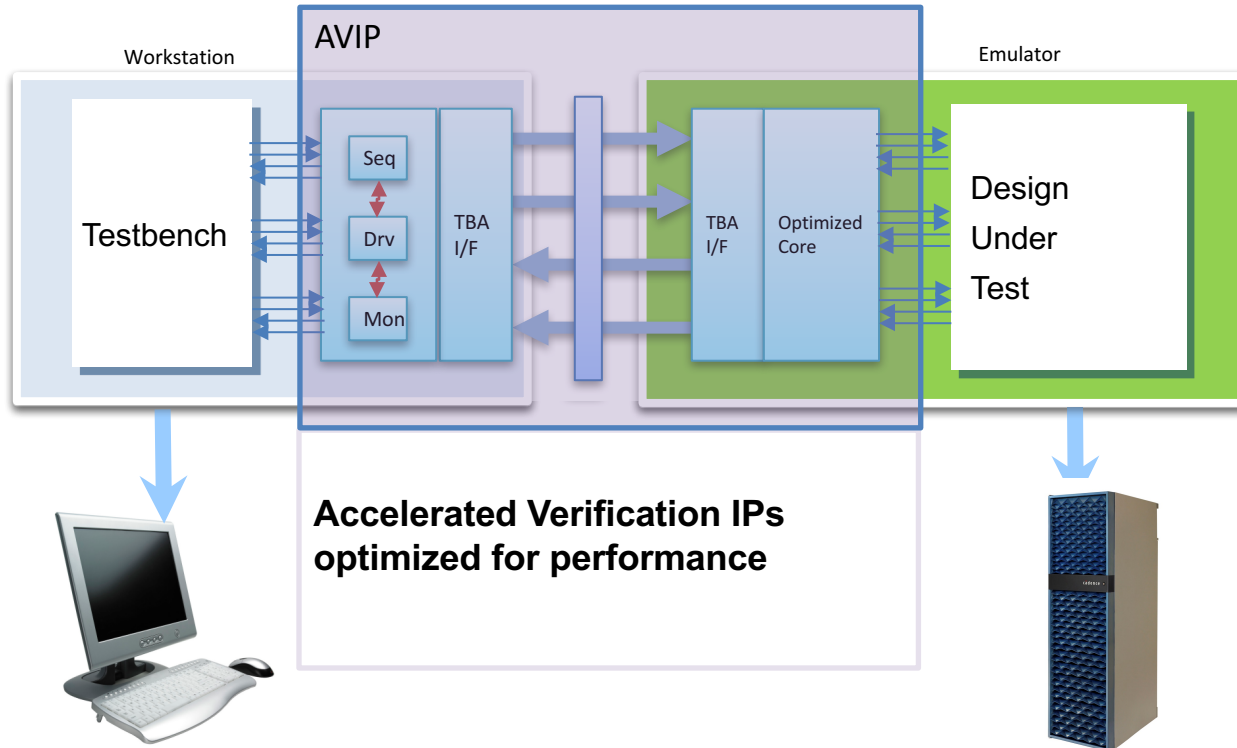
Acceleration

Signal Based Acceleration & Transaction Based Acceleration



Cadence Design Systems

Accelerated Verification IP (AVIP)



Cadence Design Systems

Acceleration Methodology Advantages

- Enables orders-of-magnitude gains in throughput over Simulation
- Enables re using selected parts of your simulation verification environment
- Enables advanced technologies with virtual emulation, like:
 - Hybrid operation for optimal partition of the design between HW and SW to achieve maximum speedup
 - Connection to Virtual Devices, Virtual machines, etc.
- Enables OS-level benchmarks and driver bring-up

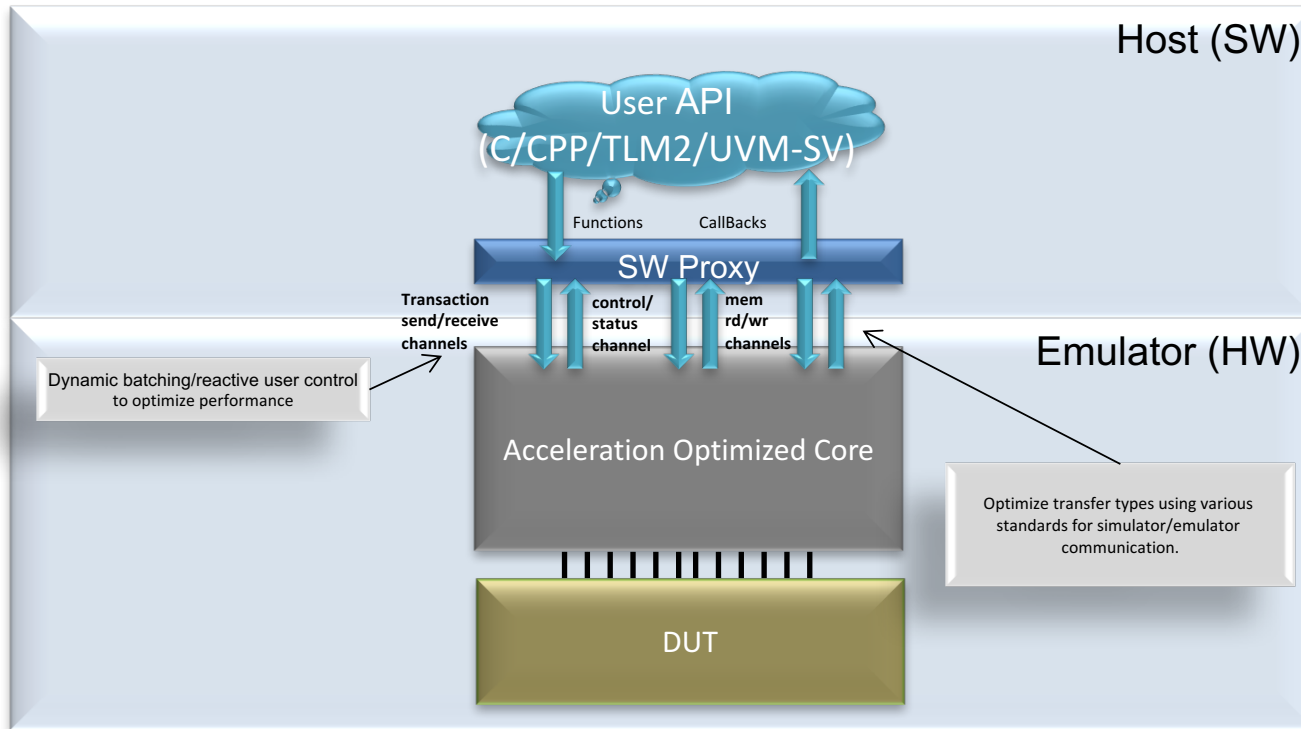
Cadence Design Systems

Agenda

- Overview: MIPI Verification approaches and challenges
- Acceleration methodology overview and advantages
- **Accelerated verification IP Architecture**
- Migration guidelines: from simulation to acceleration
- Virtual emulation using MIPI virtual device models
- Demonstration

Cadence Design Systems

Architecture of Accelerated Verification IP (AVIP)



Cadence Design Systems

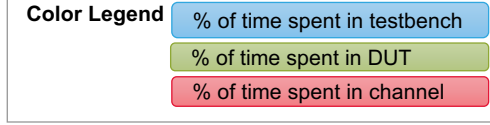
HSINCHU CITY, TAIWAN | 2017

Agenda

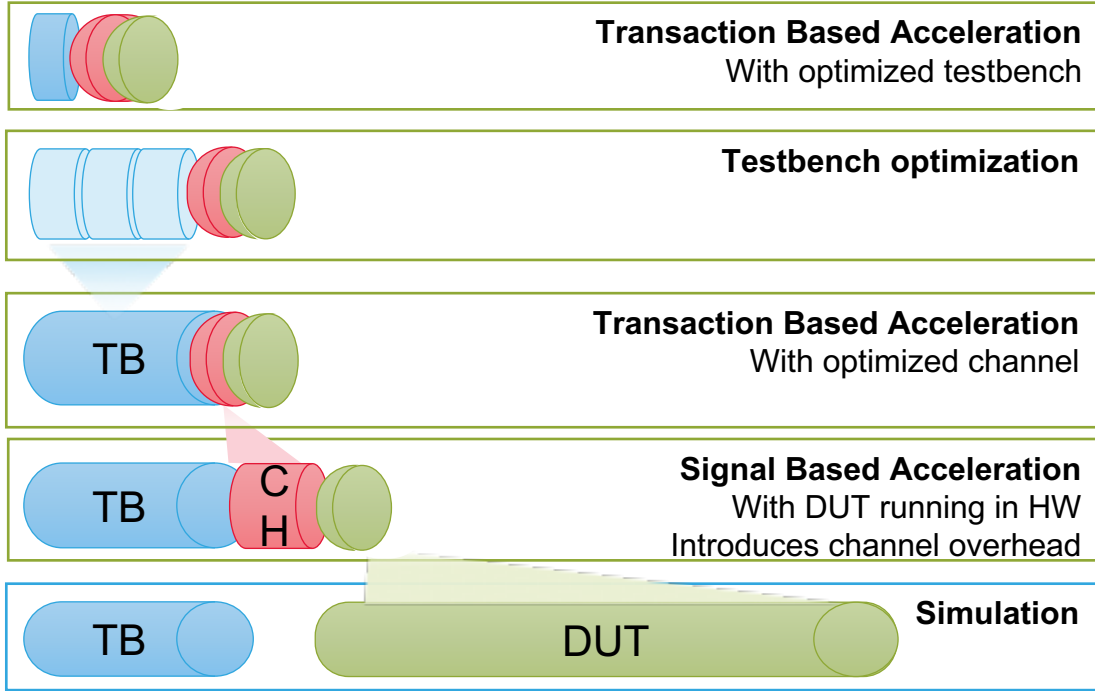
- Overview: MIPI Verification approaches and challenges
- Acceleration methodology overview and advantages
- Accelerated verification IP Architecture
- **Migration guidelines: from simulation to acceleration**
- Virtual emulation using MIPI virtual device models
- Demonstration

Cadence Design Systems

Optimizing Acceleration performance



Higher acceleration performance ↑



Transaction Based Acceleration
With optimized testbench

Testbench optimization

Transaction Based Acceleration
With optimized channel

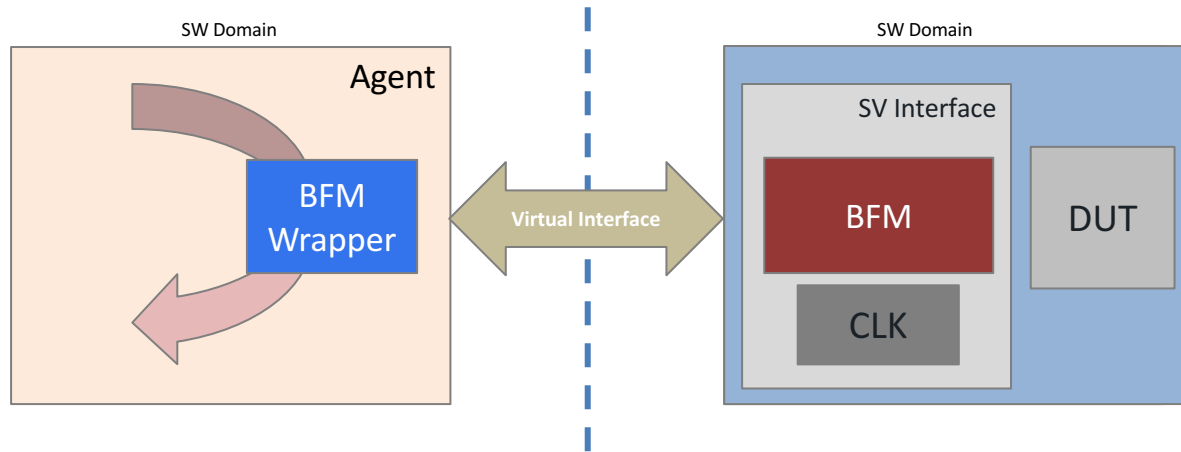
Signal Based Acceleration
With DUT running in HW
Introduces channel overhead

Simulation

- High level of acceleration
- Focus on sub-system & system level verification
- Optimize testbench by removing verification redundancies from IP-level - stimulus generation.
- Increase acceleration factor
- Reduce communication overhead
- Transactor may need modeling effort
- Quickest path to acceleration
- Maximize re-use of testbench
- Profile simulation runs to identify acceleration candidates
- Select runs that are long & spend large amount of time in DUT

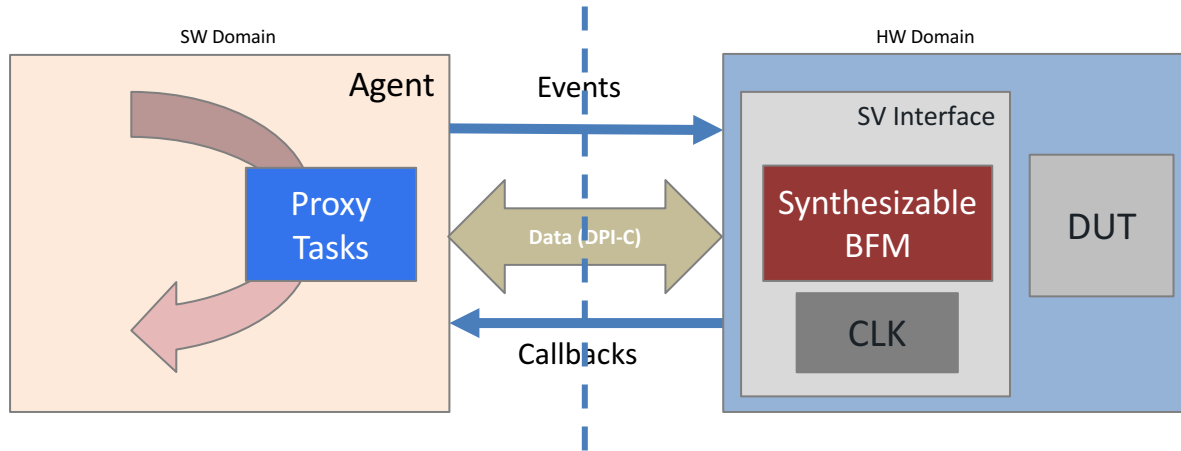
Cadence Design Systems

Acceleration Friendly UVC (at the Simulation Stage)



Cadence Design Systems

Acceleration Ready – UVC (at the Emulation Stage)



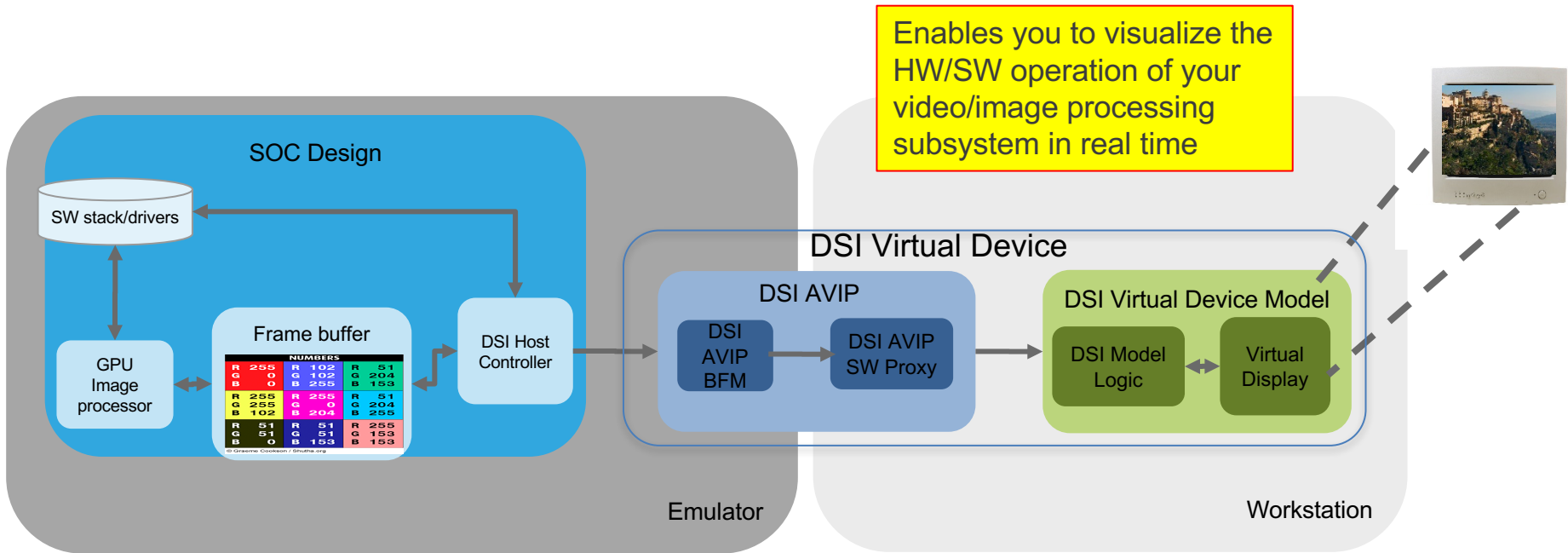
Cadence Design Systems

Agenda

- Overview: MIPI Verification approaches and challenges
- Acceleration methodology overview and advantages
- Accelerated verification IP Architecture
- Migration guidelines: from simulation to acceleration
- **Virtual emulation using MIPI virtual device models**
- Demonstration

Cadence Design Systems

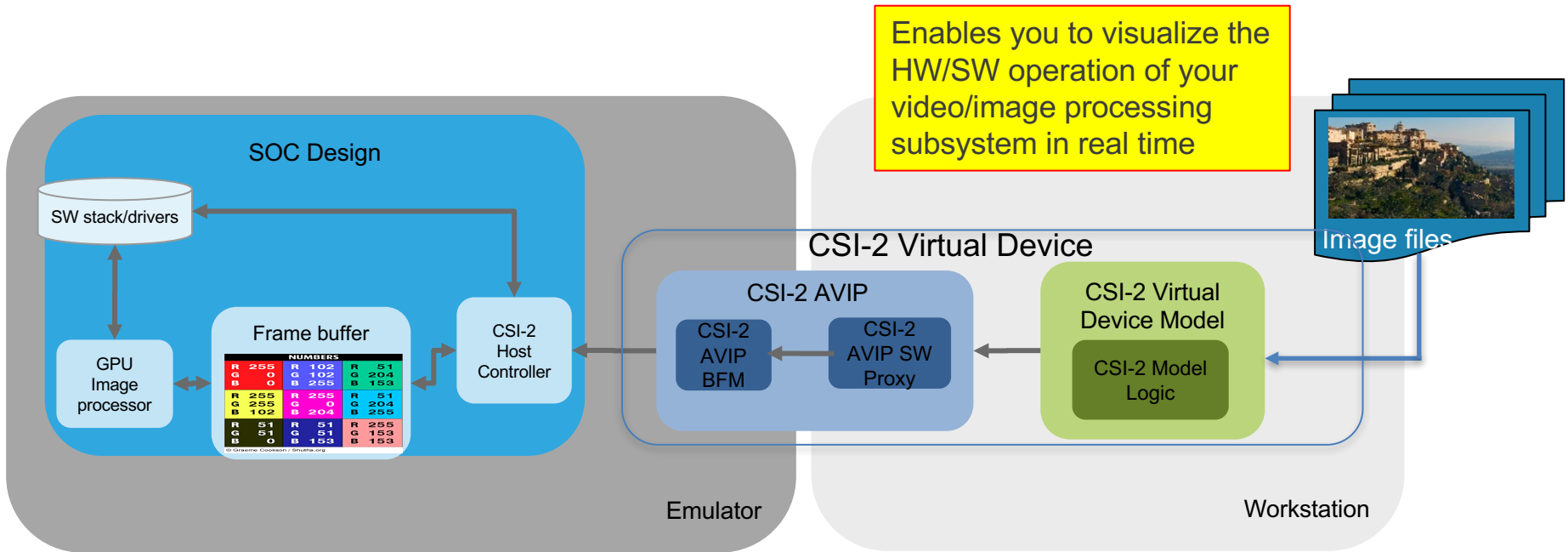
DSI Virtual Device



Cadence Design Systems

CSI-2 Virtual Device

Enables you to visualize the HW/SW operation of your video/image processing subsystem in real time

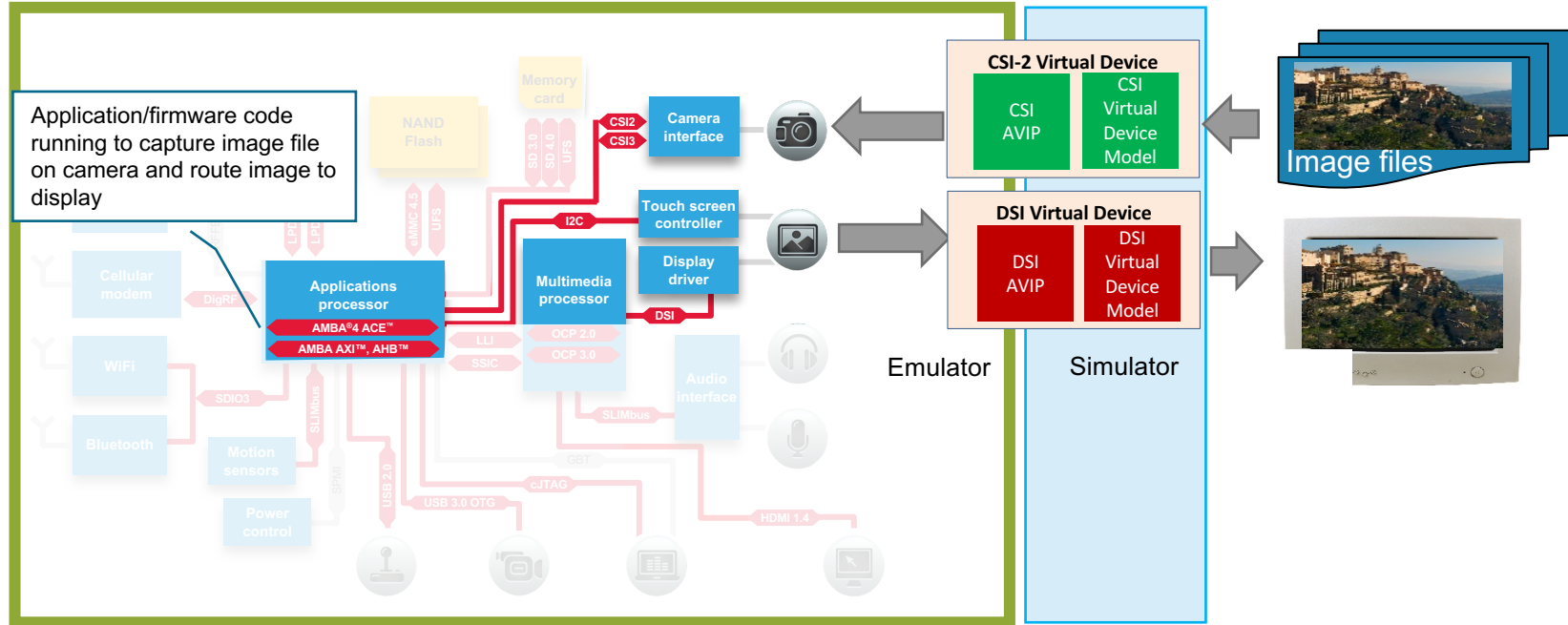


NUMBERS

R	255	R	102	R	51
G	0	G	102	G	204
B	0	B	255	B	153
R	255	R	255	R	51
G	255	G	0	G	204
B	102	B	204	B	255
R	51	R	51	R	255
G	51	G	51	G	153
B	0	B	153	B	153

Cadence Design Systems

Virtual Device Models usage example

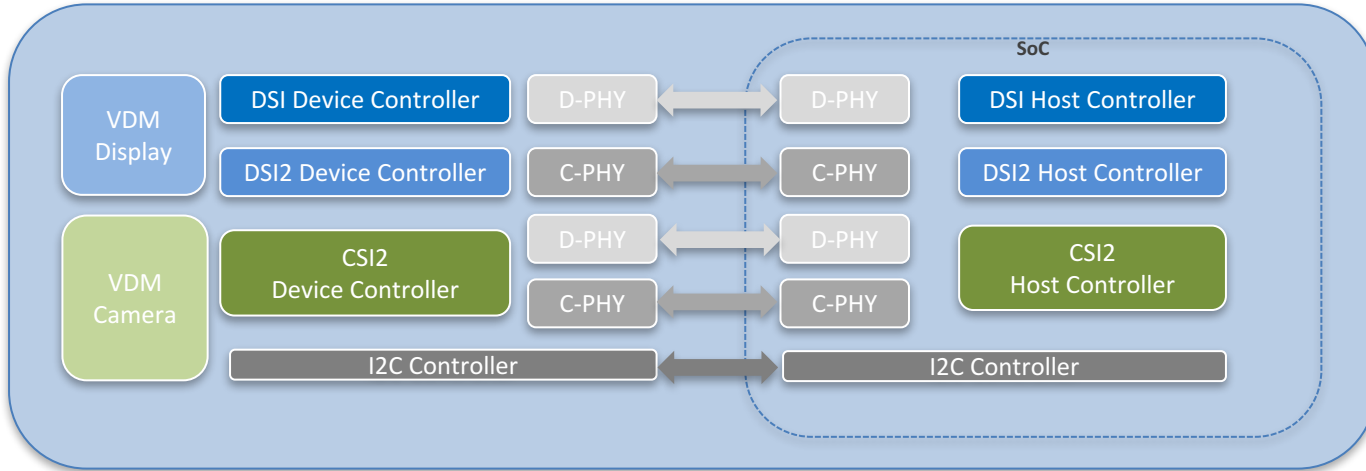


Cadence Design Systems

Agenda

- Overview: MIPI Verification approaches and challenges
- Acceleration methodology overview and advantages
- Accelerated verification IP Architecture
- Migration guidelines: from simulation to acceleration
- Virtual emulation using MIPI virtual device models
- **Demonstration**

Cadence Design Systems



To discuss Cadence MIPI Accelerated VIPs availability,
 Please contact: HSV_PM@cadence.com

Cadence Design Systems



mi^{pi}[®]
DEVCON

THANK YOU

HSINCHU CITY, TAIWAN

MIPI.ORG/DEVCON



2017

MIPI ALLIANCE
DEVELOPERS
CONFERENCE