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MIPI I3C℠ High Data Rate modes – How to speed up design verification?

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Introduction

The MIPI Alliance MIPI I3C℠ standardized sensor interface provides a number of significant advantages over existing digital sensor interfaces.

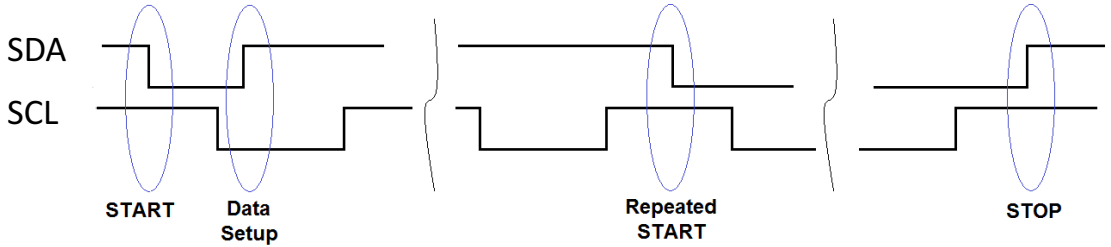
This paper will briefly present MIPI I3C℠ interface basics and will focus on various verification aspects of MIPI I3C℠ High Data Rate modes through an advanced verification methodology based on coverage driven verification and real-life scenarios

Single Data Rate Mode

- Single Data Rate (SDR) Mode is the default mode used by MIPI I3C℠
- MIPI I3C℠ Bus always initializes in SDR Mode
- Maximum data rate – 12.5 Mbps
- SDR is almost similar to I^2C, but introduces many new features not present in I^2C
- SCL wire operates as a clock signal, while the data is transferred using SDA wire

SDR Basics

- START Condition: SCL = High, SDA = High → Low
- STOP Condition: SCL = High, SDA = Low → High
- Transmitter writes data bit to SDA on falling edge of SCL
- Receiver(s) read data bit on rising edge of SCL

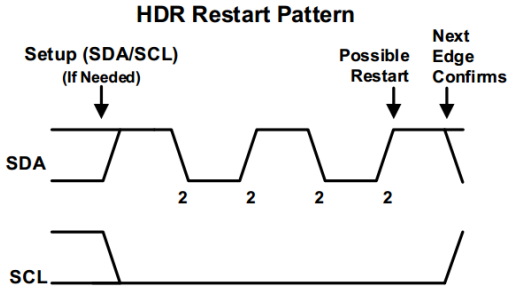


High Data Rate Modes

- MIPI I3C℠ High Data Rate modes allow to transfer more data while preserving SDR Frequency
- There are three MIPI I3C℠ HDR modes:
  - HDR-DDR – Double Data Rate mode
  - HDR-TSP – Ternary Symbol Pure-bus mode
  - HDR-TSL – Ternary Symbol Legacy-inclusive-bus mode
- MIPI I3C℠ HDR modes can be used only on:
  - Pure I3C bus – no I^2C devices present on the bus
  - Mixed Fast Bus – I^2C devices equipped with 50ns Spike Filter
- MIPI I3C℠ Bus cannot be initialized in any of HDR modes
- While in HDR mode, Repeated START and STOP are “replaced” with HDR Restart and HDR Exit patterns

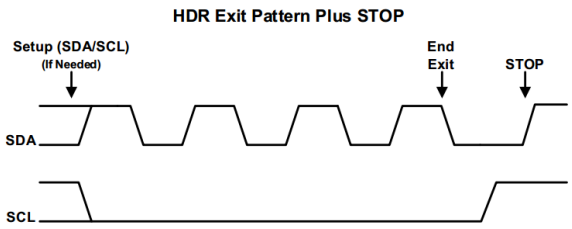
HDR Restart and HDR Exit Patterns

HDR Restart



- Separates HDR transactions
- Serves as “recovery point” in case of any error detected while in HDR mode

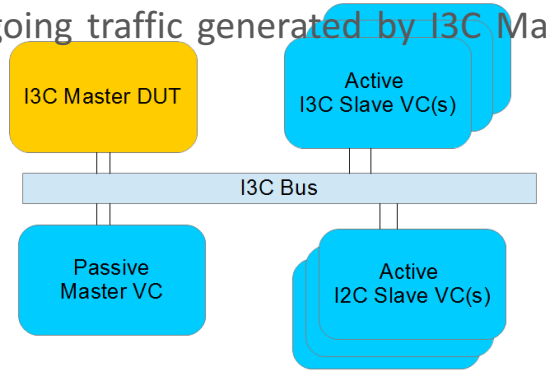
HDR Exit



- Must be detected by all I3C devices, including SDR-only devices
- Separates HDR transactions
- Serves as “recovery point” in case of HDR error detection as well as S0 and S1 error detection

Verification Environment – Master DUT

Passive Master verification component (VC) monitors outgoing traffic generated by I3C Master DUT, issues alerts about detected errors and collects coverage

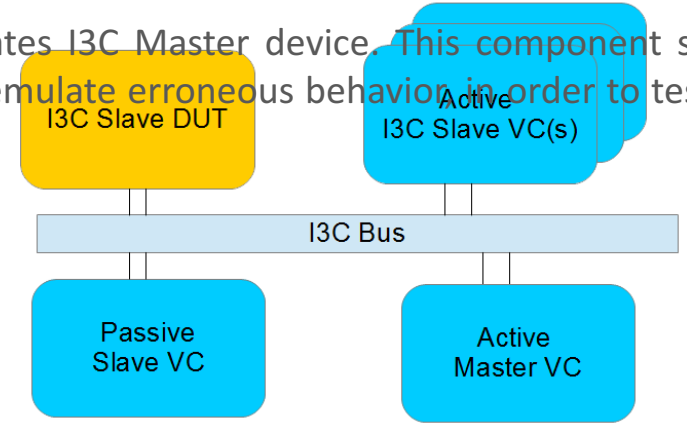


Active I3C/I²C Slave verification components emulate I3C/I²C devices present on the bus. These components should be able to emulate both proper and erroneous behavior, in order to test the ability of DUT to recover from errors in accordance with I3C spec requirements

Verification Environment – Slave DUT

Passive Slave verification component monitors outgoing traffic generated by DUT, issues alerts about detected errors and collects coverage

Active I3C Master verification component emulates I3C Master device. This component should be able to manage I3C bus. In addition it should be able to emulate erroneous behavior in order to test the DUT's error reaction capability

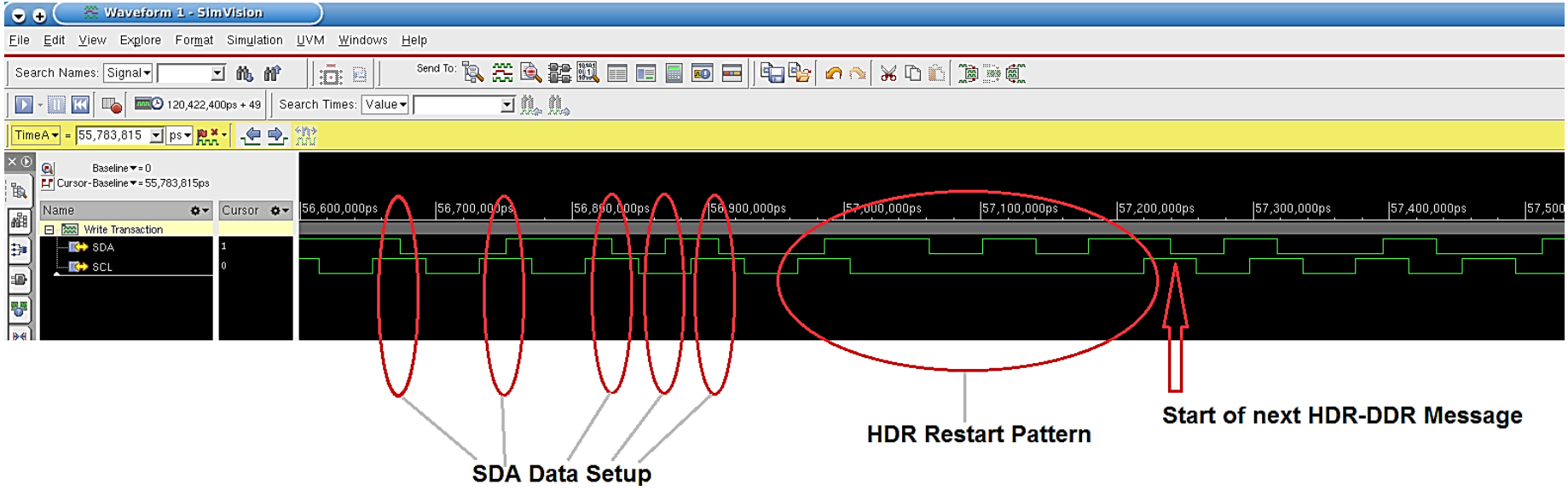


Active I3C Slave verification components emulate additional slave devices present on the bus, mostly for testing of arbitration-related aspects

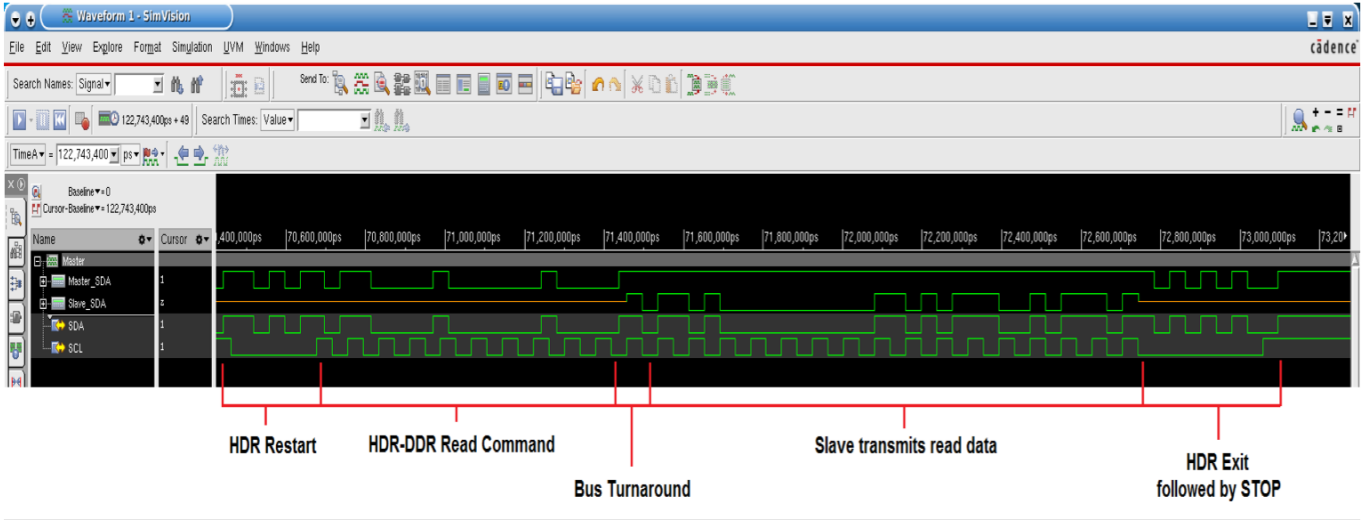
I3C HDR-DDR – Main Features

- I3C Dual Data Rate (HDR-DDR) mode allows to increase data rate up to 25 Mbps by reading data bits on both edges of SCL clock signal.
- The I3C Bus enters HDR-DDR mode upon transmission of ENTHDR0 Common Command Code and exits it when HDR Exit pattern is observed
- Data is transferred in messages that consist of Command Word, one or more Data Words and CRC Word
- Allows 128 Write commands and 64 Read commands

MIPI I3C℠ HDR-DDR Transmission



HDR-DDR Read Message



MIPI I3C℠ HDR-DDR – Main Verification Points

1. "Invisibility" of HDR-DDR traffic to I^2C devices present on the bus
2. Correct encoding and decoding of data
3. Termination of Read operation by Master
4. Error detection and recovery
5. For designs not supporting HDR-DDR – proper ignoring of all HDR-DDR traffic

Verification Scenarios for HDR-DDR

Slave DUT

1. **General Write-Read** – verifies proper operation of Slave DUT in HDR-DDR mode
2. **Read Terminated by Master** – verifies DUT ability to recognize and accept read termination by I3C Master
3. **Write with invalid preamble** – Active Master VC generates invalid Preamble in different kinds of DDR Words written to Slave DUT, in order to test DUT ability to detect, ignore and recover from erroneous transmission
4. **Write with invalid parity** - Active Master VC generates invalid parity bits in different kinds of DDR Words written to Slave DUT, in order to test DUT ability to detect, ignore and recover from erroneous transmission
5. **Write with invalid CRC5** - Active Master VC generates invalid CRC5 Word in DDR Write Message, in order to test DUT ability to detect, ignore and recover from erroneous transmission

Verification Scenarios for HDR-DDR

Master DUT

1. **General Write-Read** – verifies proper operation of Master DUT in HDR-DDR mode
2. **Read Terminated by Master** – verifies DUT ability to terminate read transaction
3. **Read with invalid preamble** – Active Slave VC generates invalid DDR Word Preamble in order to test DUT ability to detect and recover from preamble error. Invalid preamble should be generated in all types of DDR Words, e.g. Data Word and CRC Word
4. **Read with invalid parity** - Active Slave VC generates invalid parity bits in Data Word in order to test DUT ability to detect and recover from parity error. Invalid parity should be injected at both parity bit positions
5. **Read with invalid CRC5** - Active Slave VC generates invalid CRC5 Word in order to test DUT ability to detect and recover from CRC5 error

Questions?

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