mipi® DEVCON

SK Choi
Keysight Technologies

Next generation MIPI Physical Layer Design and Evaluation Challenges

2017
MIPI ALLIANCE
DEVELOPERS
CONFERENCE

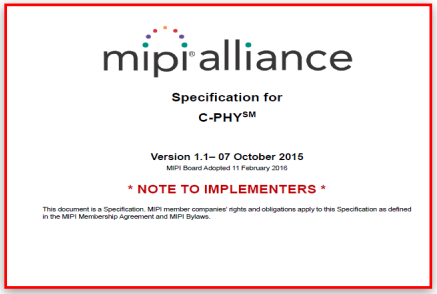
HSINCHU CITY, TAIWAN
MIPI.ORG/DEVCON

Agenda

- **New specification and CTS changes in 2017**
- Eye diagram tests changes and challenges
  - MIPI C-PHY℠
  - MIPI D-PHY℠
  - MIPI M-PHY®
- SSC test
  - MIPI D-PHY℠

KEYSIGHT TECHNOLOGIES

Specification updates in MIPI C-PHY



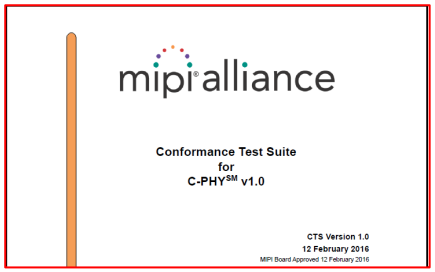
C-PHY 1.1 : Approved Feb 11, 2016

C-PHY 1.2 : Approved Mar 28, 2017

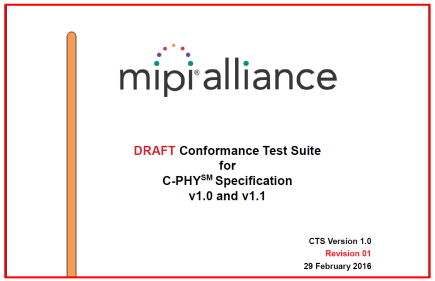
- TX Pre-Emphasis(TxEQ option) – from Pre-emphasis method to de-emphasis method
- RCLK jitter(reference clock jitter) – Annex to chapter 9
- Receiver calibration – removing PVT(Process, Voltage and Temperature variation after Long LP signal)

KEYSIGHT TECHNOLOGIES

CTS updates in MIPI C-PHY



CTS 1.0 : Approved Feb 12, 2016

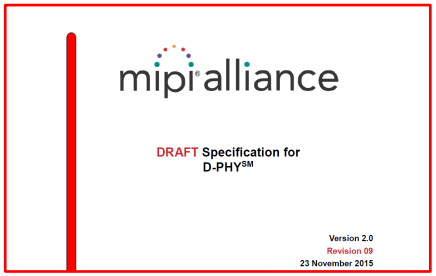


CTS 1.1 : expected approve Aug, 2017

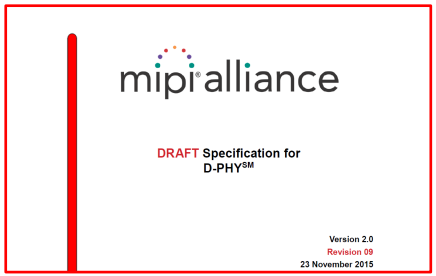
- Test 1.2.21 – Tx Eye Pattern Test
- Test 1.4.1 – HS-TX Differential Voltages Unterminated
- Test 1.4.2 – HS-TX Differential Voltage Mismatch Unterminated
- Test 1.4.3 – HS-TX Single-Ended Output High Voltages Unterminated
- Test 1.4.4 – HS-TX Static Common-Point Voltages Unterminated

KEYSIGHT TECHNOLOGIES

Specification updates in MIPI D-PHY



D-PHY 2.0 : Approved Mar 8, 2016



D-PHY 2.1 : Approved Mar 28, 2017

- Up to 6500Mbps with Short reference channel (8K support)
- Lower LP voltage level from 1.2V to 1V
- HS-Idle (lower latency)
- Programmable Preamble(RX PVT calibration due to LP signal)

KEYSIGHT TECHNOLOGIES

CTS updates in MIPI D-PHY

CTS 1.2 : April 24, 2017

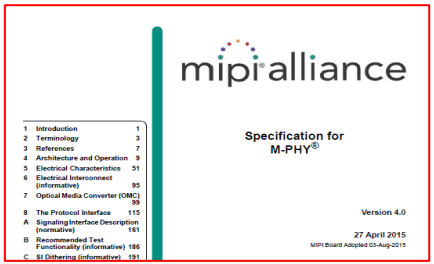
CTS v2.0/v2.1

CTS 2.0/2.1 : expected finished in October

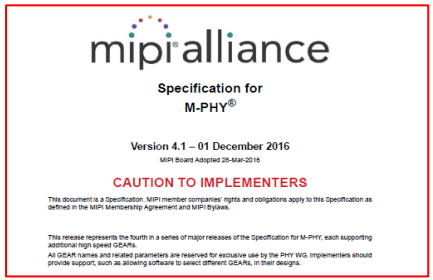
- Test 1.5.7 – HS-TX Eye Diagram
- Test 1.4.19 – TX Spread Spectrum Clocking(SSC) Requirement
- ZID open case test
- Direct connection supporting in HS continuous mode.

KEYSIGHT TECHNOLOGIES

Specification updates in MIPI M-PHY



M-PHY 4.0 : Approved Aug 3, 2015



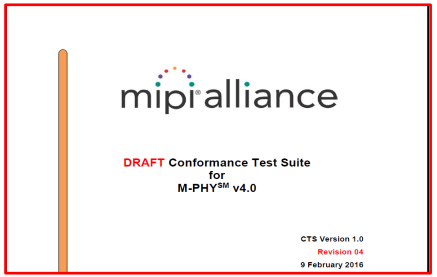
M-PHY 4. 2.1 : Approved Mar 28, 2017

- Minor spec clarification
- Target BER 10^{-10} to 10^{-12}

KEYSIGHT TECHNOLOGIES

CTS updates in MIPI M-PHY

CTS 3.1 : On-going(revision 21)



CTS 4.0/4.1 : On-going(revision 1)

- Test 1.1.7 – HS-TX G3 and G4 Differential AC Eye (TEYE-HS-G3/G4-TX, VDIF-AC-HS-G3/G4-TX)

KEYSIGHT TECHNOLOGIES

Agenda

- New specification and CTS changes in 2017
- **Eye diagram tests changes and challenges**
  - **MIPI C-PHY℠**
  - **MIPI D-PHY℠**
  - **MIPI M-PHY®**
- SSC test
  - MIPI D-PHY℠

KEYSIGHT TECHNOLOGIES

Eye Diagram Test - General

Eye diagram

MIPI C-PHY

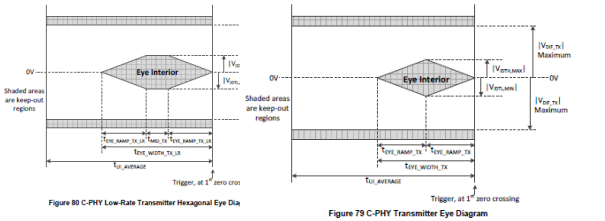


Figure 80 C-PHY Low-Rate Transmitter Hexagonal Eye Dia

Figure 79 C-PHY Transmitter Eye Diagram

MIPI D-PHY

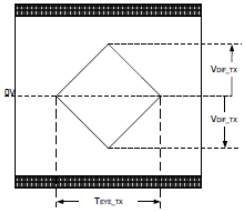


Figure 65 TX Eye Diagram Specification

MIPI M-PHY

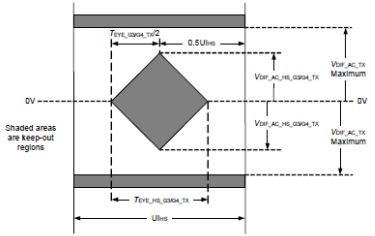
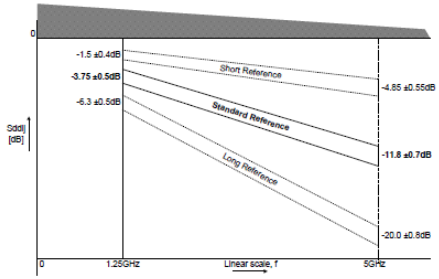


Figure 38 HS-G3 and HS-G4 Differential Transmitter Eye Diagram

Refence channel



Frequency	1.25GHz	5.0GHz
Short Reference Sddij, dB	-1.5dB ±0.4dB	-4.85dB ±0.55dB
Standard Reference Sddij, dB	-3.75dB ±0.5dB	-11.8dB ±0.7dB
Long Reference Sddij, dB	-6.3dB ±0.5dB	-20.0dB ±0.8dB

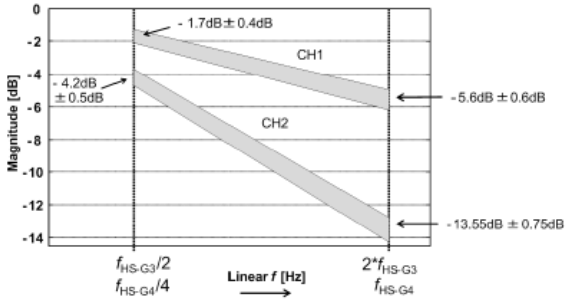


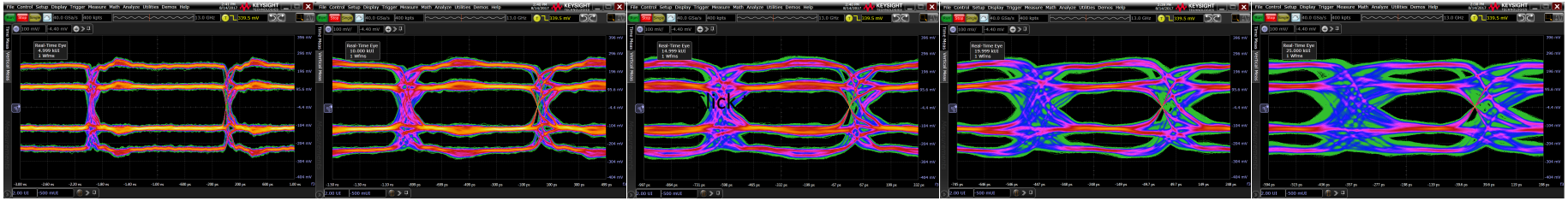
Figure 26 HS-G3 and HS-G4 Reference Channel Insertion Loss $SDD_{IL\ REF\ CH}$ Templates

KEYSIGHT TECHNOLOGIES

Eye Diagram Test Challenges for MIPI C-PHY/D-PHY

- RTB(Reference Termination Board) can't support new specifications

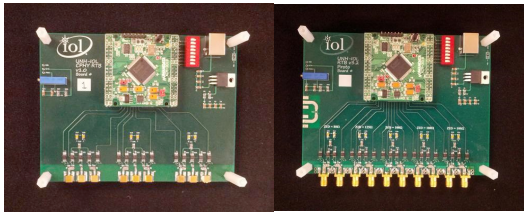
sps : Symbol Per Second



500Msps | 1Gsps | 1.5Gsps | 2.0Gsps | 2.5Gsps

Same data, +/-250mV HS swing, 82ps R/F time, without reference channel
However, eye diagram is distorted

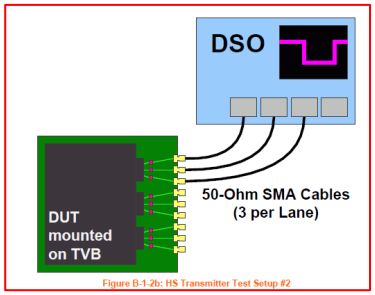
KEYSIGHT TECHNOLOGIES



MIPI C-PHY RTB | MIPI D-PHY RTB

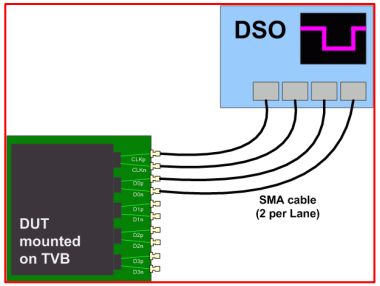
MIPI C-PHY/D-PHY Eye Diagram Test

MIPI C-PHY



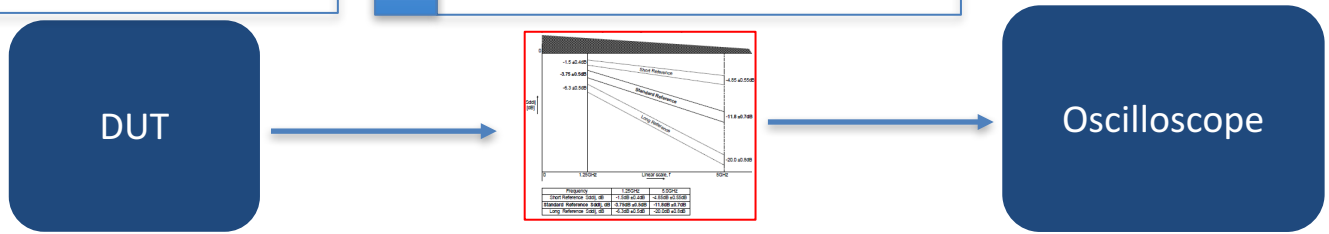
Setup 2
Direct connection to scope(HS only)

MIPI D-PHY



TX HS Test Setup 2
Direct connection to oscilloscope
(HS, 100ohm termination only)

- Now, PHY WG defines direct connection to oscilloscope
- However, RTB is still required for LP to HS timing test.

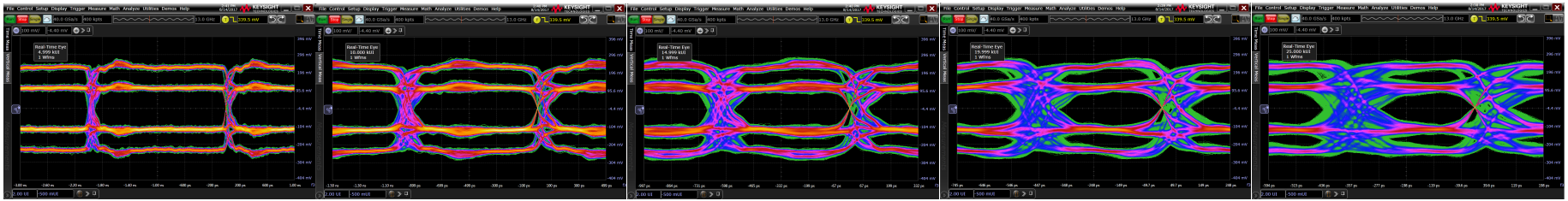


KEYSIGHT TECHNOLOGIES

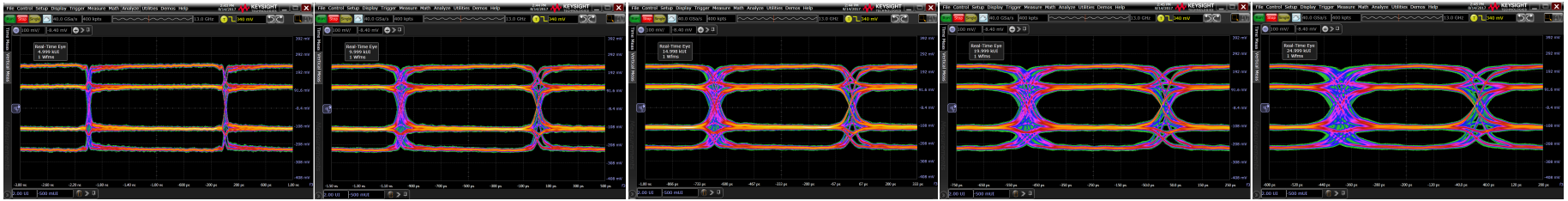
Resolving Issue with Direct Connection

- Direct connection provide more accurate result on tests

sps : Symbol Per Second



500Msps | 1Gsps | 1.5Gsps | 2.0Gsps | 2.5Gsps



Same data, +/-250mV HS swing, 82ps R/F time, without reference channel

KEYSIGHT TECHNOLOGIES

Chip Design Tip for Testing

- New MIPI C-PHY v1.1 and D-PHY v2.0 or above require to send both Burst mode and Continuous mode signal on testing, so it is good to consider to implement both mode for easy testing.
- If not, it is not easy to get right test result.

C-PHY CTS Annex B

Notes on the above Test Setup #2:

- The DUT is connected to the DSO using three high-bandwidth, low loss 50-ohm coaxial cables.
- For tests where a reference channel is required, it can either be a physical channel or be implemented in software on the oscilloscope.
- Each cable measures the single-ended V_A, V_B, or V_C signal with respect to PCB ground.
- The DSO serves as the termination, and is designed to have a resistive termination ($Z_{ID}/2$) value of 50 ohms per line, for all lines. The DSO input coupling and/or termination voltage must be set appropriately for this configuration.
- The DUT should be configured to transmit a continuous stream of HS data, because this test setup is suitable for measurements only in the HS mode of operation.
- The DSO vertical gain should be optimized so that the DUT signaling spans as much of the vertical height of the screen as possible.

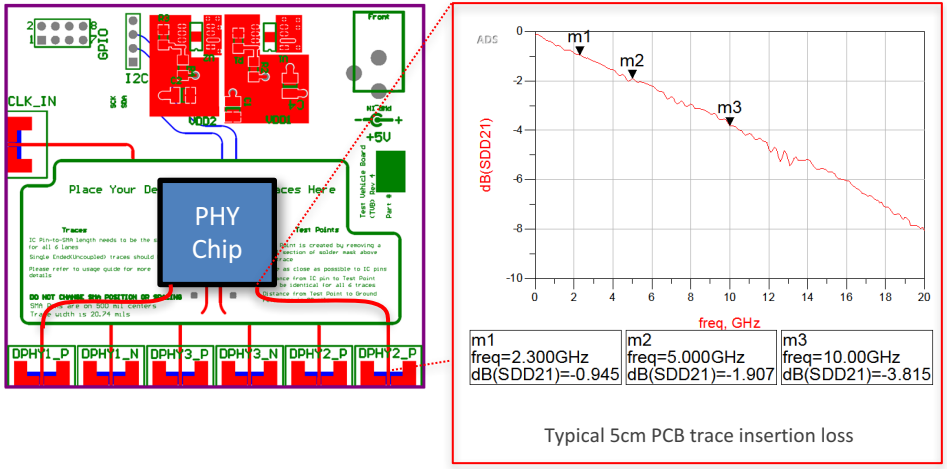
D-PHY CTS Annex B

Note on the above test setup #2:

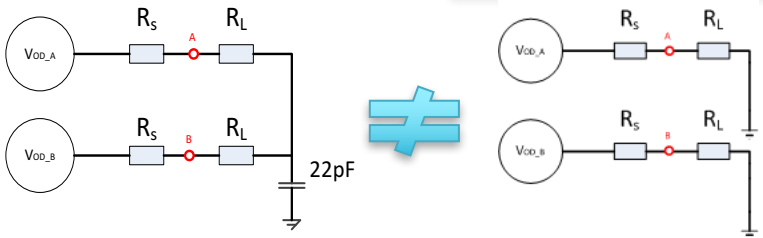
- The DUT is connected to the DSO using high-bandwidth, low loss 50Ω SMA cables
- For tests where a reference channel is required, it can either be a physical channel or be implemented in software on the oscilloscope.
- Each cable connected to single-ended + or – signal with respect to PCB ground.
- The DSO serves as the termination, and is designed to have a resistive termination(ZID/2) value of 50Ω per line, for all lines. The DSO input coupling and/or termination voltage must be set appropriately to emulate 100Ω termination in real D-PHY.
- The DUT should be configured to transmit a continuous stream of HS data only, because this test setup is suitable for measurements in HS mode of operation with only 100Ω termination emulation.
- The DSO vertical gain should be optimized so that the DUT signaling spans as much of the vertical height of the screen as possible.

KEYSIGHT TECHNOLOGIES

Test Setup Tip 1



Typical 5cm PCB trace insertion loss



- Prepare Test Fixture (TVB) with short routing to connector to reducing fixture line loss (5cm or less) or extract S-parameter of fixture trace when design TVB
- To emulate 100ohm termination in MIPI PHY, please use external voltage sourced scope or probe to compensate common mode voltage drop and double current consumption

KEYSIGHT TECHNOLOGIES

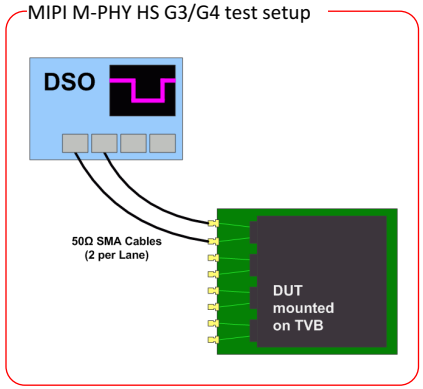
Test Setup Tip 2

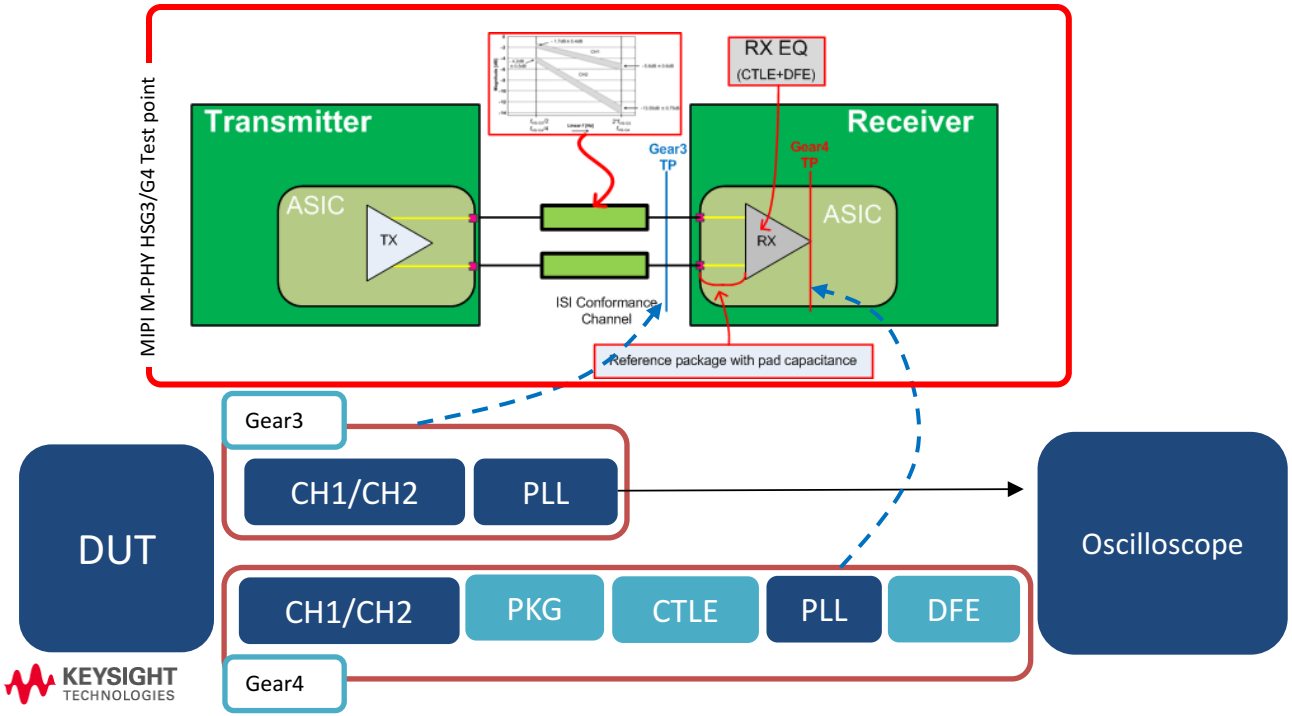
- Use hardware or software channel for eye diagram test, all oscilloscope vender provide easy tool for software channel embedding, using S-parameter file.
- For C-PHY and D-PHY, it requires more than 2 lines of channel so software embedding provide more price merit than real hardware channel, also convenient to test

KEYSIGHT TECHNOLOGIES

MIPI M-PHY Eye Diagram Test

- Test setup is same on both HSG3 and HSG4 but testing points has changed.





MIPI M-PHY Embedding Channel + Package Model

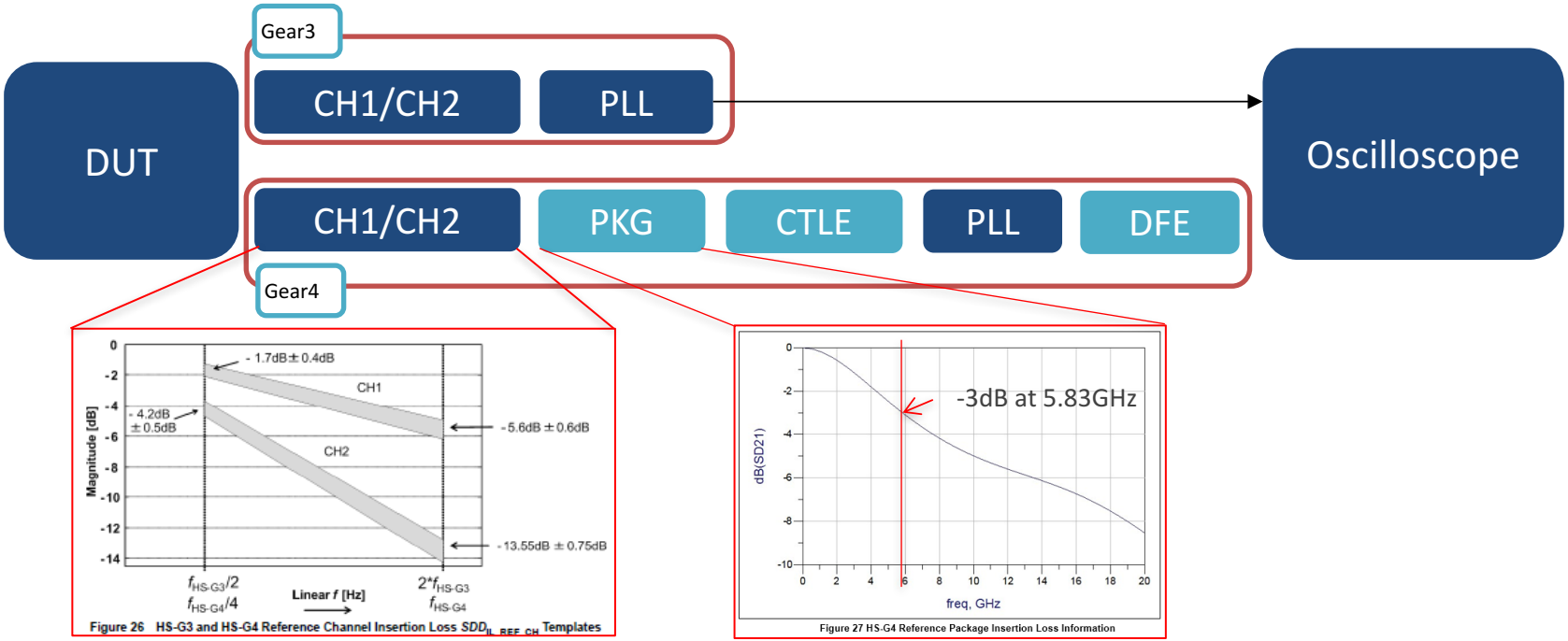


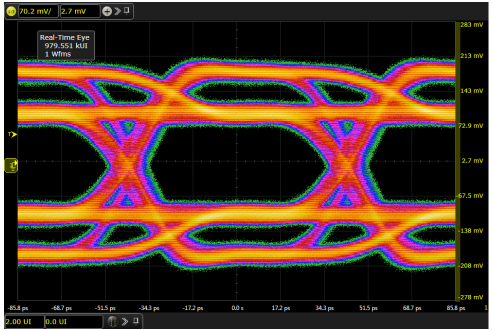
Figure 26 HS-G3 and HS-G4 Reference Channel Insertion Loss $SDD_{IL\_REF\_CH}$ Templates

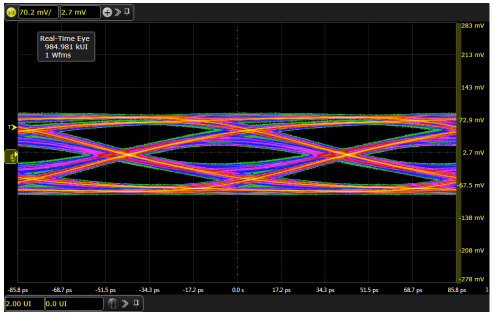
Figure 27 HS-G4 Reference Package Insertion Loss Information

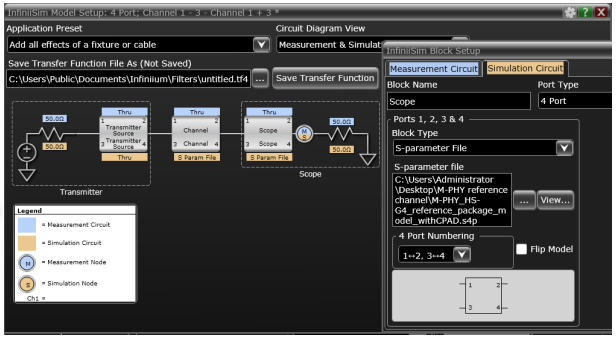
KEYSIGHT TECHNOLOGIES

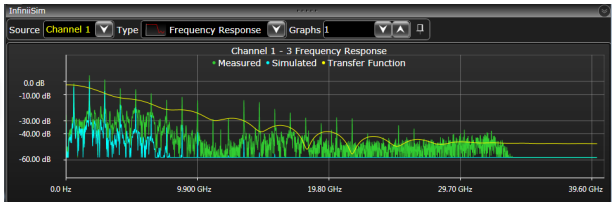
Keysight

Test Setup Tip 3 – and Must for HS Gear4









- Reference package plus pad capacitance model is not real material for using, so it is hard to emulate with real PCB or another circuit, so MIPI WG recommends using software embedding function for embedding reference package plus pad capacitance model

KEYSIGHT TECHNOLOGIES

MIPI M-PHY RX Equalizer-CTLE

- Not likely another application, M-PHY CTLE has vary wide range of zero pole value and Adc value

HS-RX Reference Equalizer					
A_{AC}			6	dB	CTLE AC gain
A_{DC}	-4		6	dB	CTLE DC gain
f_Z[1]	0.4		1.2	GHz	CTLE zero frequency
f_{P2}			10	GHz	CTLE second pole frequency
V_{DFE_RX}	-60		60	mV	DFE feedback voltage signal

1. f_{P1} is determined by other parameters: $f_{P1} = f_Z * 10^{((A_{AC} - A_{DC})/20)}$

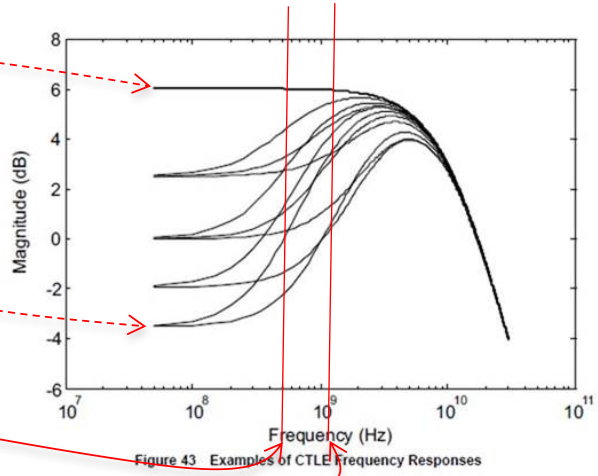


Figure 43 Examples of CTLE Frequency Responses

What if A company think 2.5dB Adc + 400MHz Fz is optimal CTLE value

B company think 0dB Adc + 400MHz Fz is optimal CTLE value?

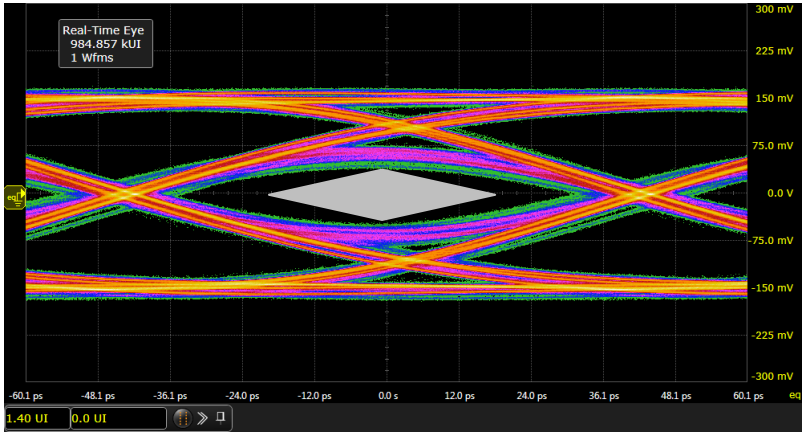
Does it correlated between?

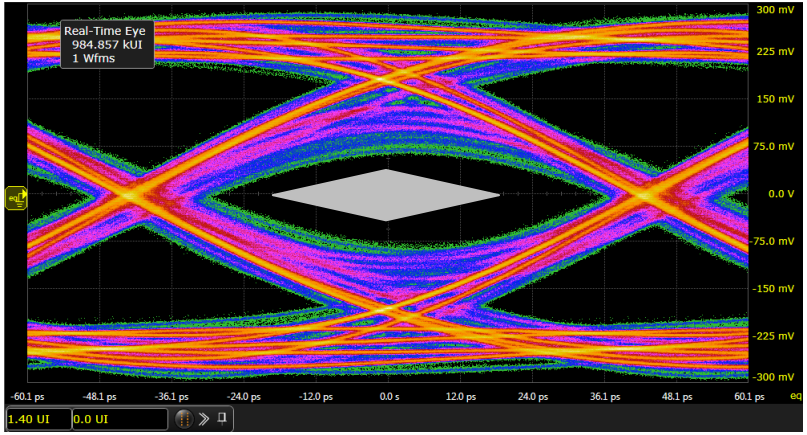
KEYSIGHT TECHNOLOGIES

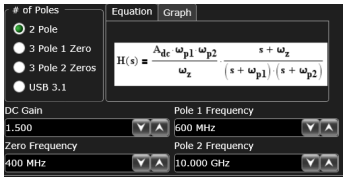
MIPI M-PHY RX Equalizer-CTLE

Same waveform but only change Adc value from 2.5dB to 0dB

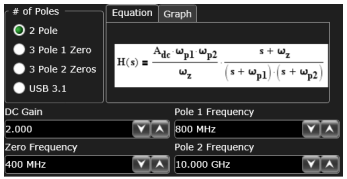
Adc : CTLE DC gain
Fz : CTLE zero frequency







2.5dB Adc case
Fz = 400MHz

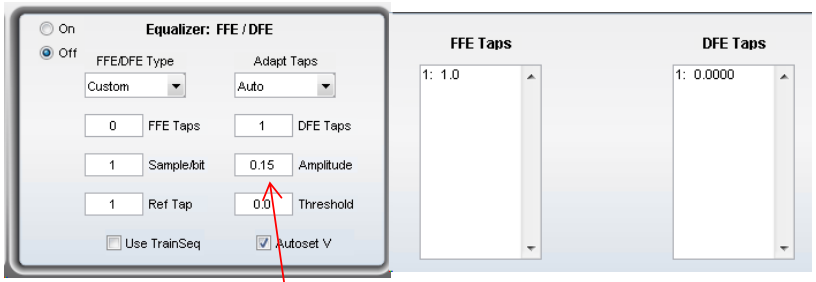


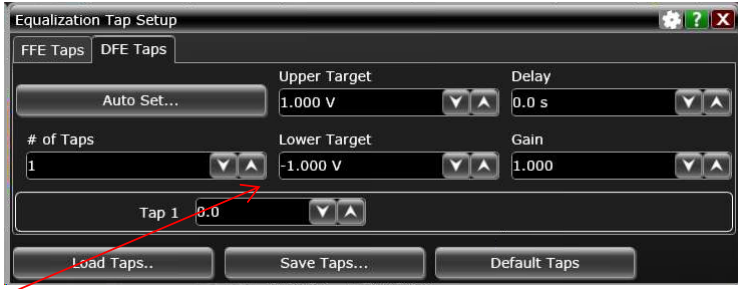
0dB Adc case
Fz = 400MHz

KEYSIGHT TECHNOLOGIES

MIPI M-PHY RX Equalizer-DFE

Also Oscilloscope's DFE setting is not favor to the customer.





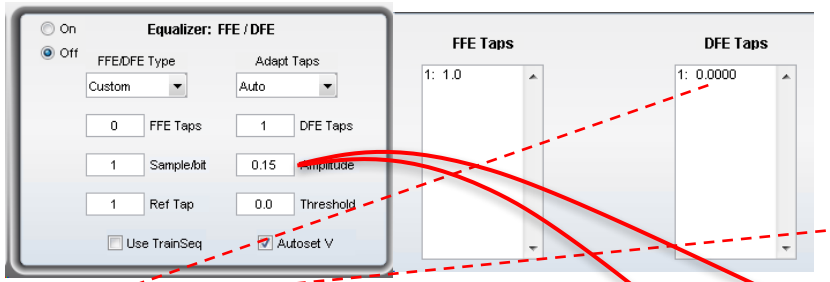
HS-RX Reference Equalizer					
A_{AC}			6	dB	CTLE AC gain
A_{DC}	-4		6	dB	CTLE DC gain
f_Z[1]	0.4		1.2	GHz	CTLE zero frequency
f_{P2}			10	GHz	CTLE second pole frequency
V_{DFE_RX}	-60		60	mV	DFE feedback voltage signal

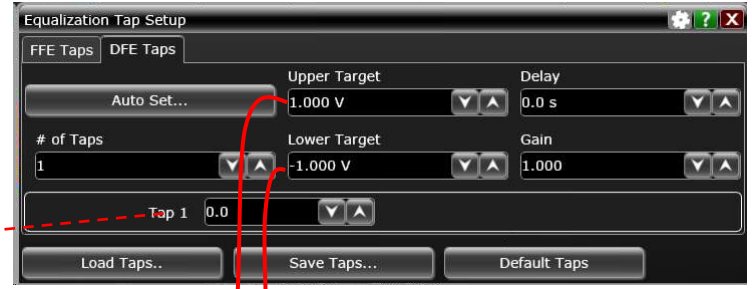
1. f_{P1} is determined by other parameters: $f_{P1} = f_Z * 10^{((A_{AC} - A_{DC})/20)}$

KEYSIGHT TECHNOLOGIES

MIPI M-PHY RX Equalizer-DFE

Also Oscilloscope's DFE setting is not favor to the customer.

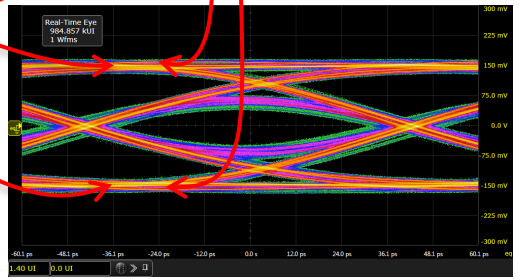




Tap = V_{DFE_RX}/Amplitude

HS-RX Reference Equalizer					
A_{AC}			6	dB	CTLE AC gain
A_{DC}	-4		6	dB	CTLE DC gain
f_Z[1]	0.4		1.2	GHz	CTLE zero frequency
f_{P2}			10	GHz	CTLE second pole frequency
V_{DFE_RX}	-60		60	mV	DFE feedback voltage signal

1. f_{P1} is determined by other parameters: $f_{P1} = f_Z * 10^{((A_{AC} - A_{DC})/20)}$



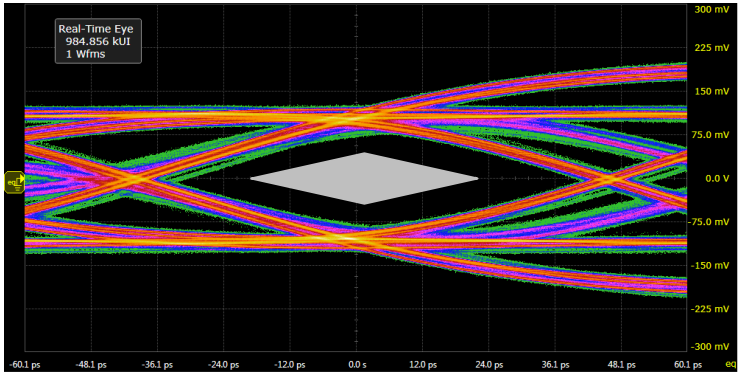
Amplitude or upper/lower target is voltage value after CTLE applied. Not direct V_{DEF_RX} value

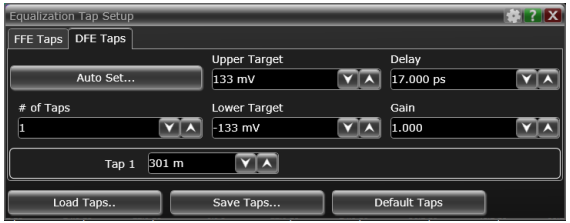
KEYSIGHT TECHNOLOGIES

MIPI M-PHY RX Equalizer-DFE

V_{DEF_RX} : DFE feedback voltage signal

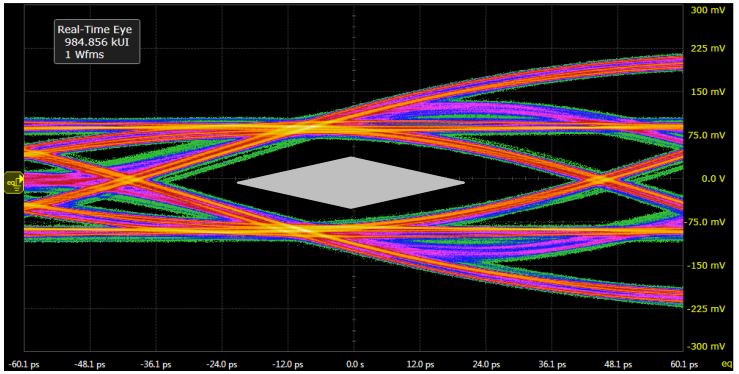
40mV V_{DEF_RX}

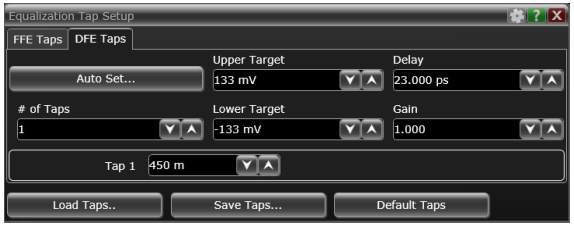




40mV/133mV
=0.30075

60mV V_{DEF_RX}

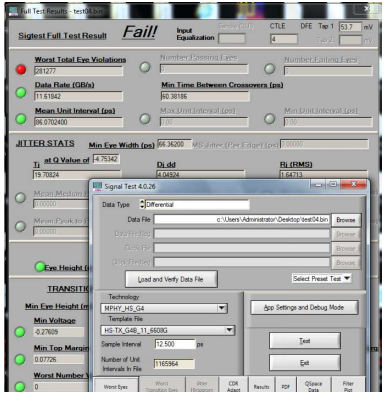




60mV/133mV
=0.45112

KEYSIGHT TECHNOLOGIES

Test Setup Tip 4

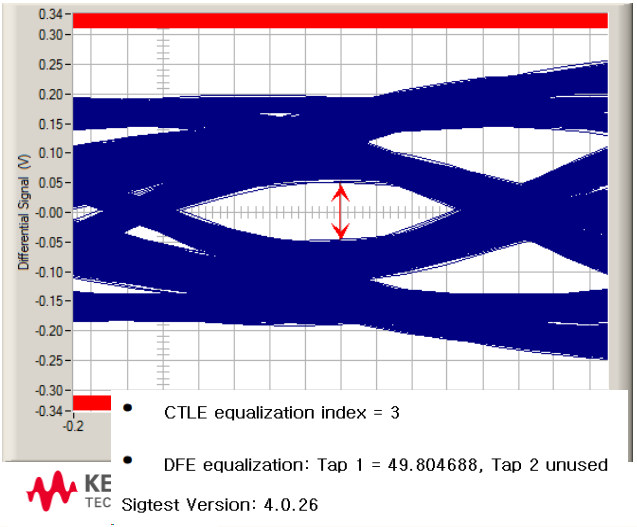


Use SigTest tool

Commonly used for High speed digital interface
- USB
- PCIe

Provide similar result between oscilloscopes

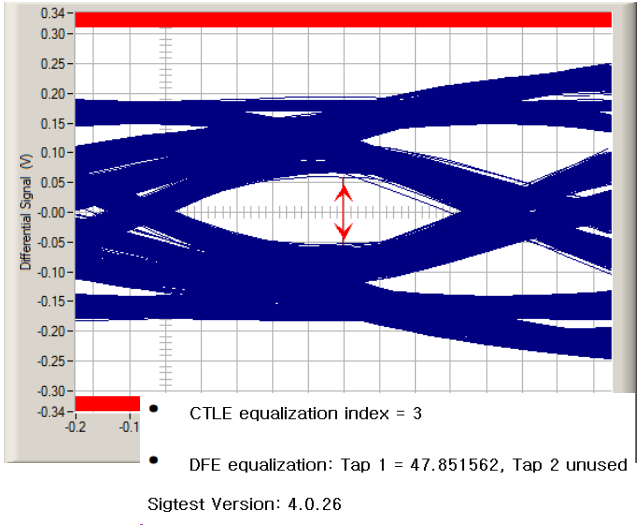
A company



- CTLE equalization index = 3
- DFE equalization: Tap 1 = 49.804688, Tap 2 unused

Sigtest Version: 4.0.26

B company



- CTLE equalization index = 3
- DFE equalization: Tap 1 = 47.851562, Tap 2 unused

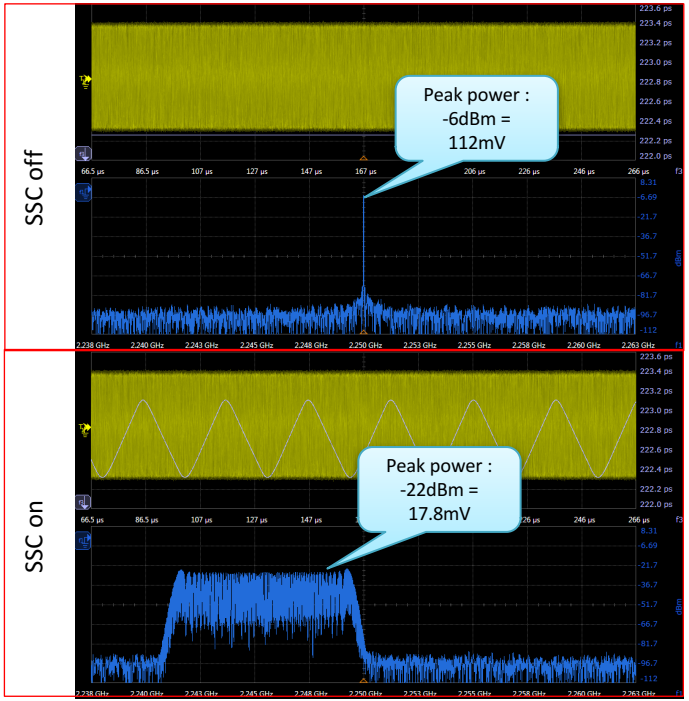
Sigtest Version: 4.0.26

Agenda

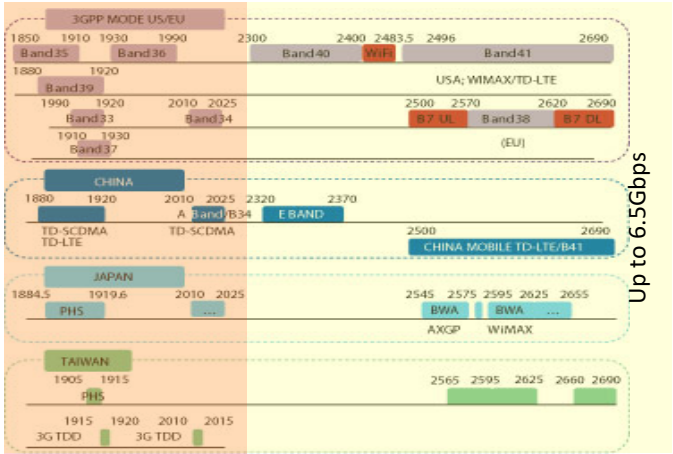
- New specification and CTS changes in 2017
- Eye diagram tests changes and challenges
  - MIPI C-PHY℠
  - MIPI D-PHY℠
  - MIPI M-PHY®
- **SSC test**
  - **MIPI D-PHY℠**

KEYSIGHT TECHNOLOGIES

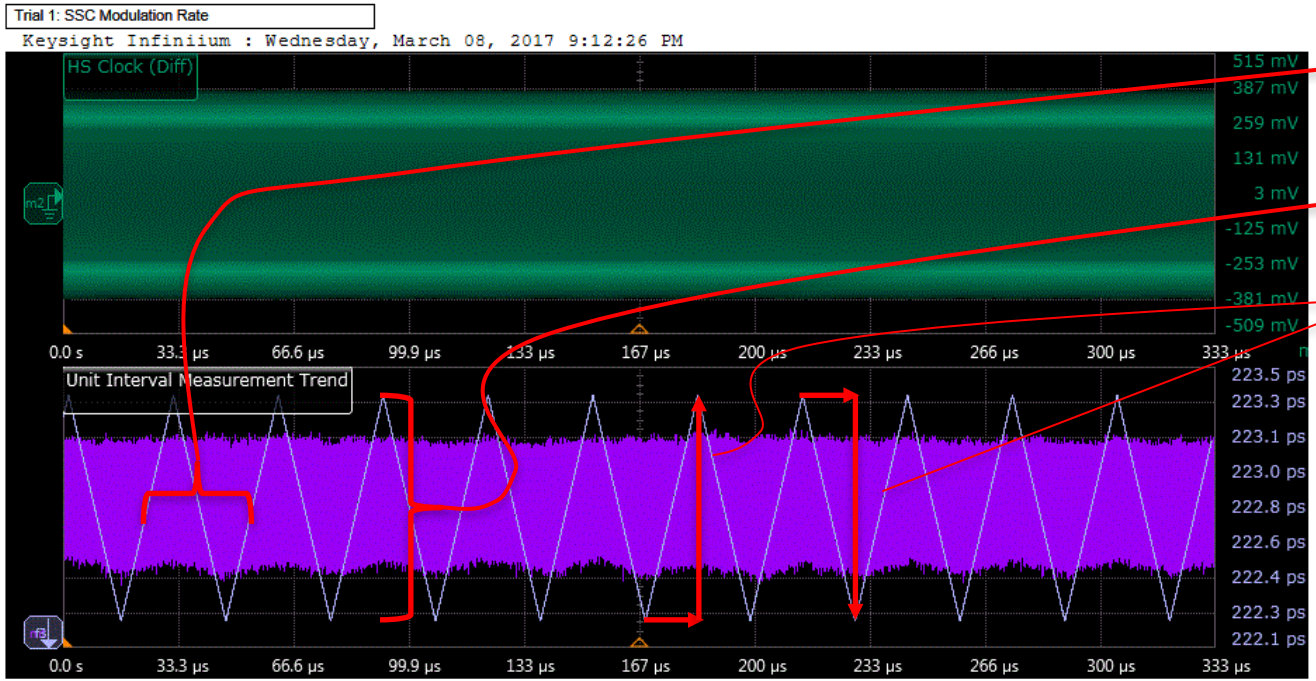
SSC (Spread Spectrum Clocking) - General



- SSC makes distribution of RF power on signal so that it can reduce interruption to another signals like wireless signal.
- Now MIPI D-PHY fundamental frequency is over 2GHz bandwidth, where lots of wireless signals have used.
- Because of Clock line in MIPI D-PHY, SSC feature is required.



SSC (Spread Spectrum Clocking) Test in MIPI D-PHY



SSC modulation frequency

SSC modulation deviation

SSC df/dt

KEYSIGHT TECHNOLOGIES

SSC in MIPI D-PHY Specification

1276

Table 39 Spread Spectrum Clocking Requirements

Parameter	Symbol	Min	Max	Units	Notes
Modulation Rate	$T_{SSC\_MOD\_RATE}$	30	33	kHz	
SSC Deviation	$T_{SSC\_FREQ\_DEV}$	-5000	0	PPM	1, 2
SSC df/dt	$SSC_{df/dt}$	N/A	1250	PPM/µs	3, 4, 5

Requirements

Note:

1. *The required SSC deviation is also called "Down-Spread".*
2. *Any implementation with an SSC deviation significantly smaller than 5000 PPM may fail in EMI testing below 1 GHz clock rate (Data Rate < 2 Gbps).*
3. *df/dt limit shall be for clock and all data lanes.*
4. *Measured over a 0.5 µs interval using an alternating 010101010… input pattern at highest data rate. The measurements shall be low pass filtered using a filter with 3 dB cutoff frequency that is 60 times the modulation rate. The filter stopband rejection shall be a second order low-pass of 40 dB per decade. Evaluation of the maximum df/dt is achieved by inspection of the low-pass filtered waveform.*
5. *Maximum change rate of 1250 PPM/µs is limiting the absolute value of the df/dt.*

KEYSIGHT TECHNOLOGIES

Chip Design Tip for Testing

- For SSC (spread spectrum clocking), Designer must implement Chip can enable and disable SSC transmission.

10.2.2 Normative Spread Spectrum Clocking (SSC)

Spread Spectrum Clocking (sometimes referred to as "Spectrum Spread Clocking") is a common technique where a low frequency modulation is added to the Transmitter's clock to reduce the peak emissions.

All Transmitters conformant to D-PHY v2.0 and above shall support SSC as per ***Table 39*** for data rates operating above 2.5 Gbps.

All Receivers conformant to D-PHY v2.0 and above shall support SSC as per ***Table 39*** for data rates operating above 2.5 Gbps.

All Transmitters conformant to D-PHY v2.0 and above shall provide the system integrator with a mechanism to enable/disable SSC transmissions.

SSC can be used in HS Data Transmission Mode. If used during HS Data Transmission Mode, SSC transmission shall be consistent during the entire mode.

SSC should not be used in Escape mode.

SSC shall be implemented within the Transmitter such that a single modulated profile, single modulation rate and a single SSC deviation is common between the clock and all High-speed data lanes.

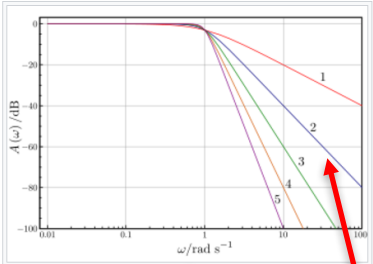
All SSC parameters are defined for the HS Clock.

KEYSIGHT TECHNOLOGIES

Test Setup Tip 5

Use 2nd order Butterworth filter to meet SSC df/dt test condition

Transfer function [edit]



Plot of the gain of Butterworth low-pass filters of orders 1 through 5, with cutoff frequency $\omega_0 = 1$. Note that the slope is $20n$ dB/decade where n is the filter order.

Like all filters, the typical prototype is the low-pass filter, which can be modified into a high-pass filter, or placed in series with others to form band-pass and band-stop filters, and higher order versions of these.

The gain $G(\omega)$ of an n-order Butterworth low pass filter is given in terms of the transfer function $H(s)$ as

$$G^2(\omega) = |H(j\omega)|^2 = \frac{{G_0}^2}{1 + \left(\frac{j\omega}{j\omega_c}\right)^{2n}}$$

where

- n = order of filter
- ω_c = cutoff frequency (approximately the -3dB frequency)
- G_0 is the DC gain (gain at zero frequency)

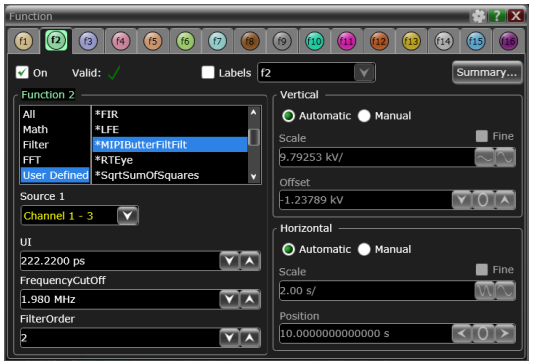
It can be seen that as n approaches infinity, the gain becomes a rectangle function and frequencies below ω_c will be passed with gain G_0, while frequencies above ω_c will be suppressed. For smaller values of n, the cutoff will be less sharp.

Source : Wikipedia

2nd order Butterworth filter
= 40dB/decade

ω0 = cutoff frequency

- Some of Digital oscilloscope are possible to use Matlab code in the oscilloscope itself so that Matlab can apply complicated filter function.



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