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MIPI I3CSM Interface – Advanced Features

2017

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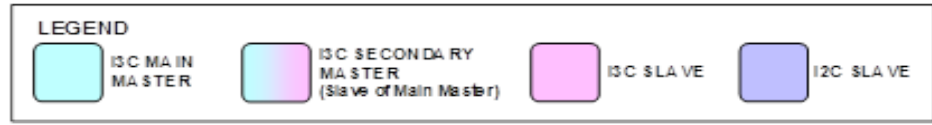
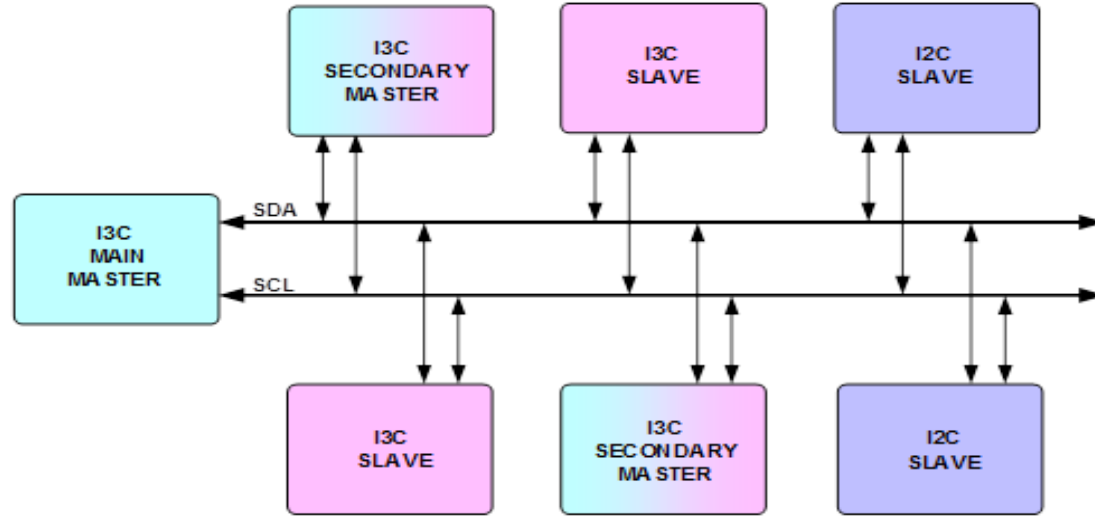
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Outline

- MIPI I3CSM – intelligent multifeatured interface
- List of main bus management procedures
- Timing Control
 - Problems solved, Challenges, Practical implementation aspects
- Elements of flow control
 - Problems solved, Challenges, Practical implementation aspects

MIPI I3CSM Bus Clients



MIPI I3CSM – Intelligent Multifeatured Interface

- MIPI I3CSM supports several communication formats, all sharing a two-wire interface.
 - The two wires are designated SDA and SCL:
 - SDA (Serial Data) is a bidirectional data pin
 - SCL (Serial Clock) can be either a clock pin or a data pin while in certain HDR Modes
- An MIPI I3CSM Bus supports the mixing of various Message types:
 - I²C-like SDR Messages, with SCL clock speeds up to 12.5MHz
 - Broadcast and Direct Common Command Code (CCC) Messages that allow the Master to communicate to all or one of the Slaves on the I3C Bus, respectively
 - HDR Mode Messages, which achieve higher data rates per equivalent clock cycle
 - I²C Messages to Legacy I²C Slaves
 - Slave-initiated requests to the Master, for example for In-Band Interrupt or to request the Master role

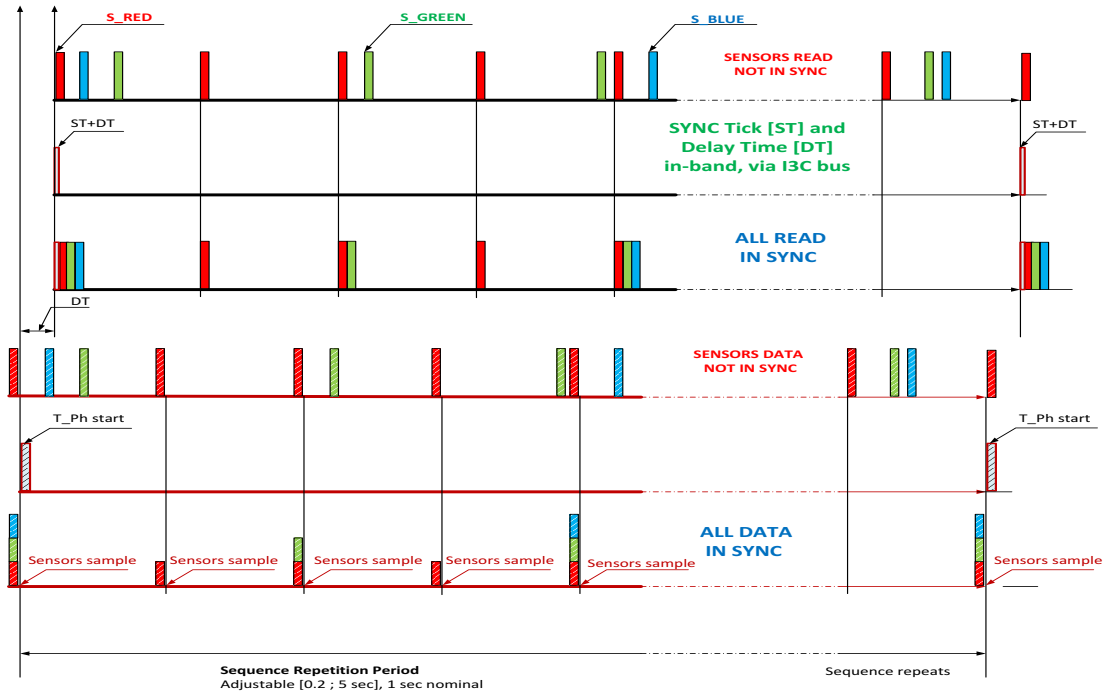
MIPI I3CSM BUS Management Features

- Dynamic Address Assignment
- Hot-Join
- In-Band Interrupt
- Secondary Master
- In-Band Hard RESET
- Timing Control
- Common Command Codes
- Error detection and Recovery
- Elements of Flow Control

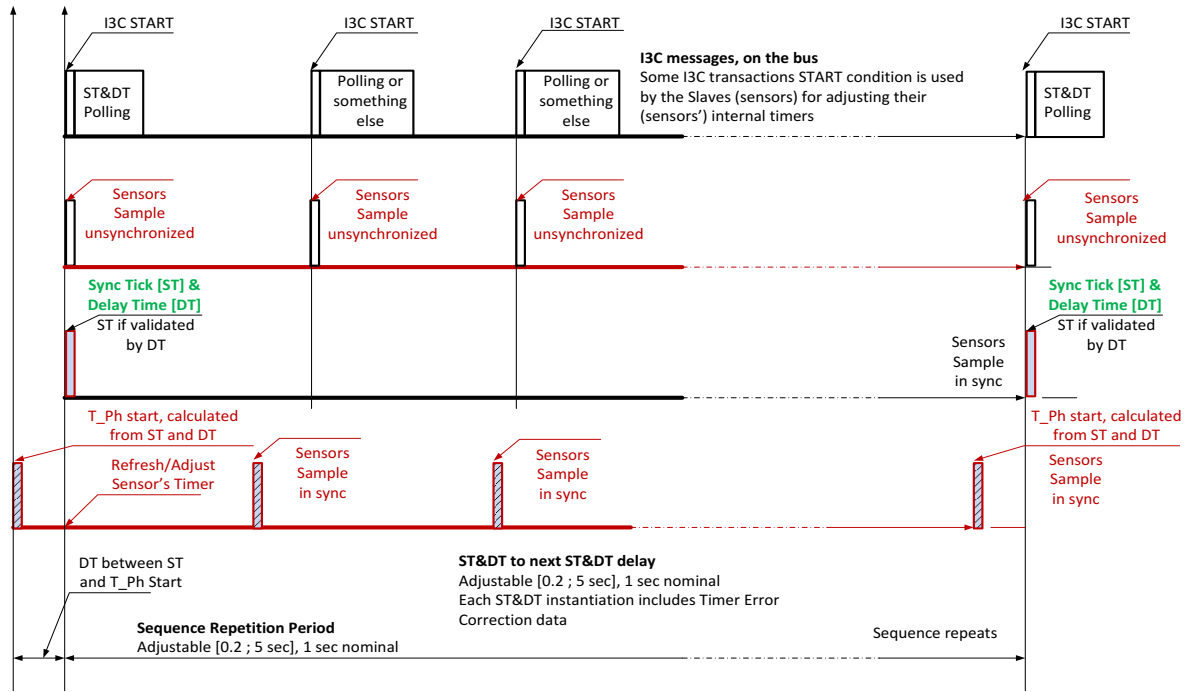
Timing Control

- Complex applications require several Sensors on a common timeline
- Synchronous Systems and Events
 - Controlling the sampling moments has the potential of drastically reducing the system energy expenditure
- Asynchronous Systems and Events
 - The accuracy of the timestamps of events matters
- The Synchronous and Asynchronous modes can be used independently and concurrently on the same bus and devices

Synchronous Systems and Events



Synchronous – Multiple Transactions



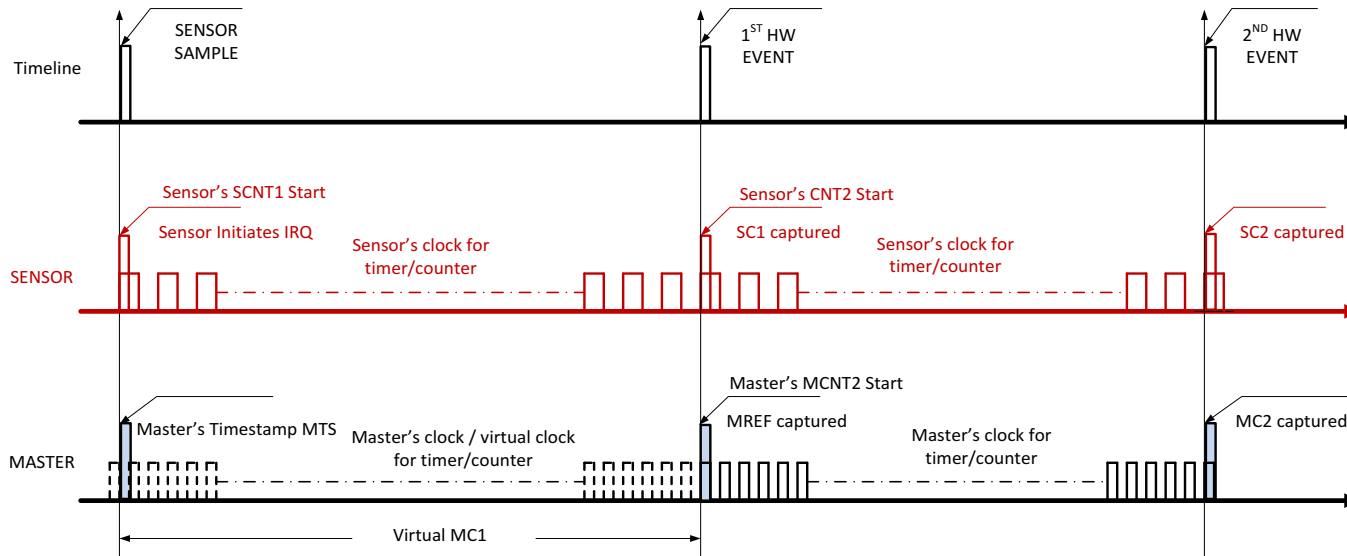
Synchronous – Common Command Codes

- SETXTIME CCC
- Configuration messages
 - ODR (Output Data Rate)
 - TPH (Procedure Repetition Time)
 - TU (Time Unit)
- Run Time messages
 - SYNC Tick [ST]
 - Delay Time [DT]

Asynchronous Systems and Events

- Four Async Modes
 - Basic – Async Mode 0
 - Enhanced – Async Mode 1, 2 and 3
- SETXTIME is the CCC
 - The defining byte selects the running mode

Async 0 Time Diagram



$$MTS = MREF - MC2 \times SC1 / SC2$$

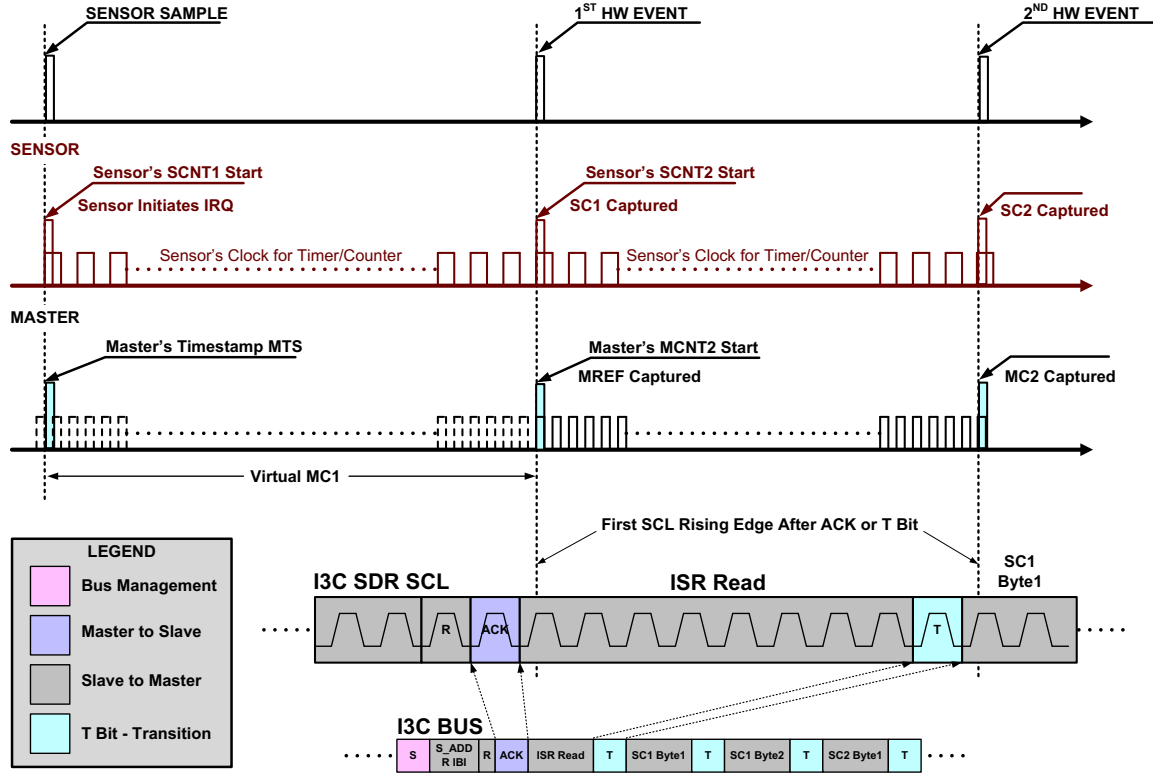
MTS – Master Timestamp, expressed in MASTER's time units

MREF – Master Reference, i.e. Start of Master's secondary counter, MCNT2

MC1, MC2 – Master's counters values, captured at the corresponding HWSE events.

SC1, SC2 – Slave's counters values, captured at the corresponding HWSE events.

Async 0 on SDR



Elements of Flow Control

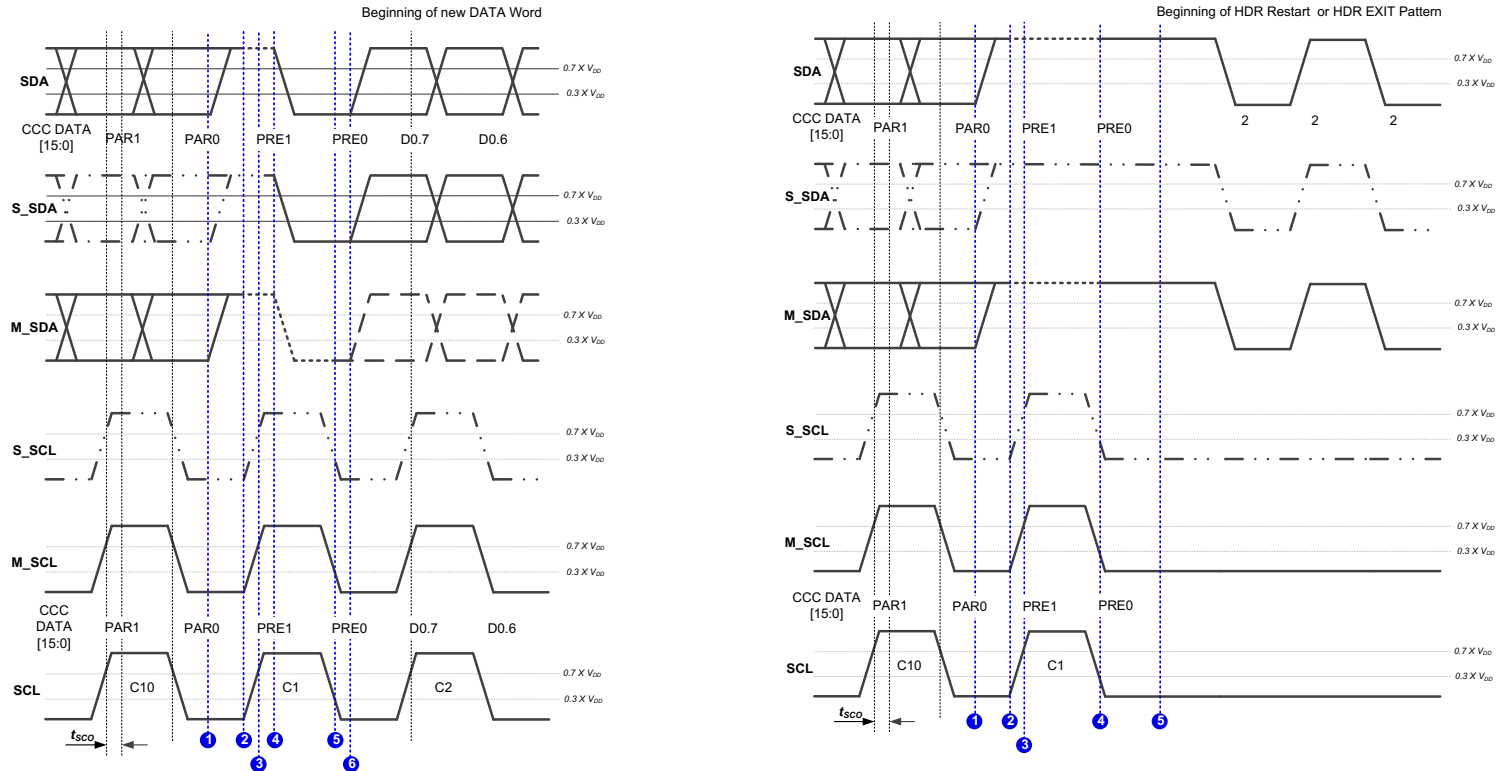
- The Transmitter drives actively the data lines
 - SDA on HDR-DDR
 - SDA and SCL on HDR-TSx
- The Receiver might need to end the transaction
 - The bus needs to provide the opportunity for the Receiver to change the state of a line, in a pre-established way

HDR-DDR Transactions

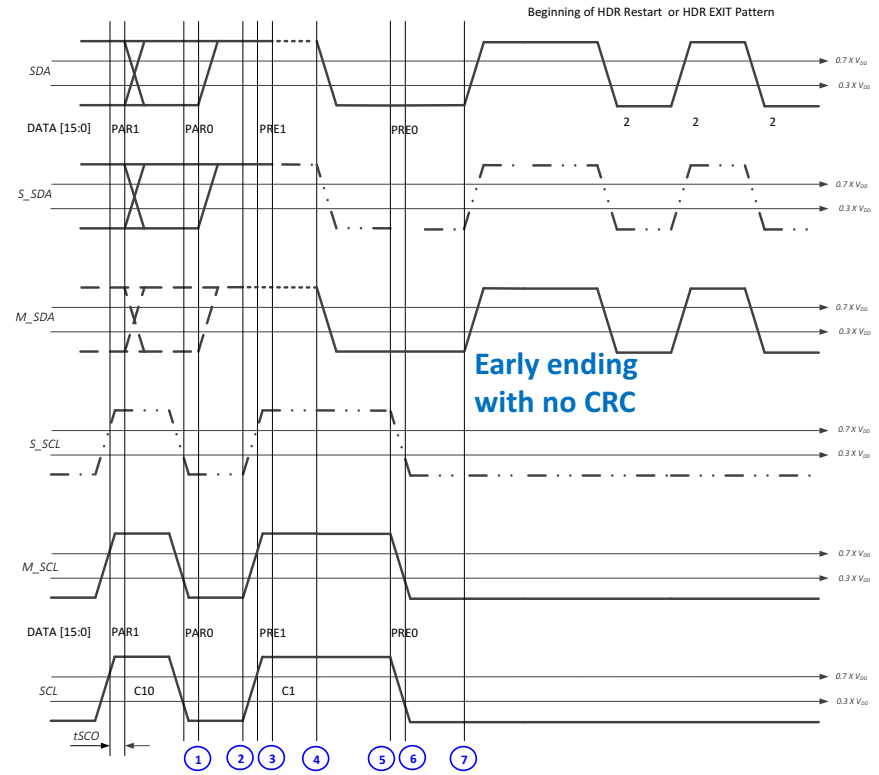
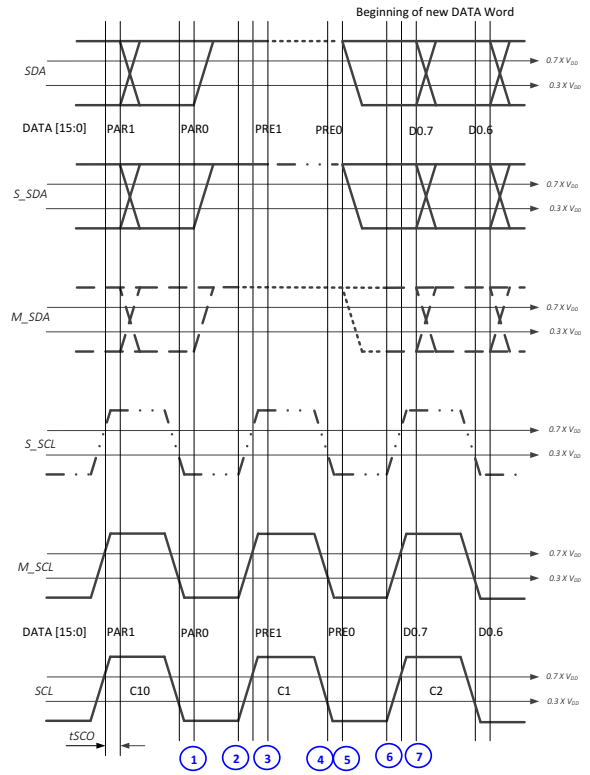
HDR-DDR Preamble Values

Context	Preamble Value and Interpretation			
	2'b00	2'b01	2'b10	2'b11
After EnterHDR	Reserved for Future Use	Command Word follows	-	-
After Read CMD		-	Slave ACK, Data follows	Slave NACK, Aborted
After Read DATA		CRC Word follows	Master Aborts, Slave yields. Master drives second 0.	Data follows. Master does not drive second bit.
After Write CMD		-	Data follows	-
After Write DATA		CRC Word follows	-	Data follows

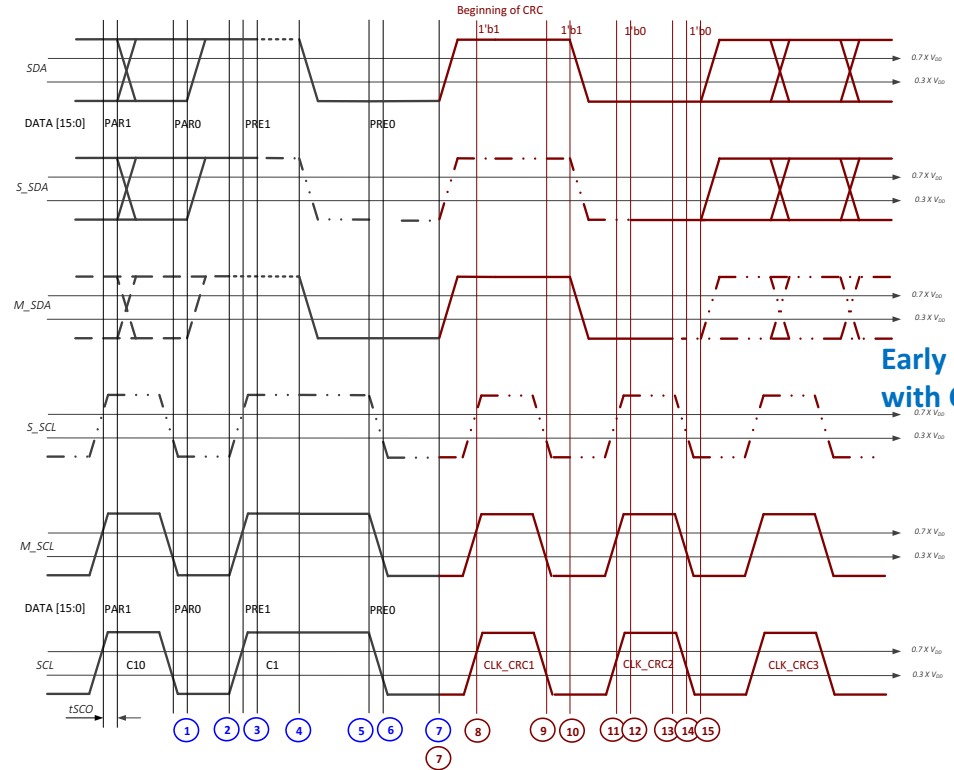
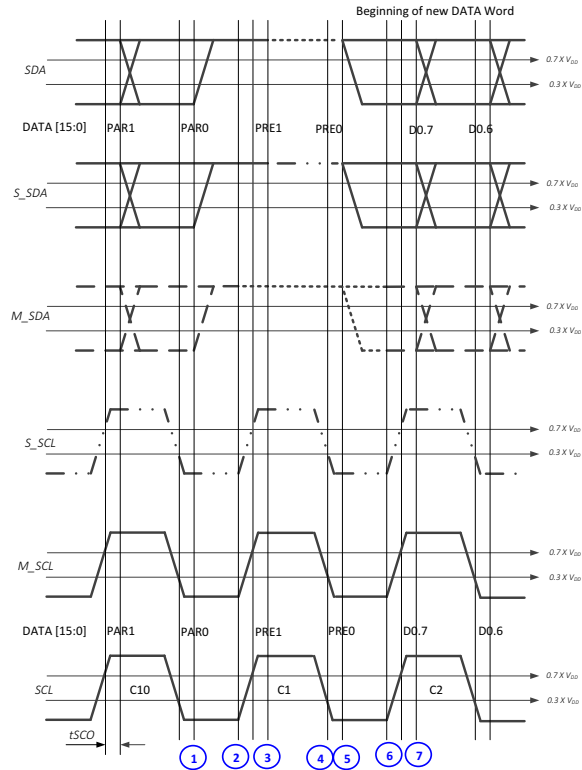
HDR-DDR – Slave controls DDR READ command



HDR-DDR – Master Controls DDR READ Transaction [1]

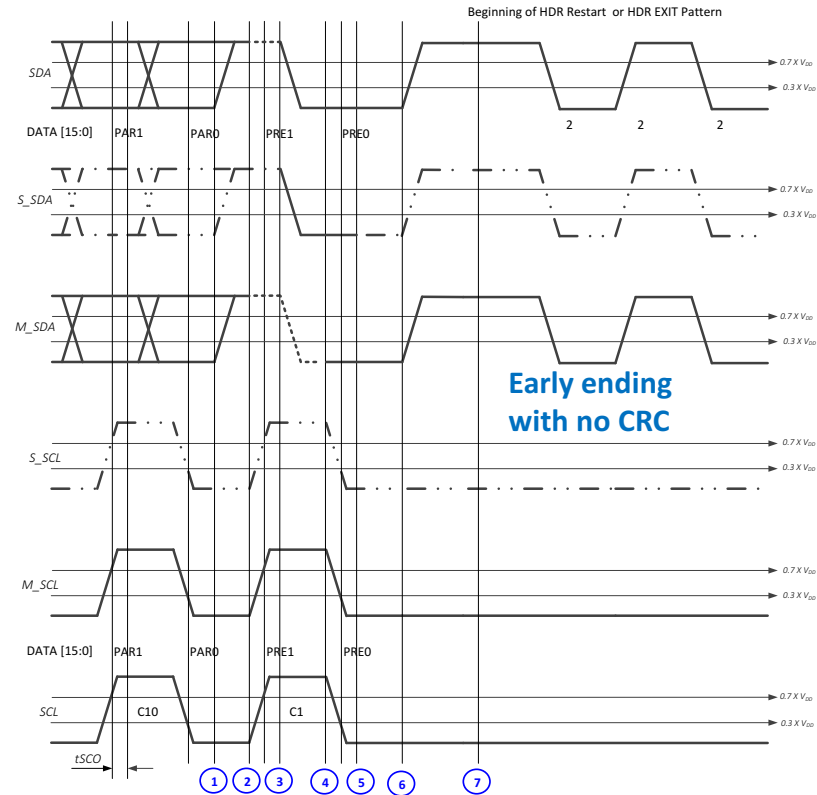
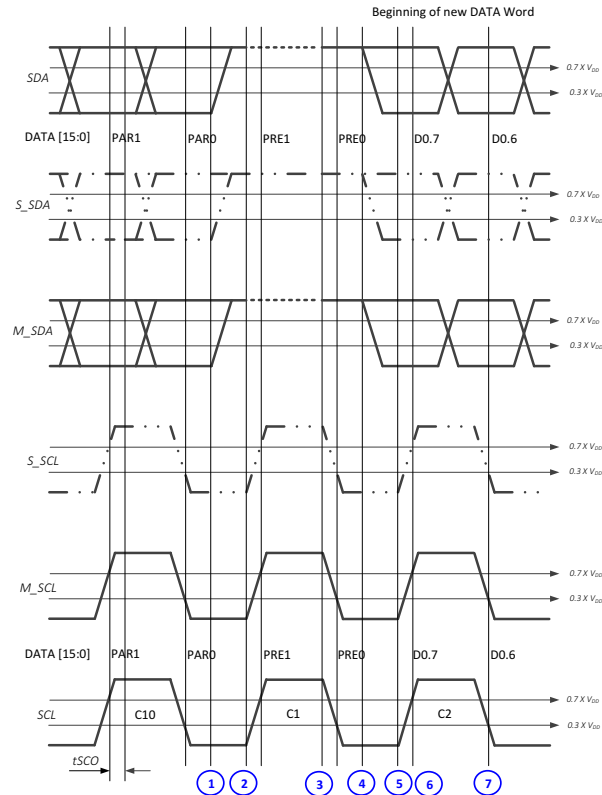


HDR-DDR – Master Controls DDR READ Transaction [2]

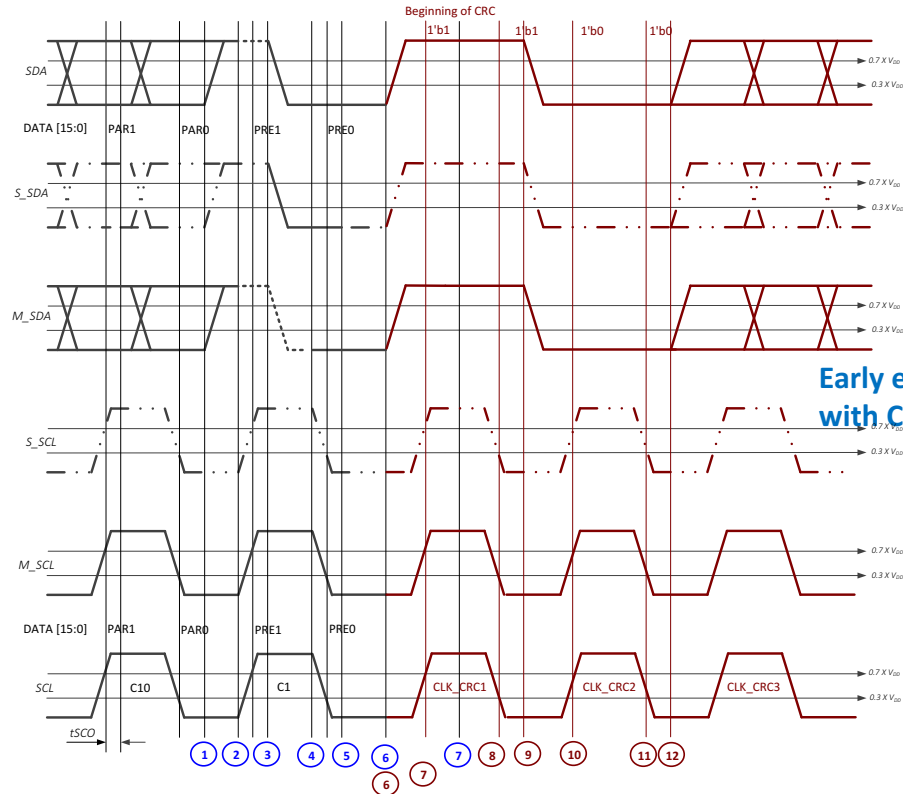
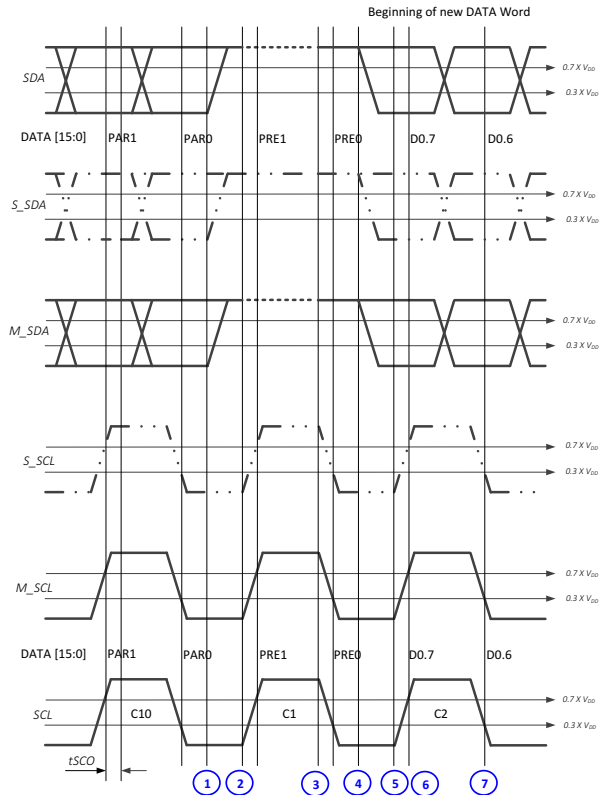


Early ending with CRC

HDR-DDR – Slave Requests DDR WRITE Termination [1]

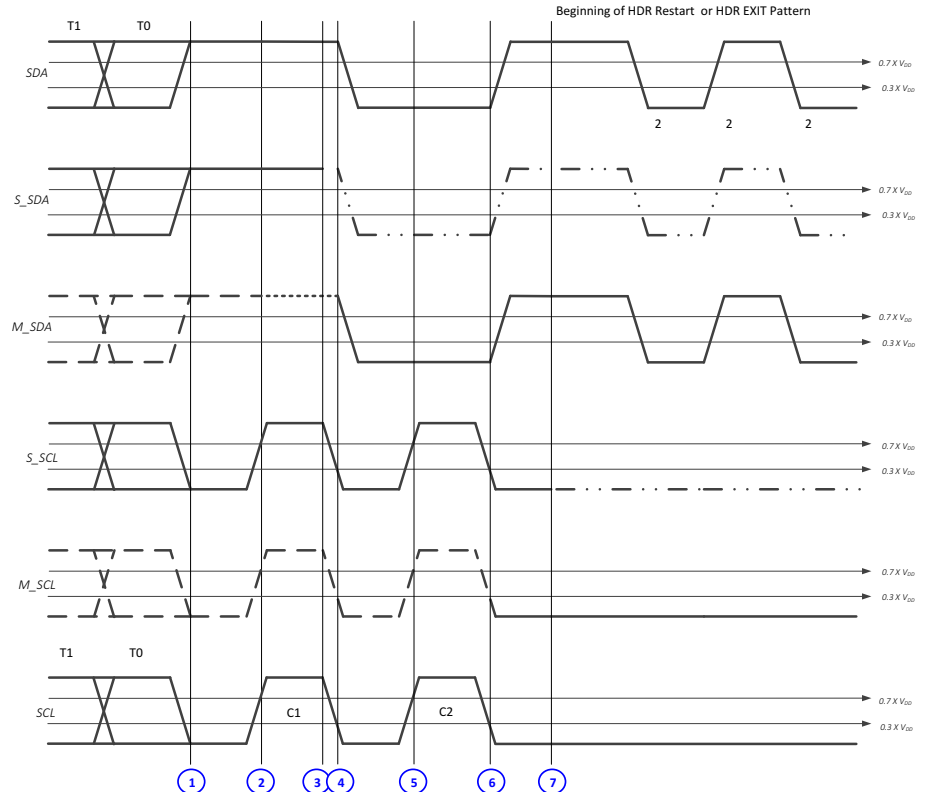
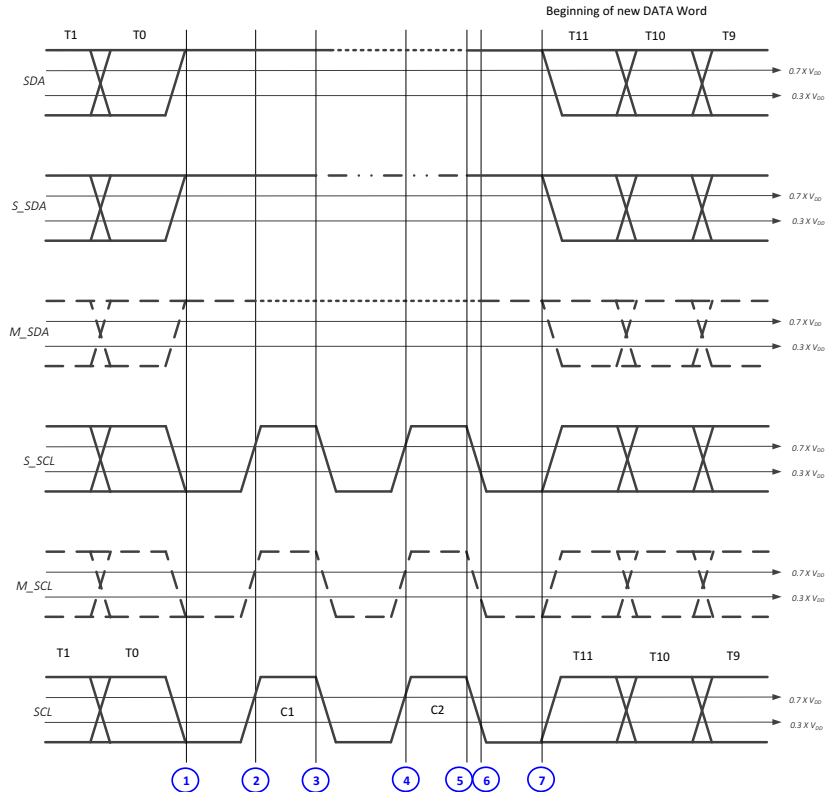


HDR-DDR – Slave Requests DDR WRITE Termination [2]

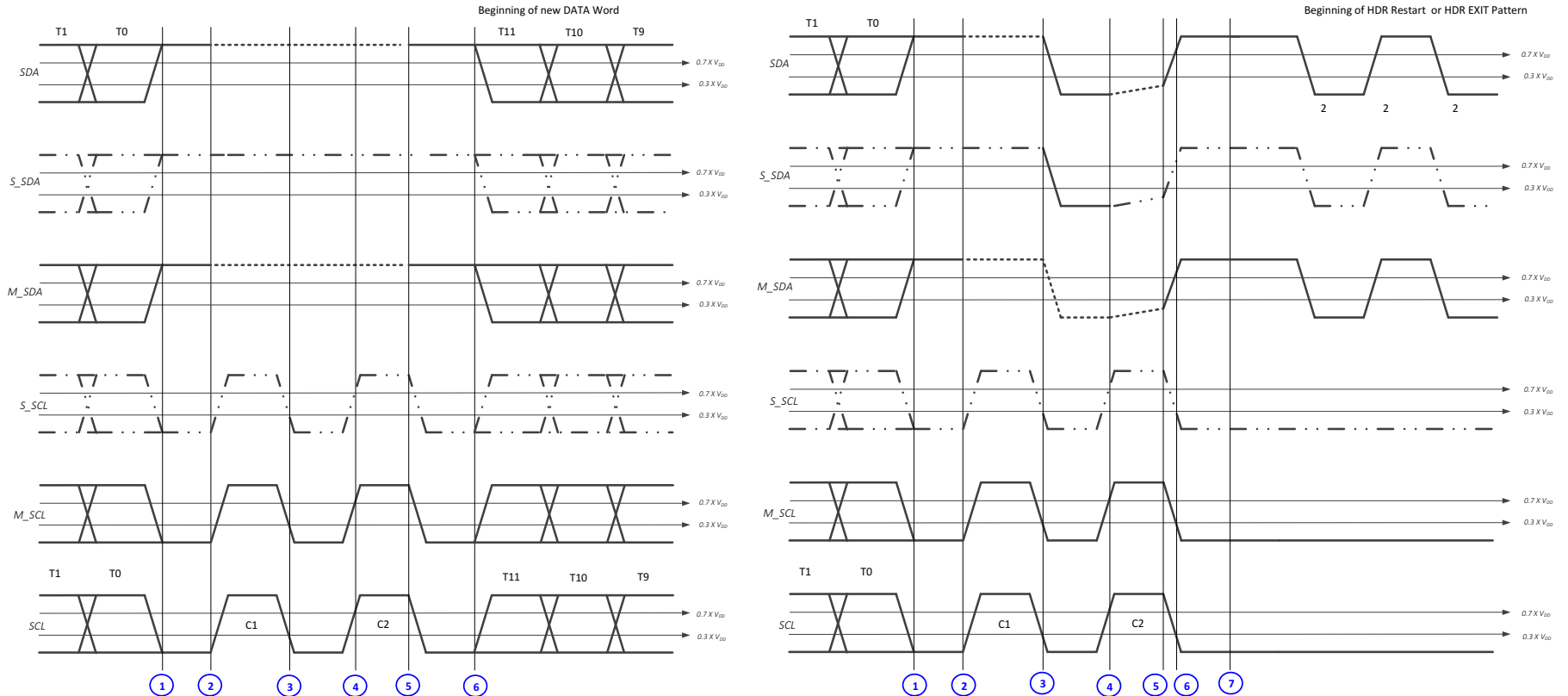


Early ending
with CRC

HDR-TSx – Master Controls S2M Data Transfer



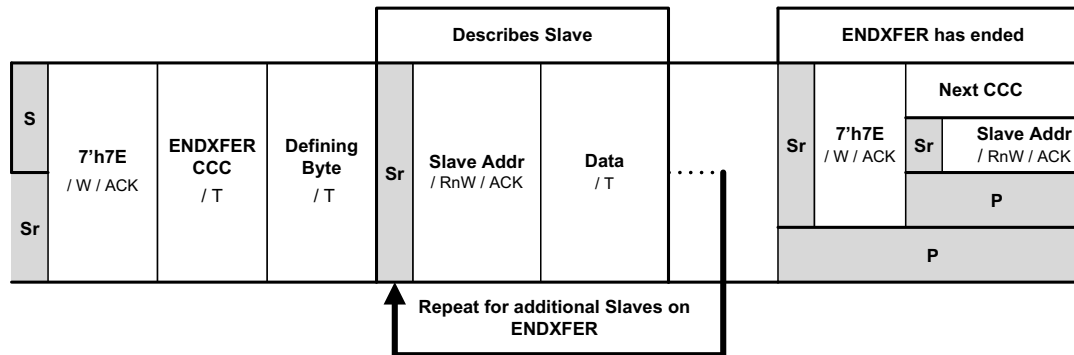
HDR-TSx – Slave Controls the M2S Data Transfer



ENDXFER CCC – Early Termination Setup and Invocation

- Defining Bytes
 - 0x7F – SET/GET Repetition Interval for HDR-TSx
 - 0x55 – Initiates the HDR-TSx with Ending Data Transfer Procedure Enabled
 - 0xF7 – SET/GET CRC Index for HDR-DDR
 - 0xAA – Initiates the HDR-DDR with Ending Data Transfer Procedure Enabled

S	7'h7E	ENDXFER CCC	Defining Byte	(Optional) Data	Sr
Sr	/ W / ACK	/ T	/ T	/ T	P





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