mipi®
DEVCON

Ashraf Takla
President & CEO
Mixel, Inc.

C.K. Lee
Director, Engineering
Qualcomm Technologies, Inc.

MIPI C-PHY^{SM}/D-PHY^{SM} Dual Mode Subsystem Performance & Use Cases

2017
MIPI ALLIANCE
DEVELOPERS
CONFERENCE

HSINCHU CITY, TAIWAN
MIPI.ORG/DEVCON

Agenda

- MIPI D-PHY spec
  - Overview
  - Block diagram
- MIPI C-PHY spec
  - Overview
  - Block diagram
  - C-PHY additional block
- Comparison: D-PHY vs. C-PHY
  - Advantage
  - Disadvantages
- Dual mode MIPI D-PHY/MIPI C-PHY
- Silicon Results
  - TX
  - RX
- Use Cases
  - Camera
  - Display
- Adoption
- Challenges
- Conclusion
- Q & A

Mixel, Inc.

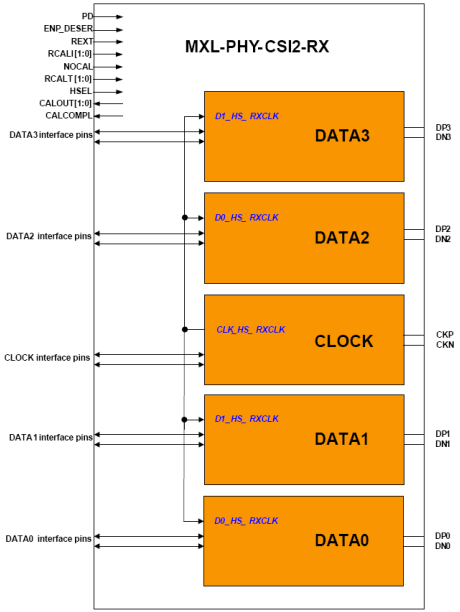
Qualcomm Technologies, Inc. Technologies, Inc.

MIPI D-PHY Specifications & Performance

- Spec version versus data rate

Standard	Version	Adopted	Data Rate (Per Lane)	PHY Interface (Per Lane)
MIPI D-PHY	1.0	Sep 2009	1.0 Gbps	8 bit
	1.1	Dec 2011	1.5 Gbps	8 bit
	1.2	Sep 2014	2.5 Gbps	8 bit
	2.0	Mar 2016	4.5 Gbps	8/16/32 bit
	2.1	March 2017	4.5 Gbps	8/16/32 bit

MIPI D-PHY Block Diagram



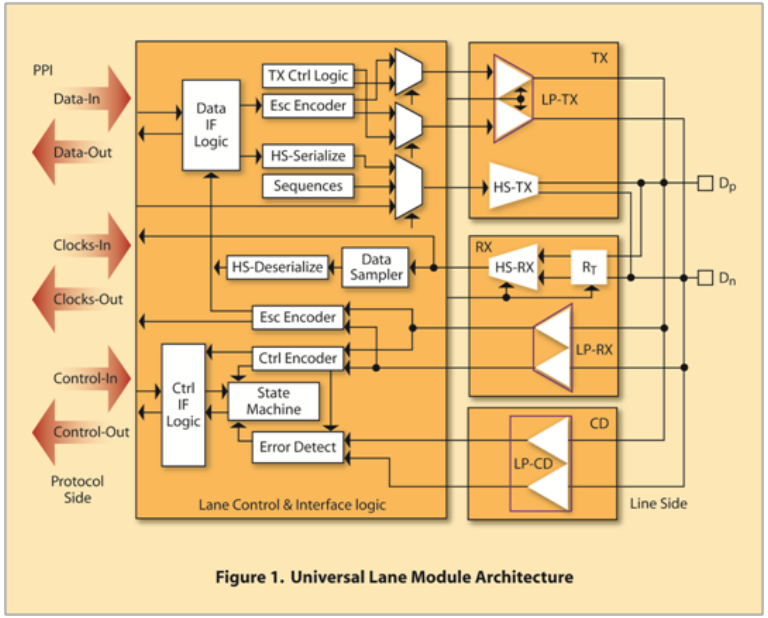
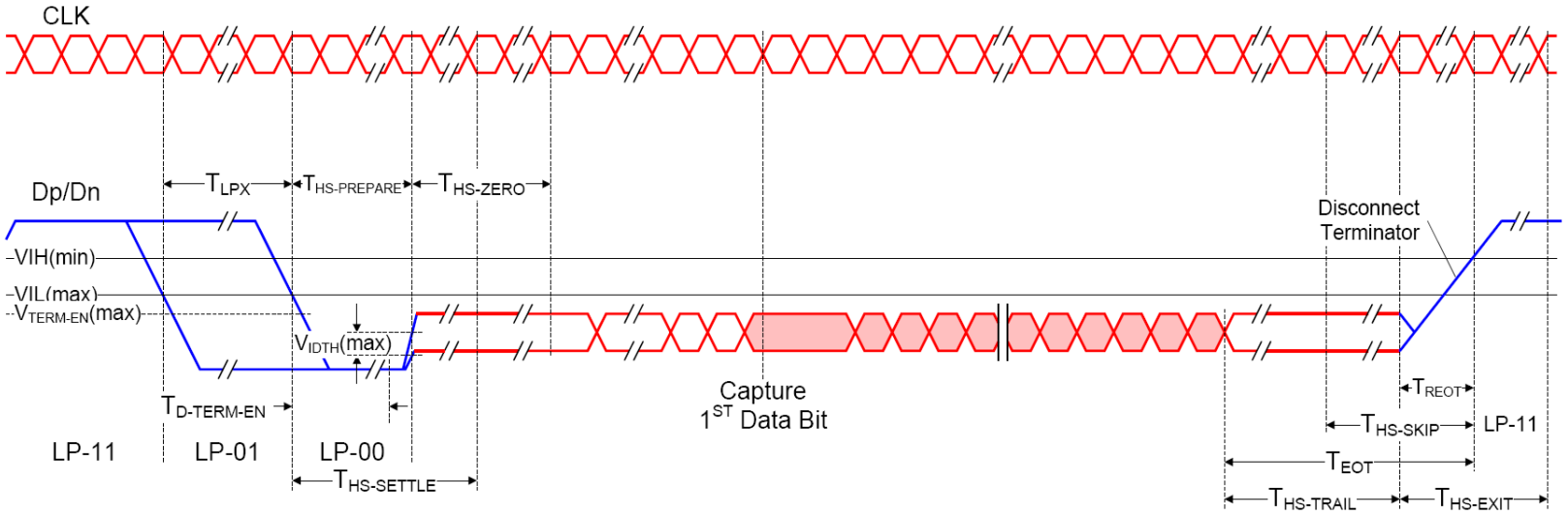


Figure 1. Universal Lane Module Architecture

Mixel, Inc.

Qualcomm Technologies, Inc.

MIPI D-PHY HS & LP Operation



Mixel, Inc.

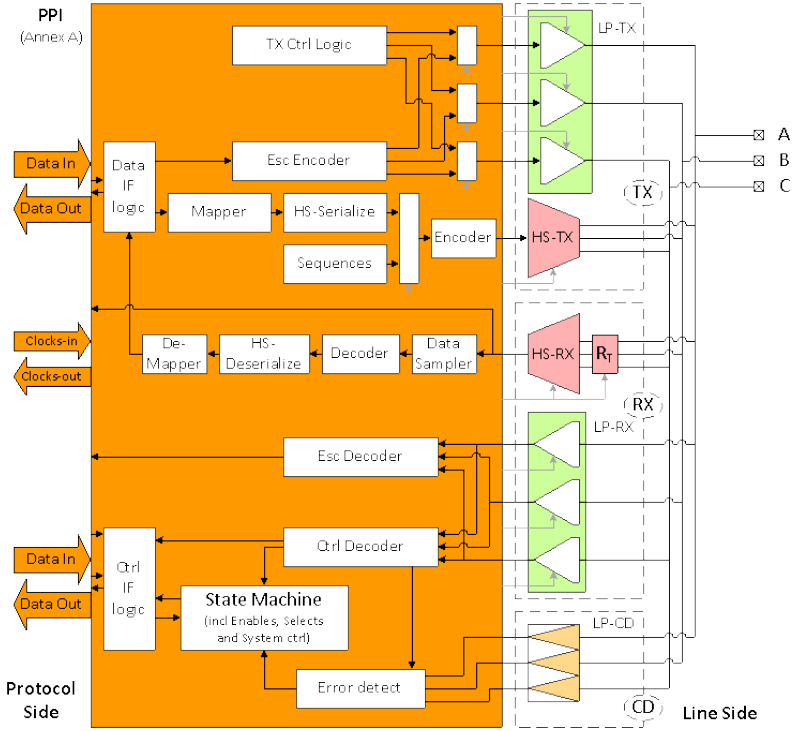
Qualcomm Technologies, Inc.

MIPI C-PHY Block Specifications & Performance

- Spec version versus data rate

Standard	Version	Adopted	Data Rate (Per Trio)	PHY Interface (Per Trio)
MIPI C-PHY	1.0	Oct 2014	2.5 Gsps	16 bit
	1.1	Feb 2016	2.8 Gsps	16/32 bit
	1.2	March 2017	3.5 Gsps	16/32 bit
Note: A MIPI C-PHY lane is known as a Trio. 1 Sym = 2.28 bits				

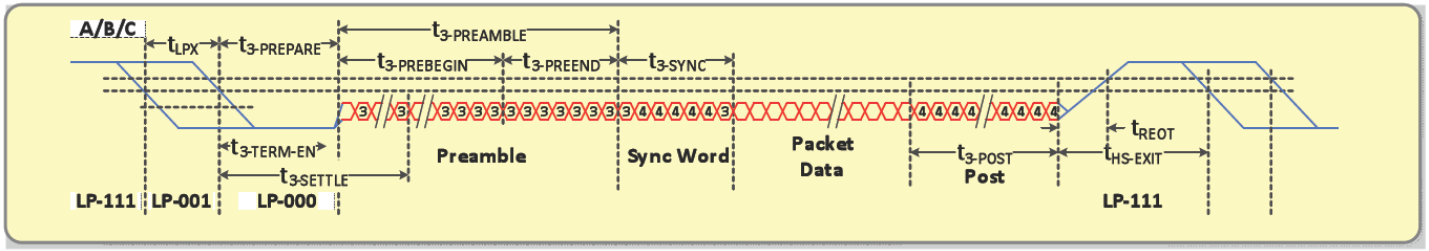
MIPI C-PHY Block Diagram

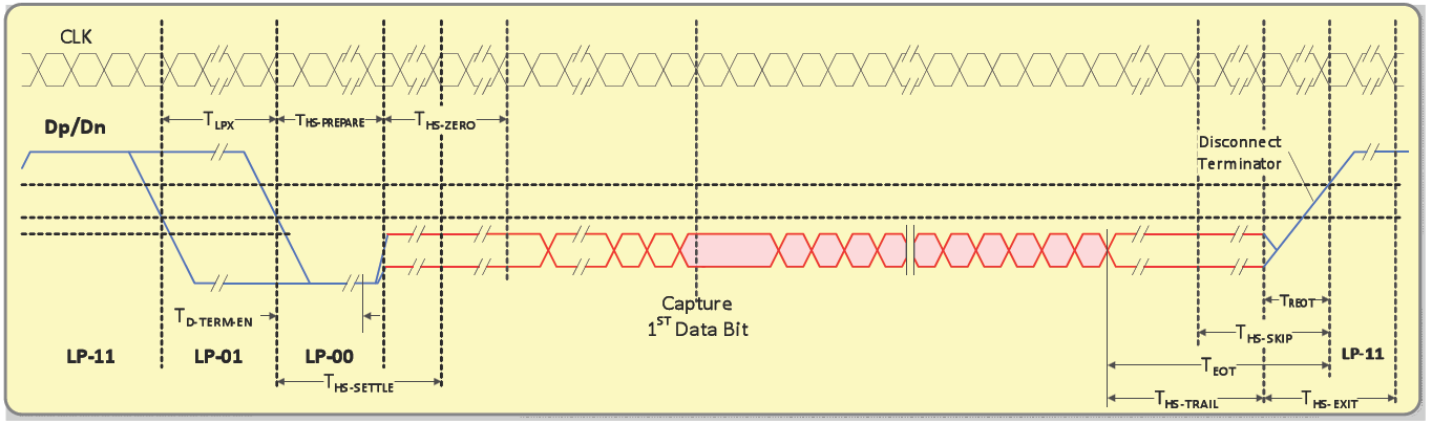


Mixel, Inc.

Qualcomm Technologies, Inc.

MIPI C-PHY and MIPI D-PHY HS & LP Operation





Mixel, Inc.

Qualcomm Technologies, Inc.

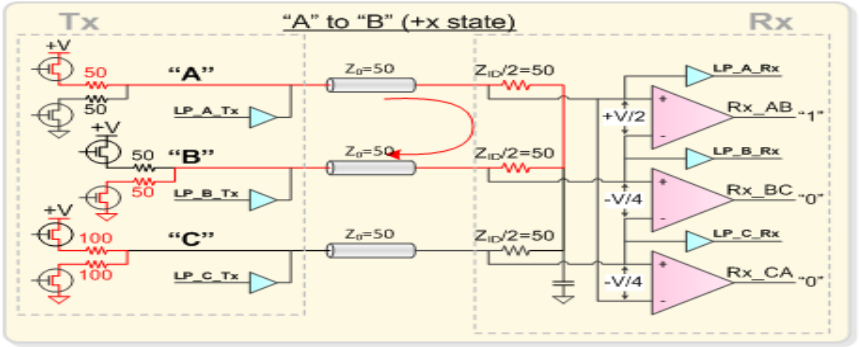
MIPI C-PHY Unique Features

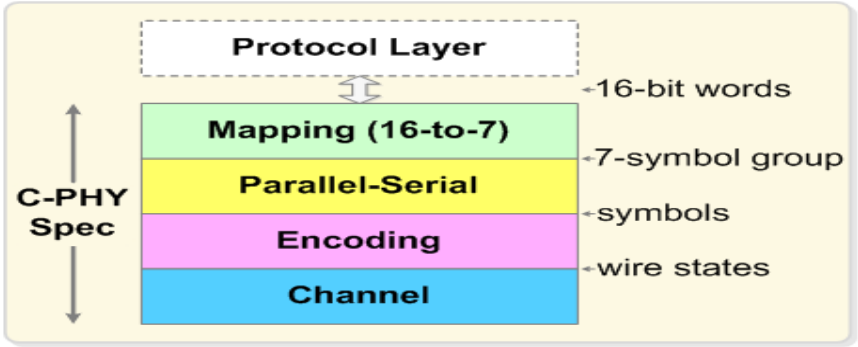
- Performance (bit rate 2.28x the signaling rate, e.g. 1Gsps=2.28Gbps)
  - Higher than D-PHY on a nominal 10-wire port by 1.7X
- Pins
  - Fewer pins & balls (due to higher performance per pin)
  - Flexibility, due to the independence of each lane, clock is embedded, you can borrow one lane from one link to another
  - Coexists on same pins with MIPI D-PHY
- Lower Power at higher data rate applications
- Flexibility
  - Embedded clock enables assignment of any lane on the AP to any link
  - Free of MIPI D-PHY 's need to associate data lanes with a clock lane
- Interference (Low emissions)
  - Embedded clock eliminates clock spur emissions, particularly important in multi-band wireless devices
- Embedded control codes enable efficient emerging features:
  - Alternate Low Power mode (ALP), enables longer reach by eliminating single-ended LP mode, which results in area reduction
  - Fast BTA operations
  - Lower latency (LRTE) for time-sensitive links
- Lower toggle rate often simplifies manufacturing and lowers costs
  - More applicable to low cost products, such as low-end cameras

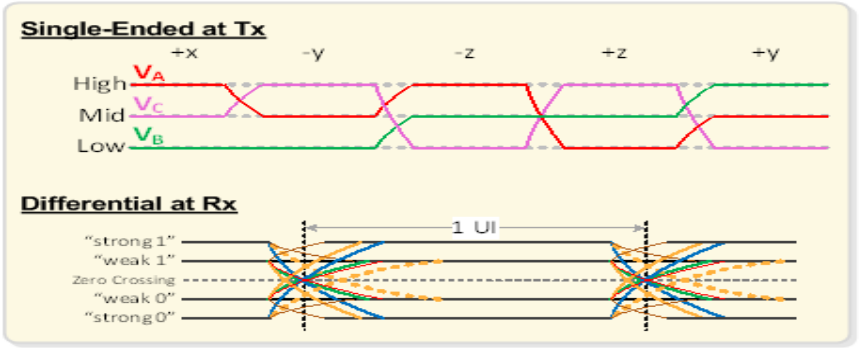
Mixel, Inc.

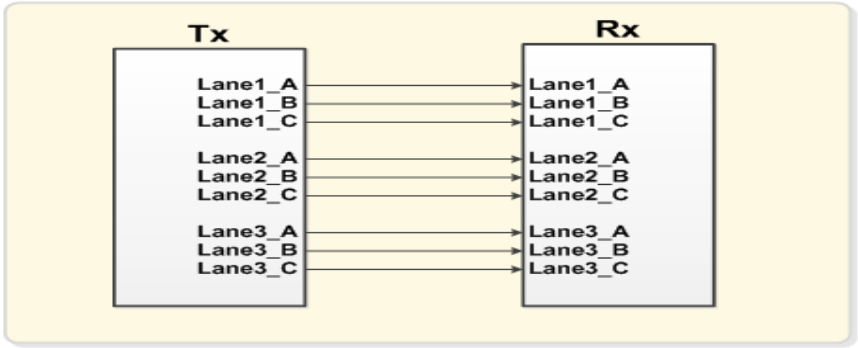
Qualcomm Technologies, Inc.

MIPI C-PHY Brief Overview







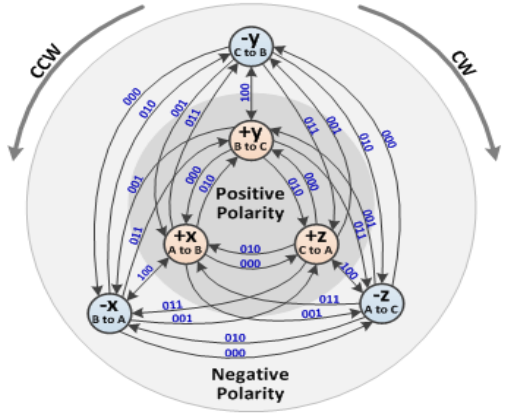


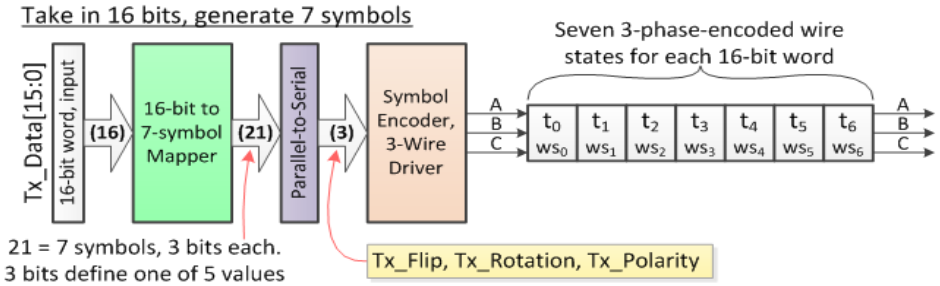
Mixel, Inc.

Qualcomm Technologies, Inc.

Overview, Encoding & Mapping (at a High Level)

- **Encoding** of clock & data, Symbols to Wire States.
  - 6 Wire States; 5 possible transitions from each.
  - $\log_2(5) \cong 2.3219$ bits/symbol capacity, in-theory,
    C-PHY uses $16 \div 7 \cong 2.2857$ bits/symbol
- **Mapping** converts 16-bit word to 7 symbols.
  - 16 bits $\Rightarrow 2^{16} = 65{,}536$ states,
    7 symbols $\Rightarrow 5^7 = 78{,}125$ states.
  - 12,589 states left over; ≅0.0362 bits/symbol are wasted!
    - Actually, what's left over goes to good use!
      - Synchronization
      - Link Control
      - Event signaling
      - LP Data transmission
      - Run-Length Limiting





MIPI D-PHY and MIPI C-PHY Comparison

Parameter	MIPI D-PHY v1.2	MIPI C-PHY v1.0
Design	Simple, source synchronous clock	Embedded clock, edge detection CDR
Power/Gbps	Larger	Smaller
Area (min. configuration)	Smaller Area	Larger, Additional blocks
Area/Gbps(1)	Larger	Smaller
Bandwidth (D-PHY 1.2 vs. C-PHY 1.0)	Max 10G for 4 lanes (10pins)	Max 17.1G for 3 lanes (9pins)(2)

(1) Four data D-PHY lanes vs. three MIPI C-PHY trios
(2) Higher bandwidth due to Encoding

Mixel, Inc.

Qualcomm Technologies, Inc.

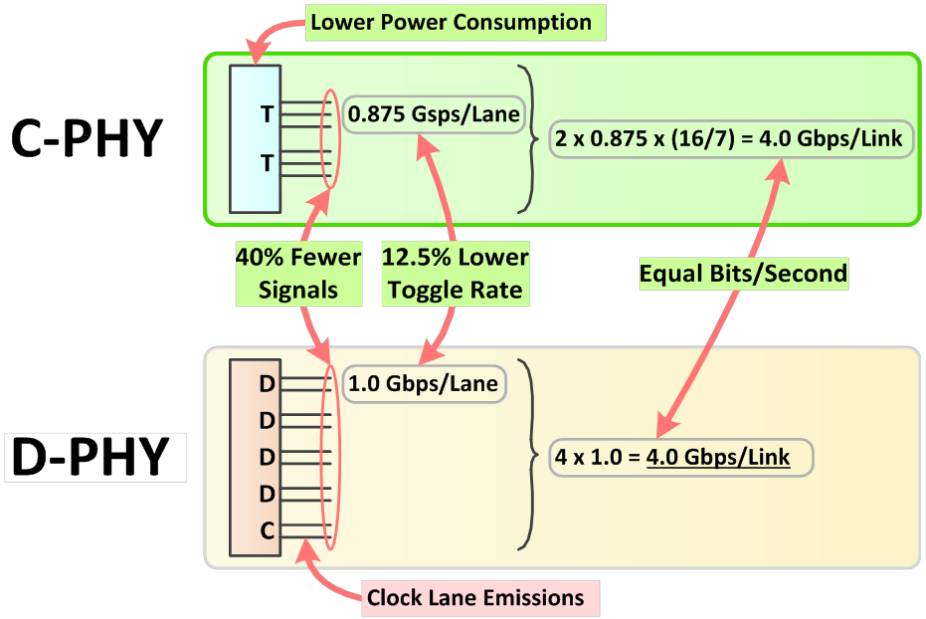
MIPI D-PHY and MIPI C-PHY Comparison

Parameter	MIPI D-PHY v1.2	MIPI C-PHY v1.0
Minimum # of pins	4	3
Flexibility	All lanes operate together	Each Lane works independently. High flexibility
Transmission Efficiency	1 Bit/UI	2.28 Bit/UI
Testing	Challenge due to LP and HS modes	Additional complexity due to 3 wires
Adoption	Long history of use, wider adoption	Accelerated adoption, co-exists with MIPI D-PHY

Mixel, Inc.

Qualcomm Technologies, Inc.

MIPI D-PHY and MIPI C-PHY Comparison



- At the Same Link Rate, C-PHY has:
  - Fewer wires (up to 40% less)
  - Lower Toggle Rate/Lane (12.5% lower)
  - Lower Power Consumption (~20-50% lower)
  - Smaller number of lanes, thus smaller area for same Gbps
  - No Emissions from a Clock Lane

Mixel, Inc.

Qualcomm Technologies, Inc.

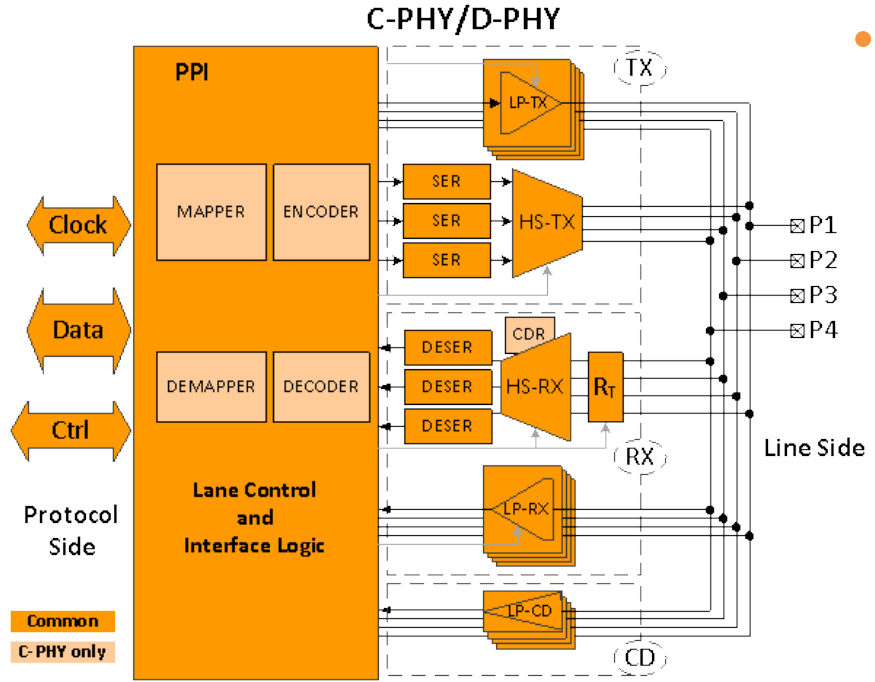
Mixel Dual Mode MIPI D-PHY/MIPI C-PHY Advantages

- Sharing of the serial interface pins
- Sharing of common blocks, resulting in area reduction
- Power/Gbps reduction
- Smooth transition between MIPI D-PHY and MIPI C-PHY
- Has the benefit of the MIPI C-PHY PPA improvements, while maintaining compatibility with MIPI D-PHY, using same pins

Mixel, Inc.

Qualcomm Technologies, Inc.

Mixel MIPI C-PHY/MIPI D-PHY Combo IP



- Combo IP Blocks
  - Shared between MIPI C-PHY and MIPI D-PHY:
    - HS-TX, HS-RX, SER, DESER, LP-TX, LP-RX and LP-CD
  - Added for MIPI C-PHY:
    - Encoder, Decoder, CDR, Mapper and De-Mapper
  - *All MIPI D-PHY functional blocks are reused for the MIPI C-PHY*

Mixel, Inc.

Qualcomm Technologies, Inc.

Foundries and nodes

Foundry	65nm	55nm	40nm	28nm	14nm	10nm	7nm
F1	**S**	**S**		**P**			***P***
F2			**S**				
F3					***S***	***S***	***P***

S : Silicon-proven

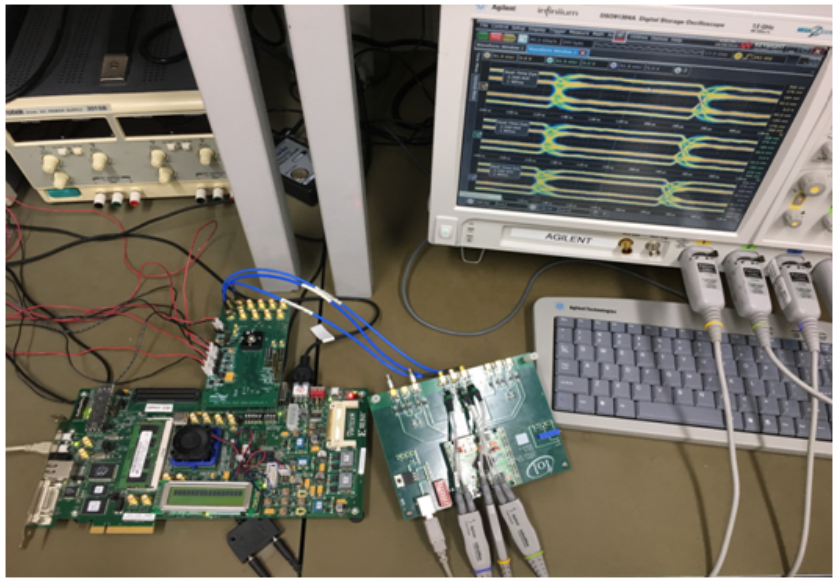
P: Pre-silicon

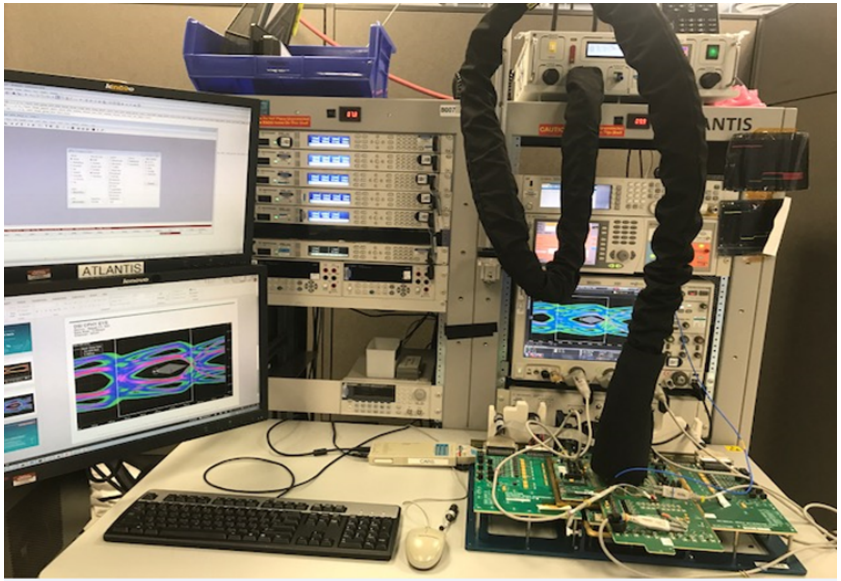
Mixel and ***Qualcomm***

Mixel, Inc.

Qualcomm Technologies, Inc.

Silicon results TX



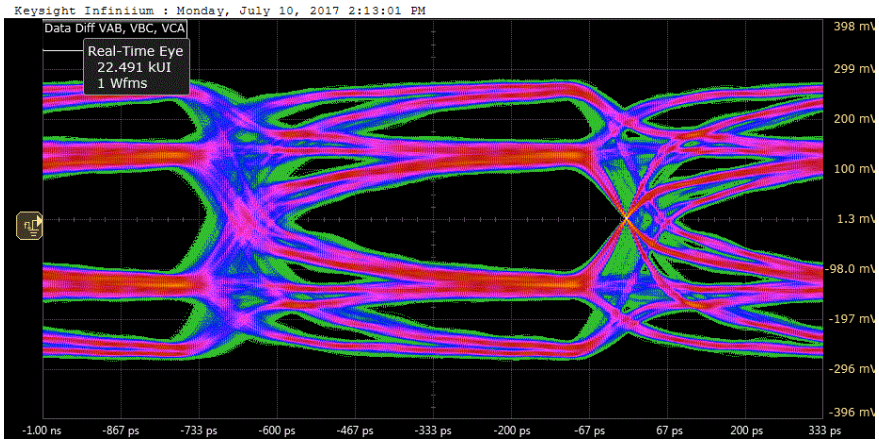


MIPI C-PHY Transmitter Testing Set-up

Mixel, Inc.

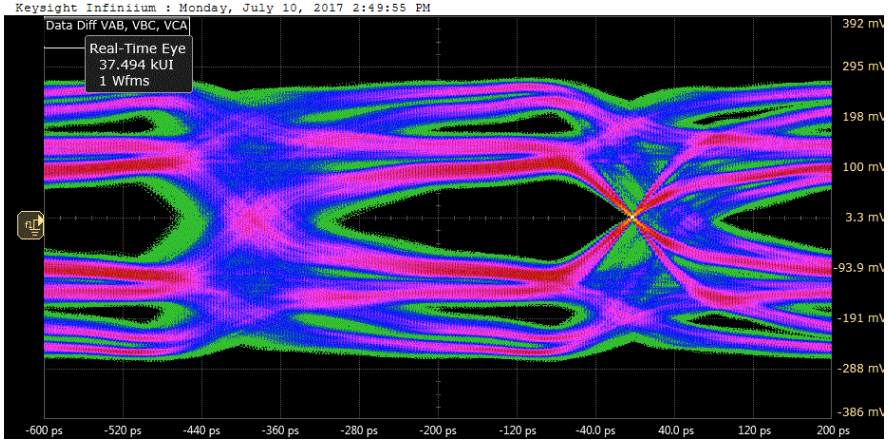
Qualcomm Technologies, Inc.

Silicon Results TX MIPI C-PHY – Eye Diagrams



1.5 GSPS

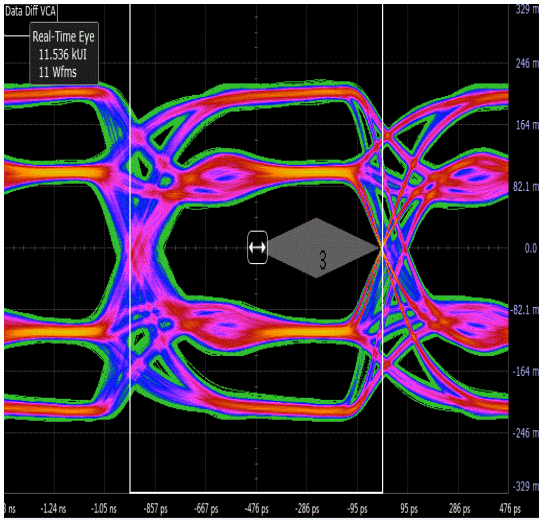
Mixel, Inc.



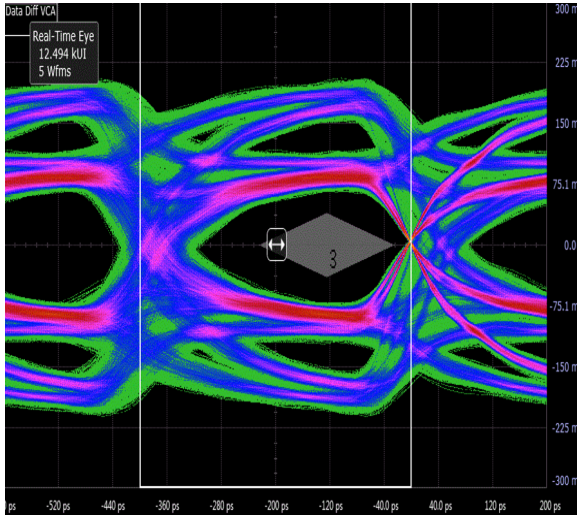
2.5 GSPS

Qualcomm Technologies, Inc.

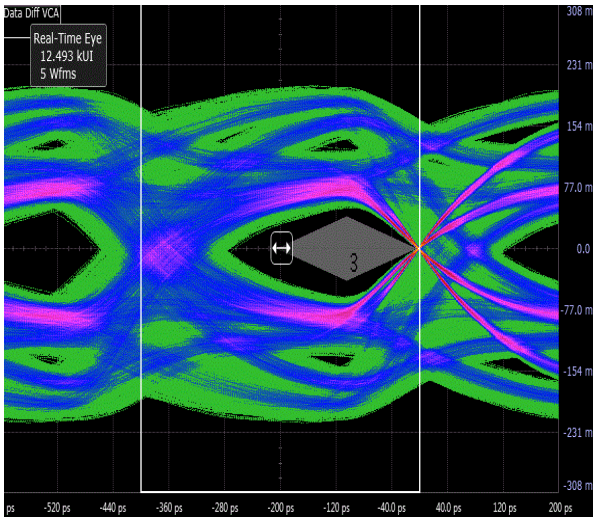
Silicon Results TX MIPI C-PHY – Eye Diagrams



1.05 GSPS @ std channel



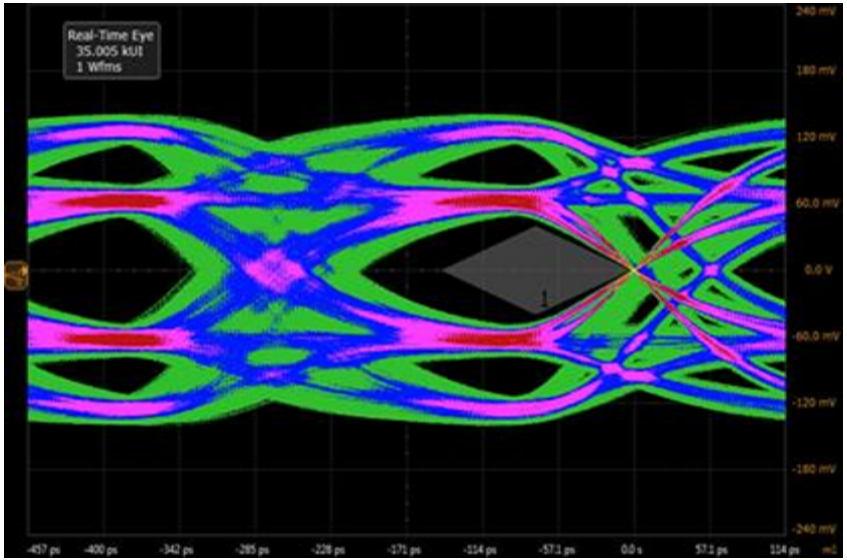
2.5 GSPS @ short channel



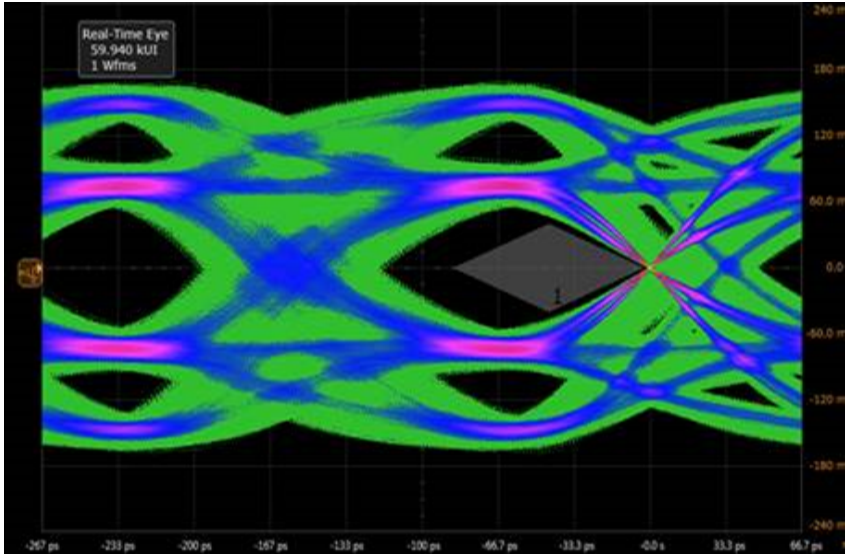
2.5 GSPS @ std channel

Qualcomm Technologies, Inc.

Silicon Results TX MIPI C-PHY – Eye Diagrams



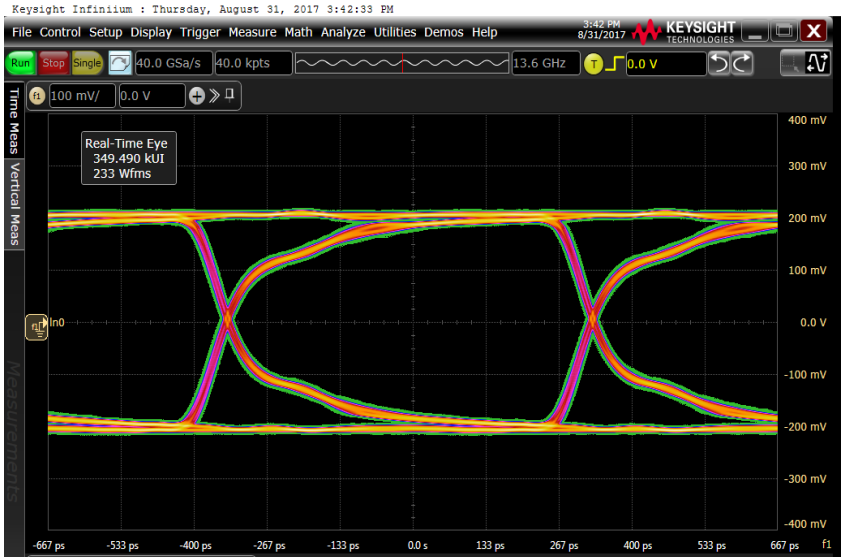
3.5 GSPS @ standard channel



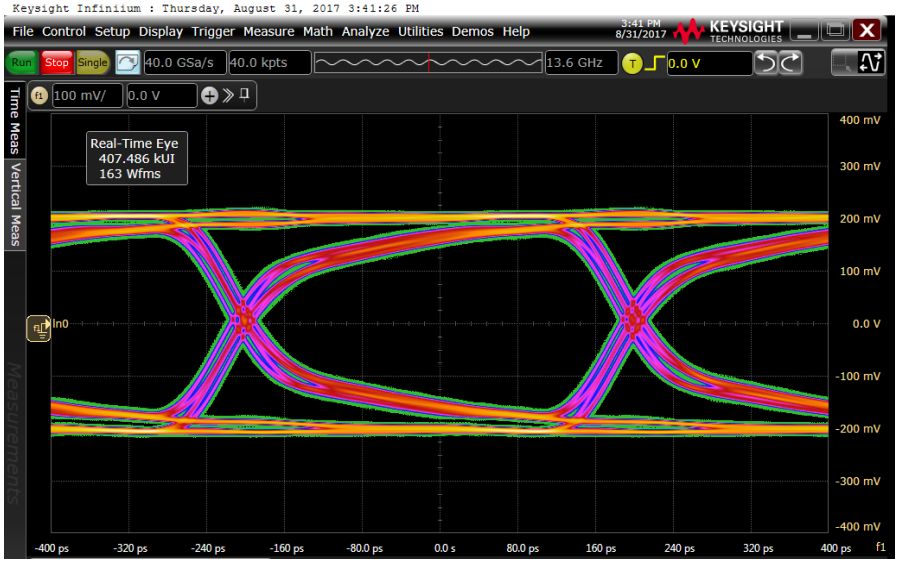
6.5 GSPS @ short channel

Sony

Silicon results TX MIPI D-PHY – Eye Diagrams



1.5 GBPS

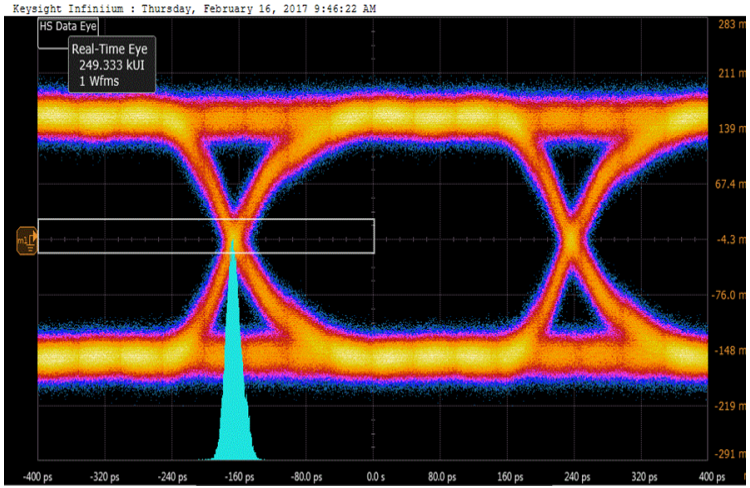


2.5 GBPS

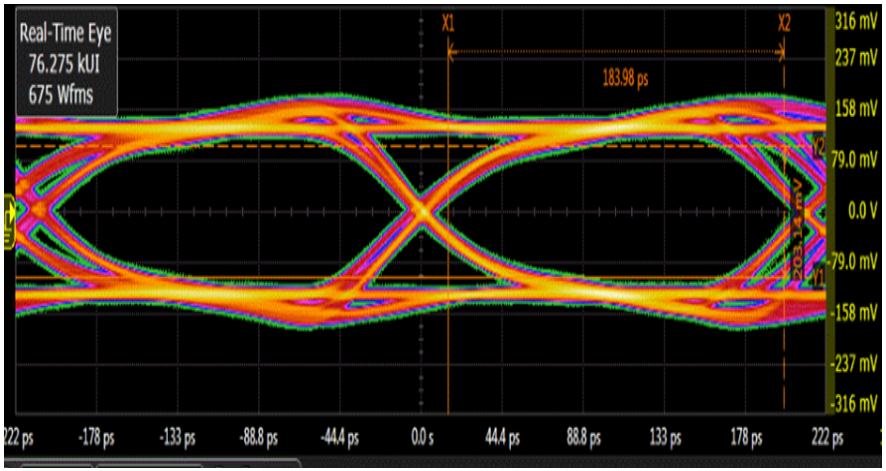
Mixel, Inc.

Qualcomm Technologies, Inc.

Silicon Results TX MIPI D-PHY – Eye Diagrams



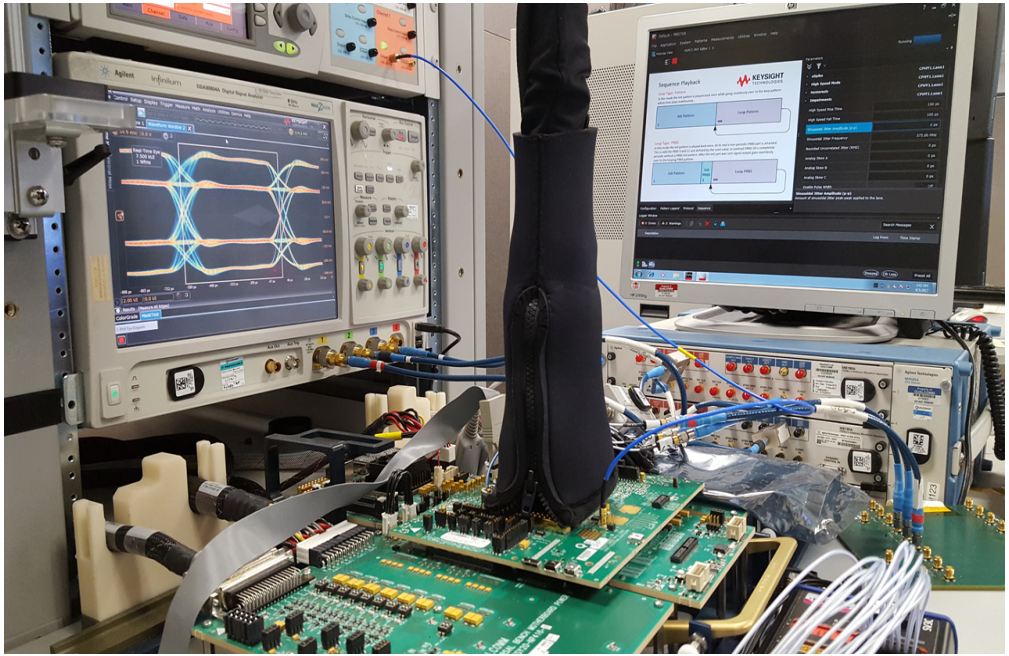
2.5 GSPS @ short channel



4.5 GSPS @ short channel

Qualcomm Technologies, Inc.

Silicon Results RX - Electrical

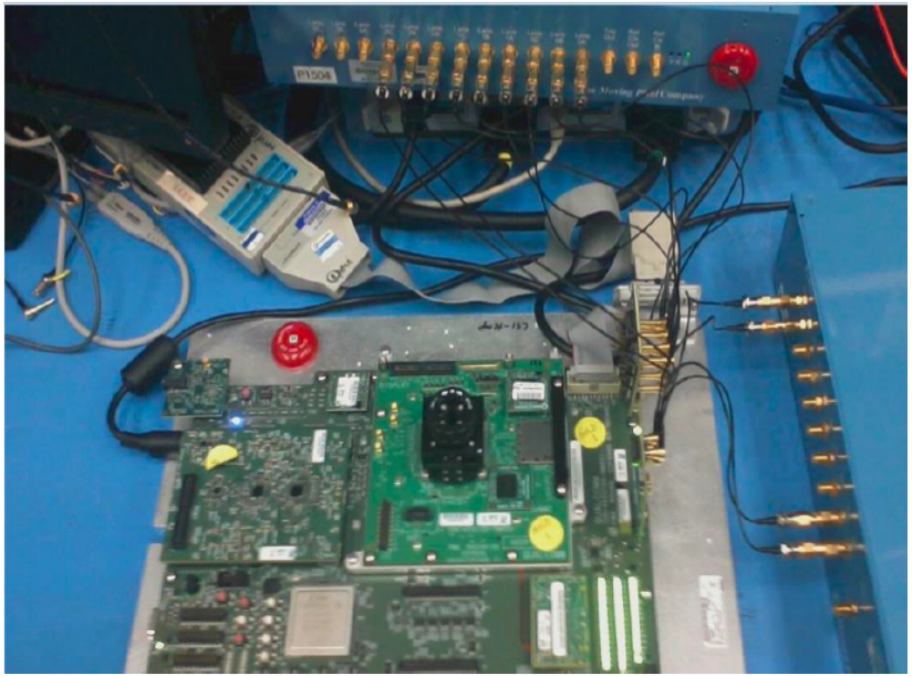


Group	Test Name	1 TT Device @ NV/25C SPEC min	SPEC max	Worst Case	Pass/Fail
(Group 2) LP-RX Voltage and Timing Requirements	LP-VIH	740mV		650 mV	Pass
	LP-VIL		550mV	570mV	Pass
	LP Hysteresis	25 mV			Pass
	Tmin Rx	20nS			Pass
	Espike		312Vps		Pass
(Group 3) HS-RX Voltage and Jitter Tolerance Requirements	HS-VIHHS		535mV		Pass
	HS-VIHLS	-40mV			Pass
	VIDTH		40mV		Pass
	VIDTL	-40mV			Pass
	HS-Prepare	38nS	95nS		Pass
	HS-PreBegin	7UI	448UI		Pass
	HS-ProSeq	0UI	14UI		Pass
	HS-Post	7UI	224UI		Pass
	JTOL	Calibrated Eye			Pass
Interface Impedance	Impedance				Pass

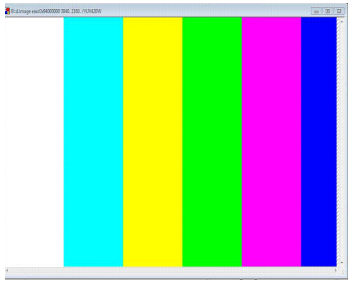
Mixel, Inc.

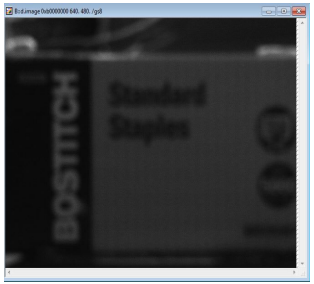
Qualcomm Technologies, Inc.

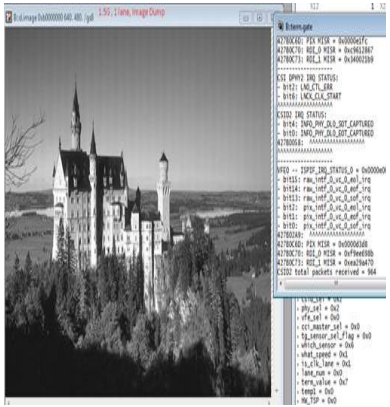
Silicon Results RX - Link



Mixel, Inc.

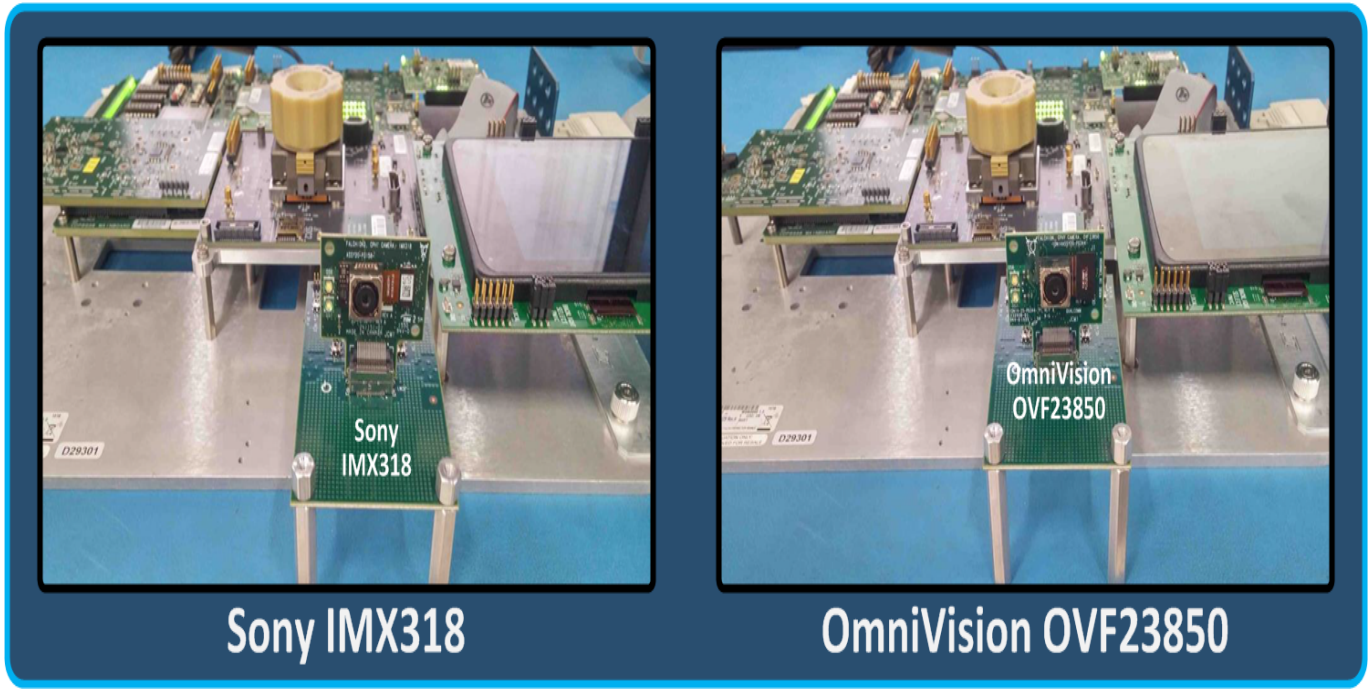




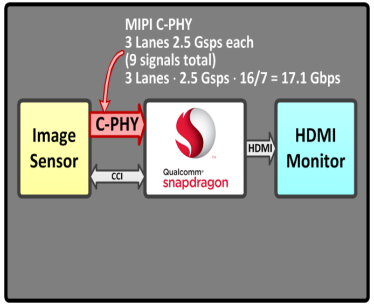


Qualcomm Technologies, Inc.

Example use case: camera bring up

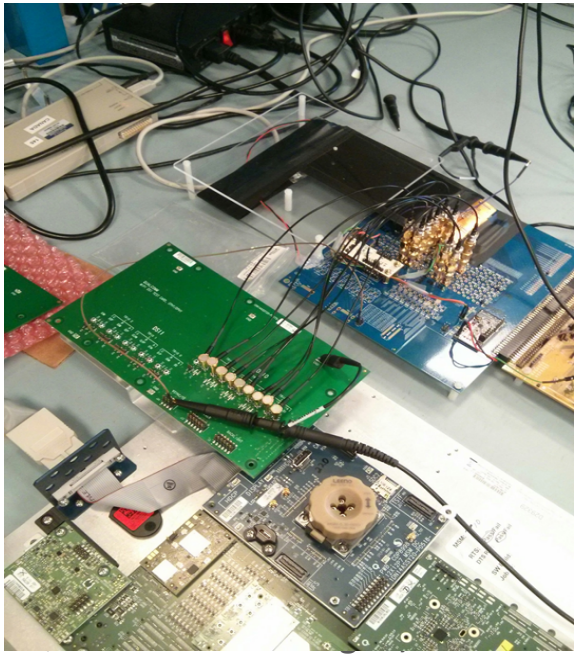


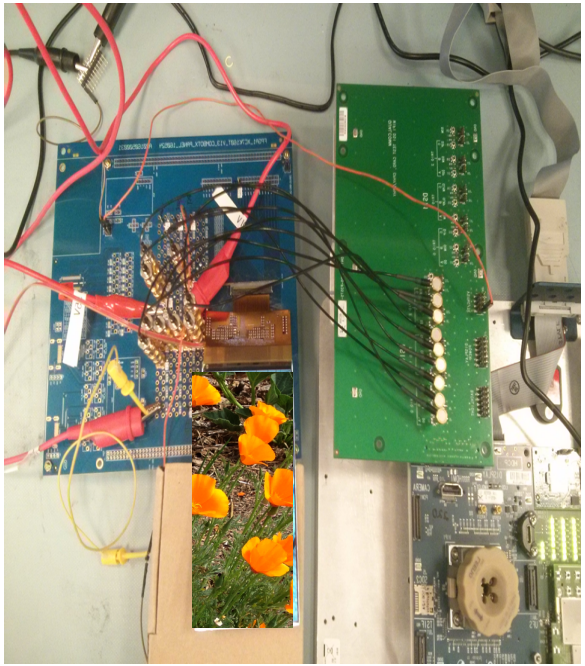
Mixel, Inc.

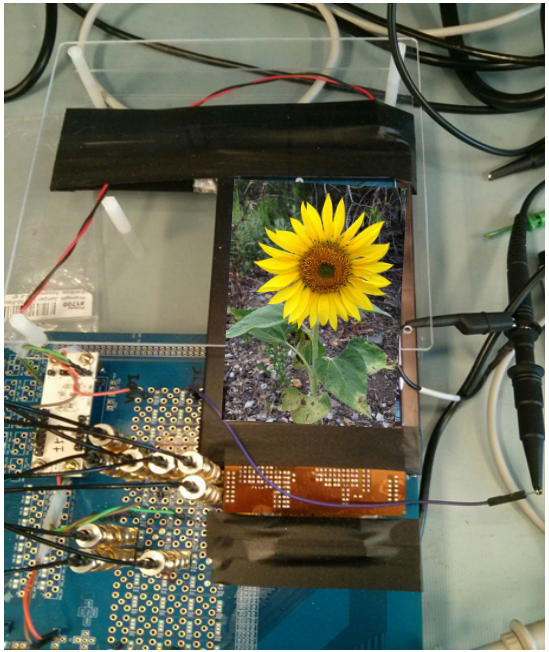


Qualcomm Technologies, Inc.

Example use case: Display bring up







1440x2560

Qualcomm Technologies, Inc.

MIPI C-PHY/MIPI D-PHY PPA - Qualcomm

TX

2560x1600	BW(Gbps)	data rate / lane (Gsps)	normalized Power
DPHY (4lane)	8.60	2.15	1.00
CPHY-T2 (3trio)	8.60	1.26	1.11
CPHY-T1 (3trio)	8.60	1.26	0.91

4k@30	BW(Gbps)	data rate / lane (Gsps)	normalized Power
DPHY (4lane)	9.17	2.29	1.00
CPHY-T2 (3trio)	9.17	1.34	1.08
CPHY-T1 (3trio)	9.17	1.34	0.89

3580x1600	BW(Gbps)	data rate / lane (Gsps)	normalized Power
DPHY (4lane)	12.00	3.00	1.00
CPHY-T2 (3trio)	12.04	1.76	0.90
CPHY-T1 (3trio)	12.04	1.76	0.76

4k@60	BW(Gbps)	data rate / lane (Gsps)	normalized Power
DPHY (4lane)	12.74	3.19	1.00
CPHY-T2 (3trio)	12.74	1.86	0.89
CPHY-T1 (3trio)	12.74	1.86	0.75

TX Area	BW(Gbps)	data rate / lane (Gsps)	normalized Area
DPHY	10.00	2.50	1.00
C/D Combo PHY	17.10	2.50	1.08

RX

21Mp@30fps	BW(Gbps)	data rate / lane (Gsps)	normalized Power
DPHY (4lane)	7.56	1.89	1.00
CPHY (3trio)	7.56	1.11	0.77
CPHY (3trio)-new RX	7.56	1.11	0.59

24Mp@30fps	BW(Gbps)	data rate / lane (Gsps)	normalized Power
DPHY (4lane)	8.64	2.16	1.00
CPHY (3trio)	8.62	1.26	0.75
CPHY (3trio)-new RX	8.62	1.26	0.58

40Mp@30fps	BW(Gbps)	data rate / lane (Gsps)	normalized Power
DPHY (4lane)	14.40	3.60	1.00
CPHY (3trio)	14.36	2.10	0.82
CPHY (3trio)-new RX	14.36	2.10	0.67

16Mp@120fps	BW(Gbps)	data rate / lane (Gsps)	normalized Power
DPHY (4lane)	23.04	5.76	1.00
CPHY (3trio)	23.04	3.37	0.89
CPHY (3trio)-new RX	23.04	3.37	0.76

RX Area	BW(Gbps)	data rate / lane (Gsps)	normalized Area
DPHY	10.00	2.50	1.00
C/D Combo PHY	23.94	3.50	1.09

- **Combo PHY area increment < 10%**
- **Combo PHY can cover wide range of Resolutions : 80Mpbs - 10Gbps - 17.1Gbps - 18Gbps - 23.94Gbps**
- **MIPI C-PHY mode : ~10-30% lower power than DPHY mode because of low freq/ smaller bias / lesser # of lanes**

Mixel, Inc.

Qualcomm Technologies, Inc.

MIPI C-PHY Adoption

- Camera & Display
  - [Cam] Sony / OVT / and others
  - [Display] Completed IOT test with most Major DDIC companies
- IP
  - Mixel
- AP (SOC)
  - SnapDragon, and others
- Tester
  - Keysight, Tektronix, Introspect, The Moving Pixel Company
- Common-mode filters
  - Murata, Panasonic, TDK

Mixel, Inc.

Qualcomm Technologies, Inc.

MIPI C-PHY Challenges

- Unique CDR that needs to be programmed for different data rate ranges
- Multi-level signal transmission
  - Introduces encoding jitter, but no need for multi-level detection on the RX side
- Unique Trio-based signaling
  - PCB design

Mixel, Inc.

Qualcomm Technologies, Inc.

Conclusion

- MIPI C-PHY is a more complex, powerful and efficient PHY. The MIPI D-PHY/MIPI C-PHY combo is even more so on all accounts
- MIPI C-PHY provides PPA improvement at the expense of additional complexity
- Combo PHY provides the flexibility to support both PHY's using same pins with minimal overhead, while enhancing PPA
- Most blocks are common between MIPI D-PHY and MIPI C-PHY, and thus are shared, resulting in small overhead for the combo IP
- There is good traction for MIPI C-PHY/MIPI D-PHY combo in MIPI CSI℠ applications and MIPI DSI℠ is coming online
- The MIPI C-PHY/MIPI D-PHY combo is silicon-proven in multiple nodes and foundries and has been integrated into several end products by many tier-one SOC, sensor, and display vendors

Mixel, Inc.

Qualcomm Technologies, Inc.

mipi®
DEVCON

Ashraf Takla
President & CEO
Mixel, Inc.

C.K. Lee
Director, Engineering
Qualcomm Technologies, Inc.

MIPI C-PHY^{SM}/D-PHY^{SM} Dual Mode Subsystem Performance & Use Cases

2017
MIPI ALLIANCE
DEVELOPERS
CONFERENCE

HSINCHU CITY, TAIWAN
MIPI.ORG/DEVCON