mipi®
DEVCON

Lalan Mishra
Principal Engineer
Qualcomm Technologies, Inc.

Satwant Singh
Sr. Director
Lattice Semiconductor

MIPI VGI℠ for Sideband GPIO and Messaging Consolidation on Mobile System

2017
MIPI ALLIANCE
DEVELOPERS
CONFERENCE

HSINCHU CITY, TAIWAN
MIPI.ORG/DEVCON

Agenda

- The Problem Statement
- Virtual GPIO Interface (MIPI VGI℠) : Concept
- MIPI VGI℠ Architecture
- Application Scenarios
- Summary
- Q&A

Mobile Connectivity Expansion Trends

Cellular

- 2G/3G/4G ➔ LTE-Advanced ➔ 5G

WiFi

- 802.11a/b/g/n/ac ➔ax
  802.11ad/WiGig

Video

- VGA/SD/HD ➔ 4K ➔ 8K

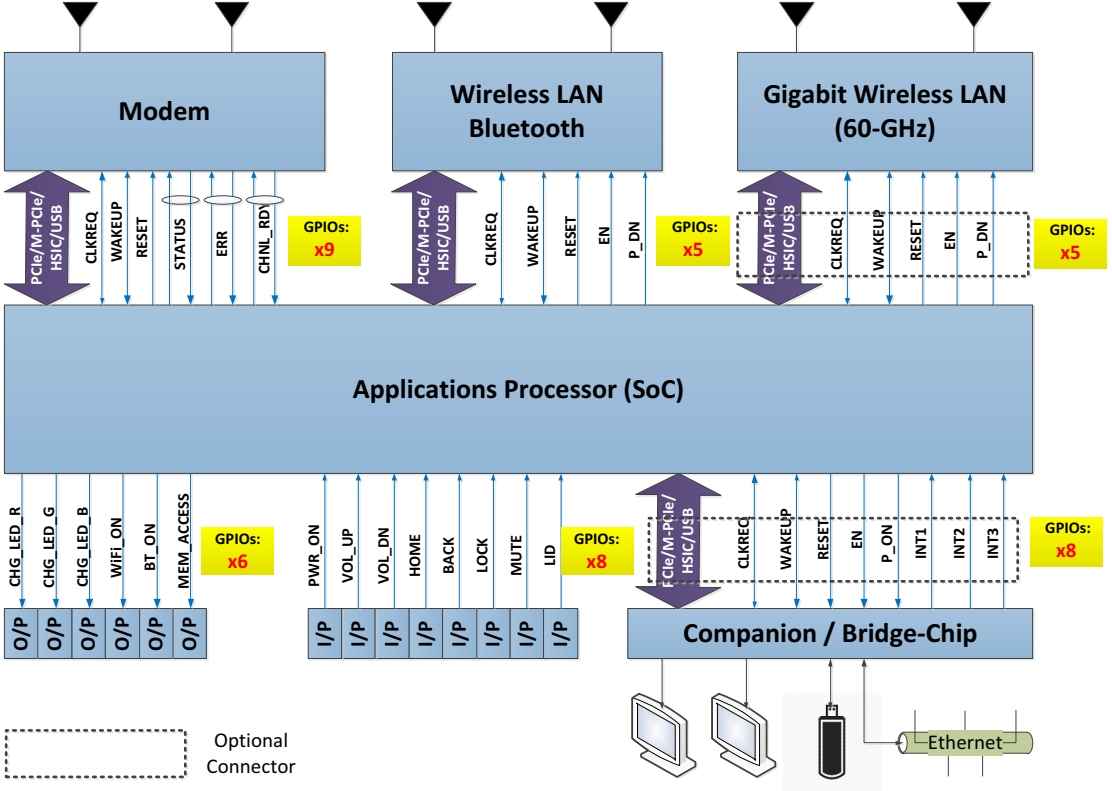
Docking

- Charging/audio/video ➔
  Productivity, Games and External Storage

Mobile Influenced

- Drones, IoT, Automotive, ….
- CAT-1 to CAT-3 Low-Power LTE Modem Support

The Problem of Sideband Proliferation

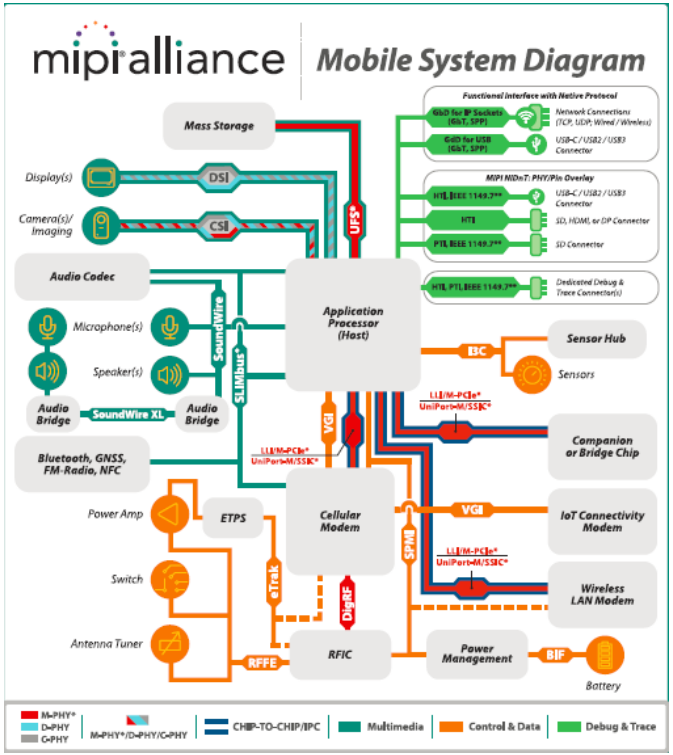


The Problem of Sideband Proliferation

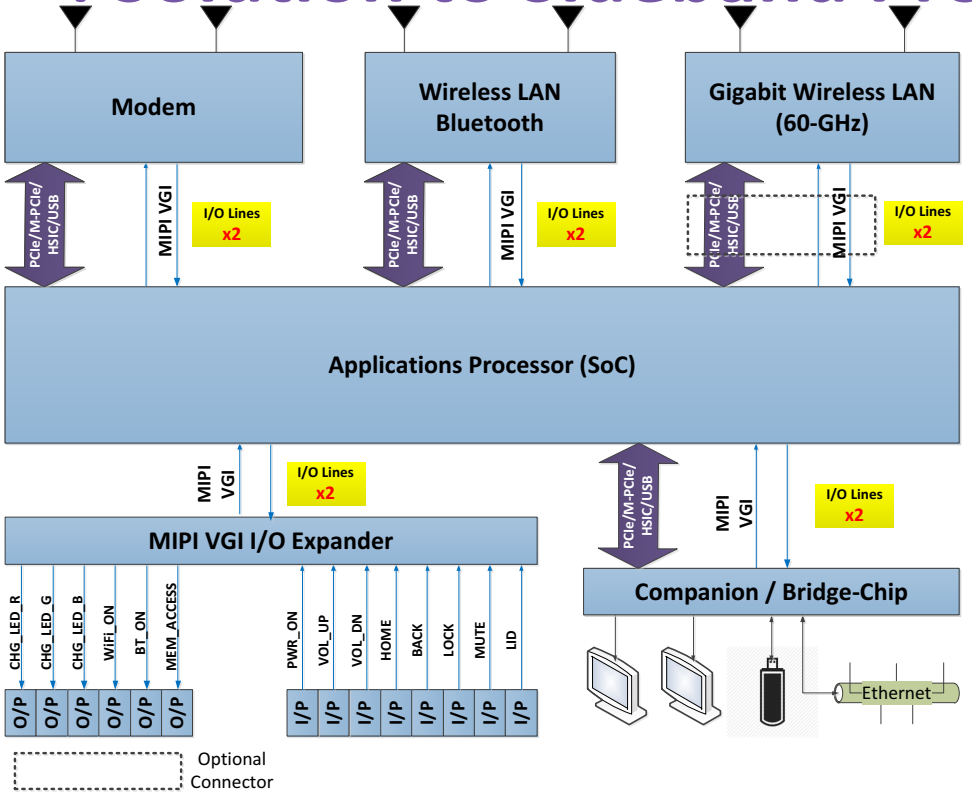
Typical Sideband Utilization

Domain	Number of Sideband I/O
Camera/Imaging	6 to 12
Audio CODEC	4 to 7
Cellular Modem	3 to 10
Wireless LAN Modem	3 to 10
Bridge Chip	3 to 8
Sensor Hub	4 to 18

Typical Sideband GPIOs: 23 to 65

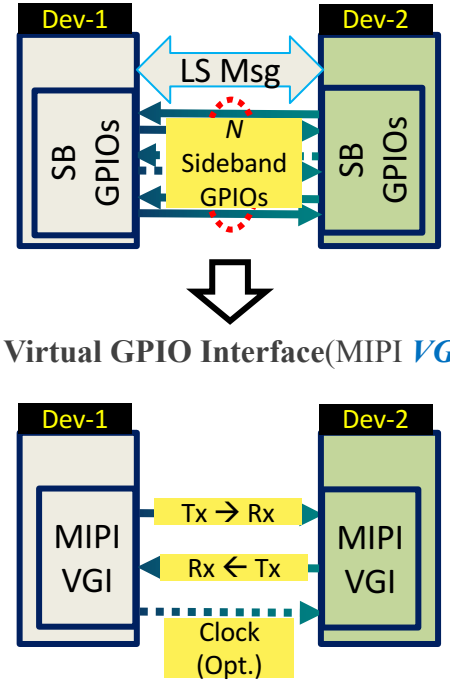


MIPI VGI℠: Solution to Sideband Proliferation



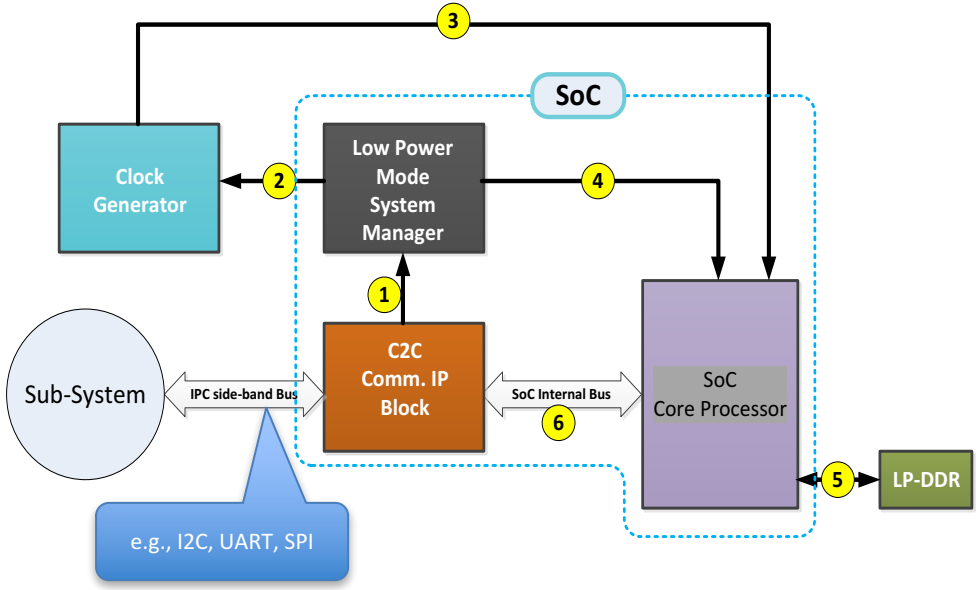
MIPI VGI℠: The Concept

- **MIPI VGI** consolidates ***N***-sideband GPIOs and sub-100 MHz serial messaging over **2** or **3** wire interface in a Point-to-Point configuration
- **2-wire MIPI VGI** : Asynchronous, Full-Duplex (4-Mbps max.)
- **3-wire MIPI VGI** : Synchronous, Full-Duplex
- **MIPI VGI Rev-1 (3-wire) Max Speed**: 76.8 MHz



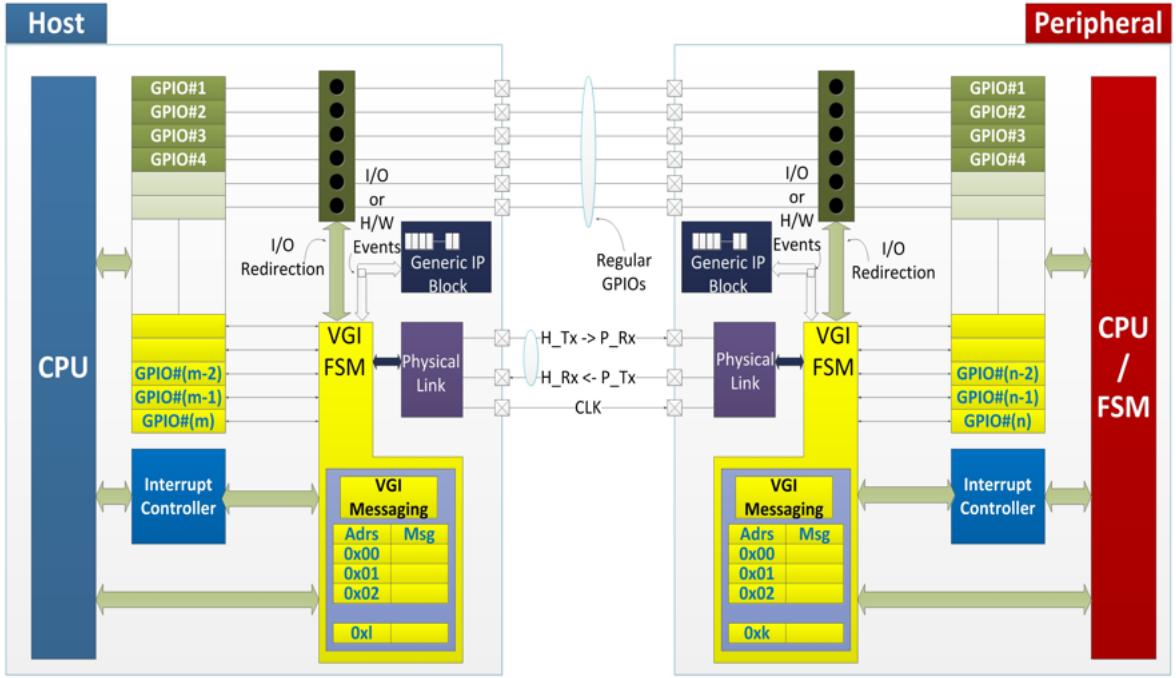
✓ **Consolidates Low Speed Messaging Interface and and Sideband GPIOs (N-pins to 2/3-pins reduction)**

Limitation of Conventional Techniques

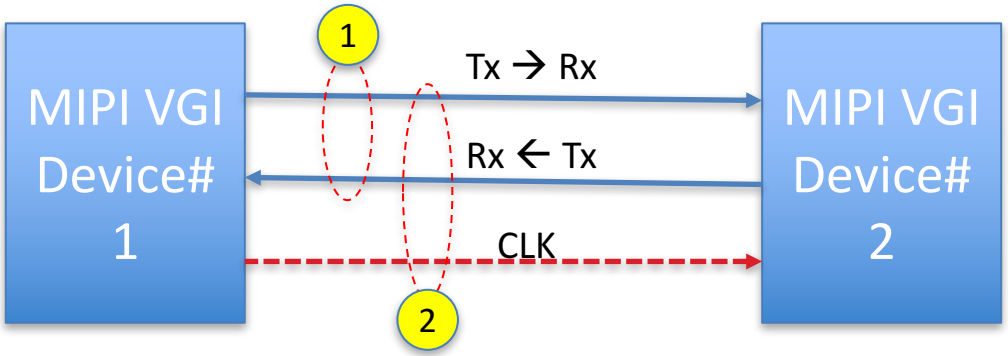


- ✓ HLOS processing latency varies widely
- ✓ Deep-sleep to active-state typical latency : Typically → 30 to 100-mS
- ✓ Timing uncertainty not suitable for the key IPC side-band signaling

MIPI VGI℠ Architectural Block-Diagram



MIPI VGI℠ Physical Interface: 2-wire or 3-wire



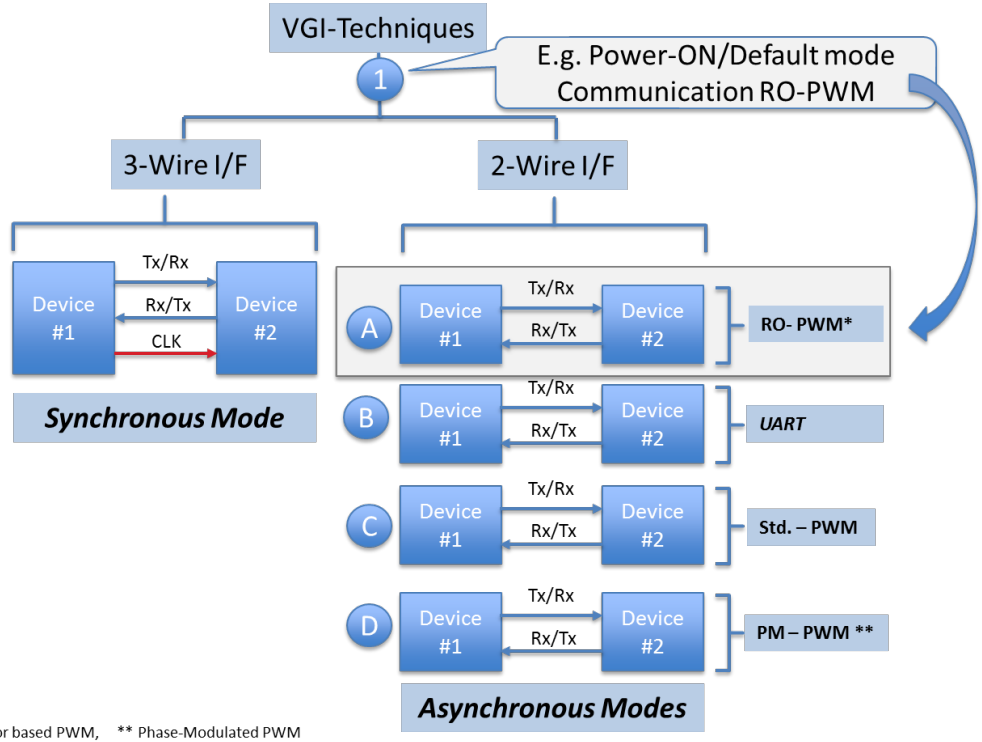
1 Asynchronous MIPI VGI

- Initial and Power State Transition mode communication over 2-wire, 4-Mbps max.

2 Synchronous MIPI VGI

- Common clock (Up to 76.8 MHz in VGI Rev-1)
- Sleep clock based operation supported in Low Power Modes

MIPI VGI[SM] Techniques At-a-Glance

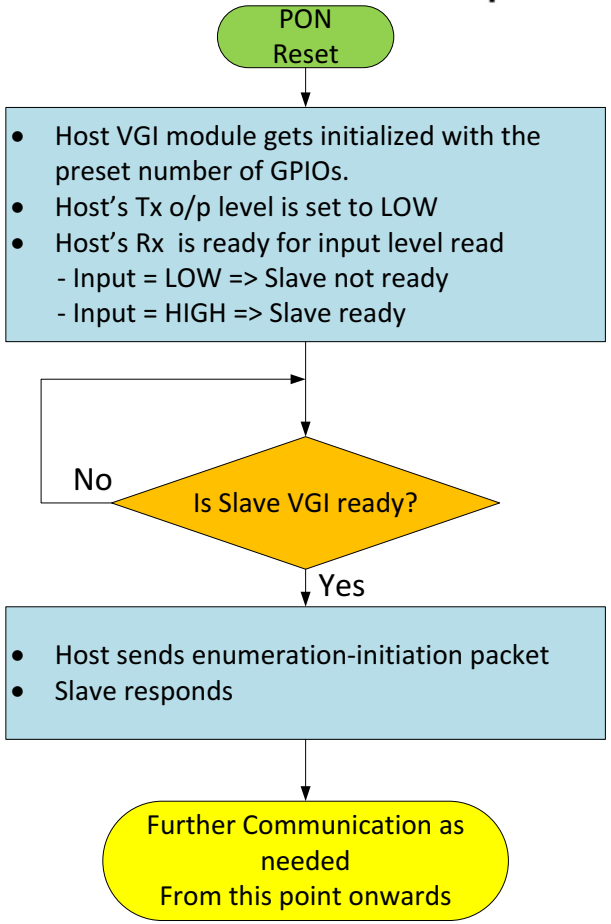


* Ring-Oscillator based PWM, ** Phase-Modulated PWM

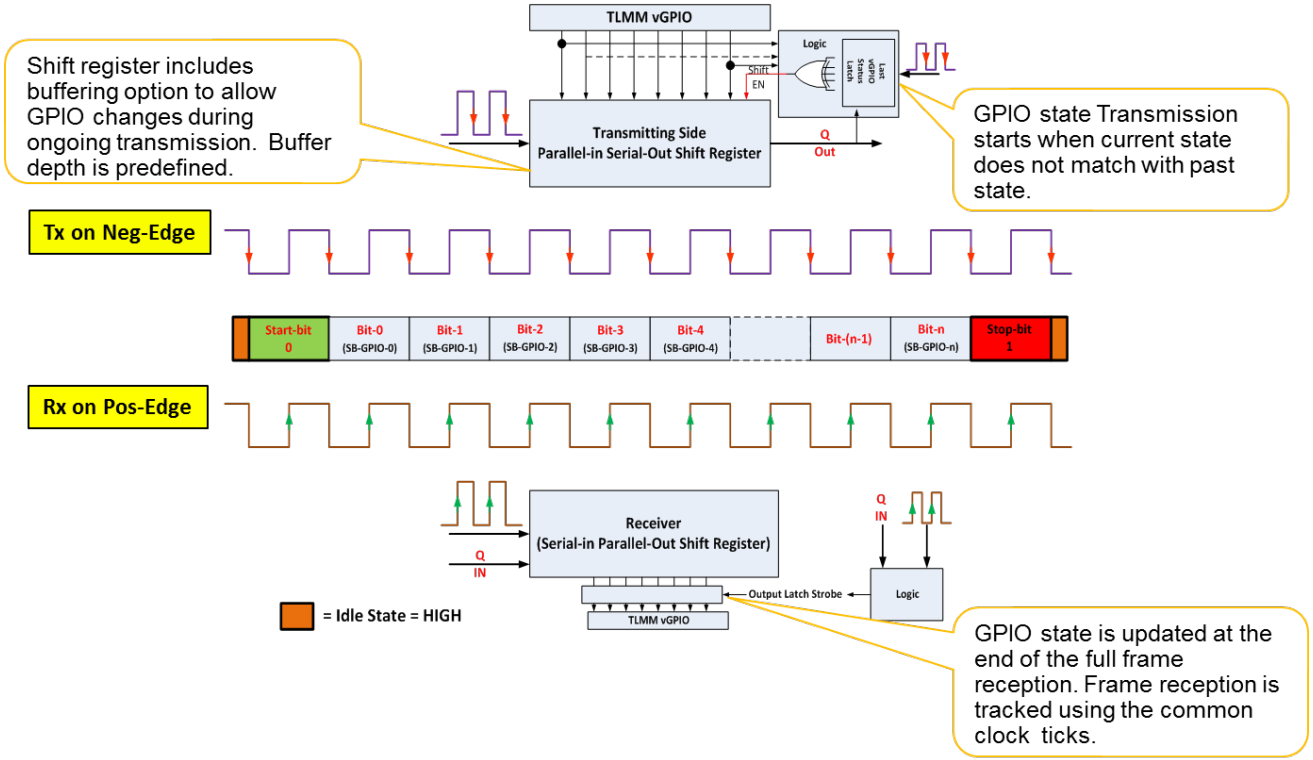
MIPI VGI℠ Roadmap

#	VGI Features	VGI v1.0	VGI Next
1	2-wire and 3-wire I/F support	✓	✓
2	Default PWM encoding	✓	✓
3	UART Encoding	✓	✓
4	PM-PWM Encoding (Phase-Modulated PWM)	-	✓
5	2-wire mode max throughput	4 Mbps	8 Mbps (PM-PWM)
6	3-wire mode max throughput	76.8 Mbps	153.6 Mbps
7	1.2V, 1.8V Operation support	✓	✓
8	1-wire mode support	-	✓

MIPI VGI℠ Init Sequence

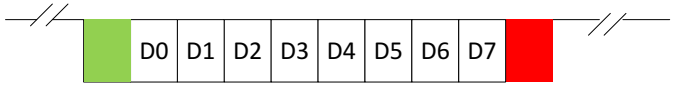


Synchronous 3-Wire MIPI VGI℠

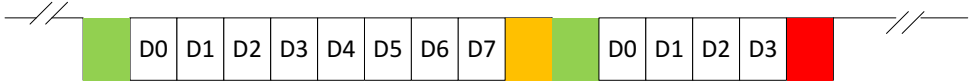


Asynchronous 2-wire MIPI VGI℠: *UART Mode*

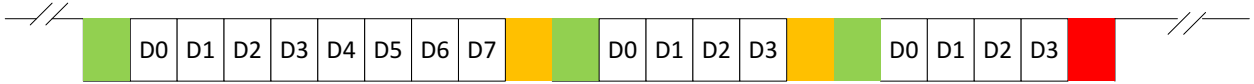
Illustration#1 : 8-bit frame



Illustration#2 : 12-bit frame

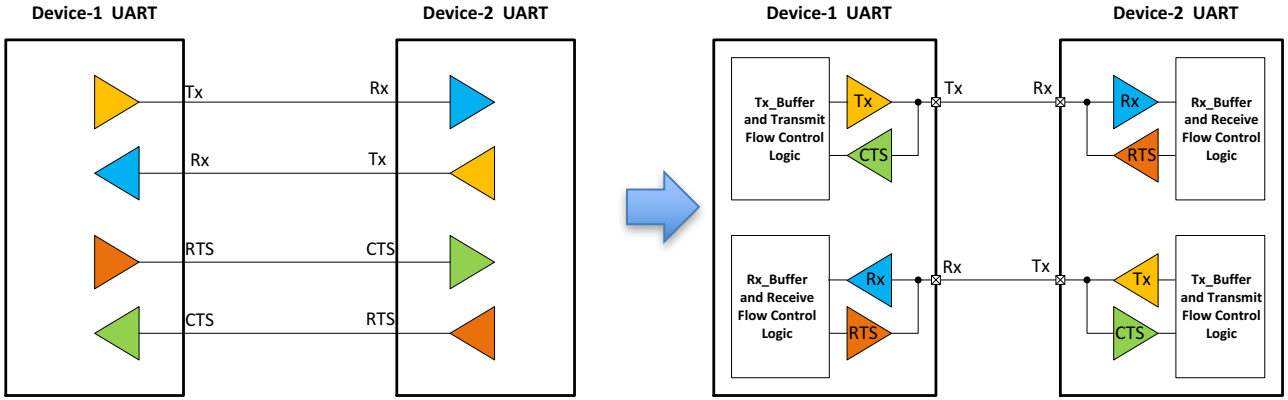


Illustration#2 : 16-bit frame

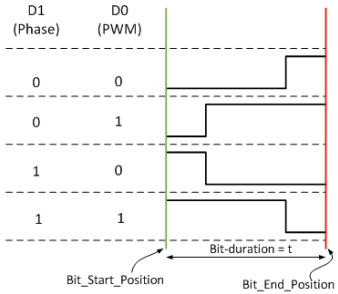


Asynchronous 2-wire MIPI VGI℠: *UART Mode*

H/W Flow Control over Tx/Rx eliminates RTS/CTS physical pins



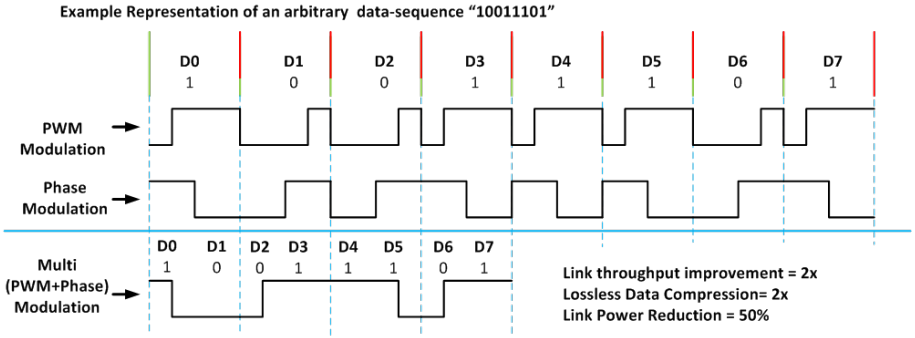
Asynchronous MIPI VGI[SM]: *Phase-Modulated PWM*



Symbol to signal mapping for a joint (PWM+Phase) modulation scheme

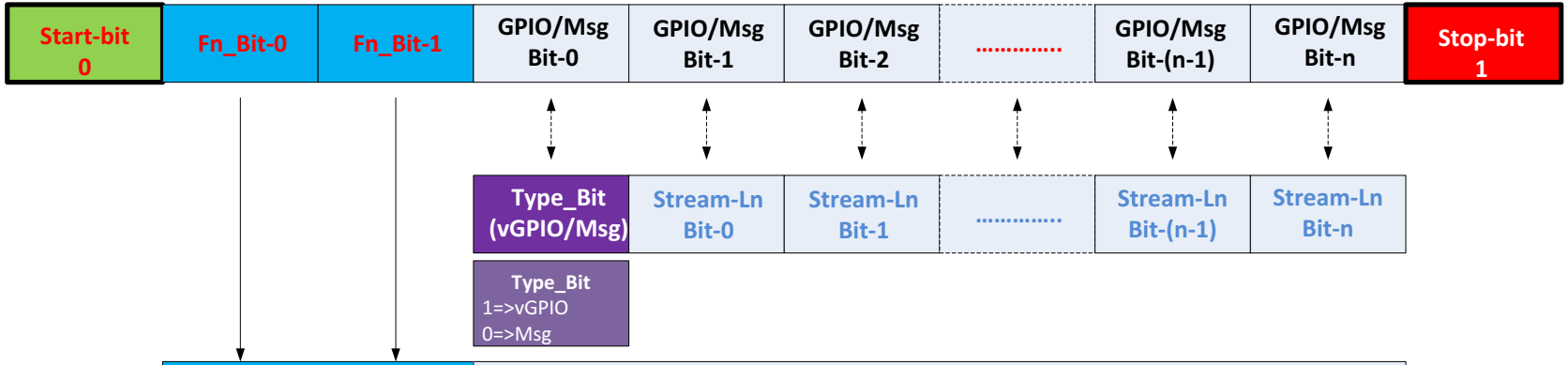
Highlights:

- All Digital Solution
- 2x Throughput
- Time-domain data compression
- Link power Reduction by 50%



Link throughput and power :: A comparative look

MIPI VGI[SM] Protocol

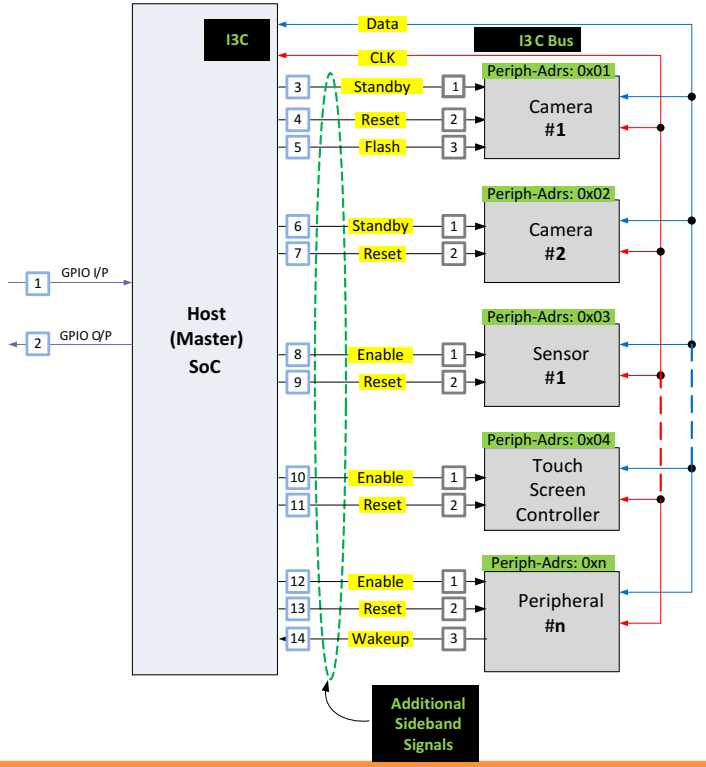


Function_Bits		Description
0	0	Following bits are vGPIO states
0	1	Following bits are message bits.
1	0	Following bit-stream represent the vGPIO stream length to be set on the receiver side.
1	1	Following bit-stream represent the new vGPIO stream length acknowledgement w.r.t the previously received stream-length programming command.

NOTE: The mechanism has a fixed overhead of two-bits over the base-line vGPIO implementation.

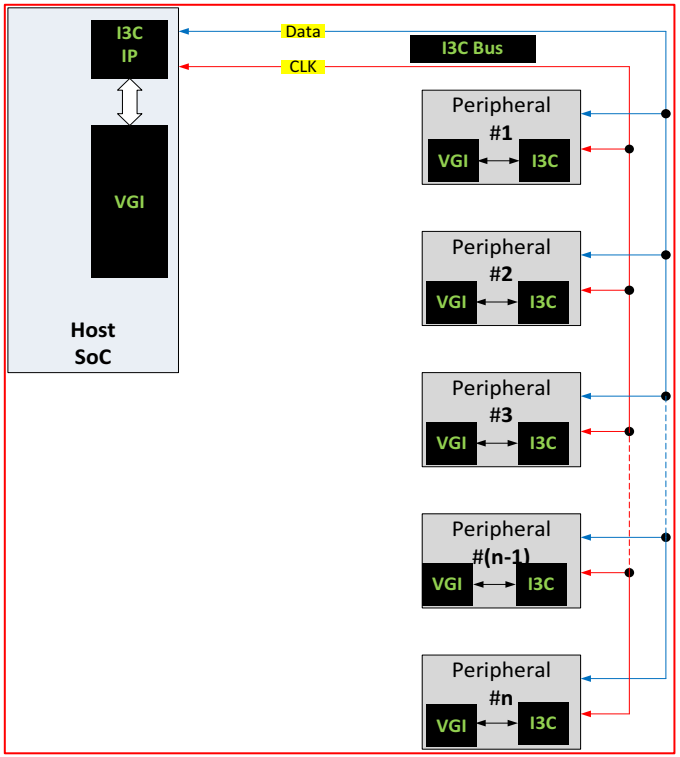
MIPI VGI℠ FSM Integration with MIPI I3C℠

- VGI FSM could be integrated with a serial interface of choice, such as MIPI I3C(SM)
- I3C(SM) supports MIPI VGI integration through dedicated Common Command codes (CCC) support in I3C(SM) v1.0
- Helps reduce Hardware event pins at system level



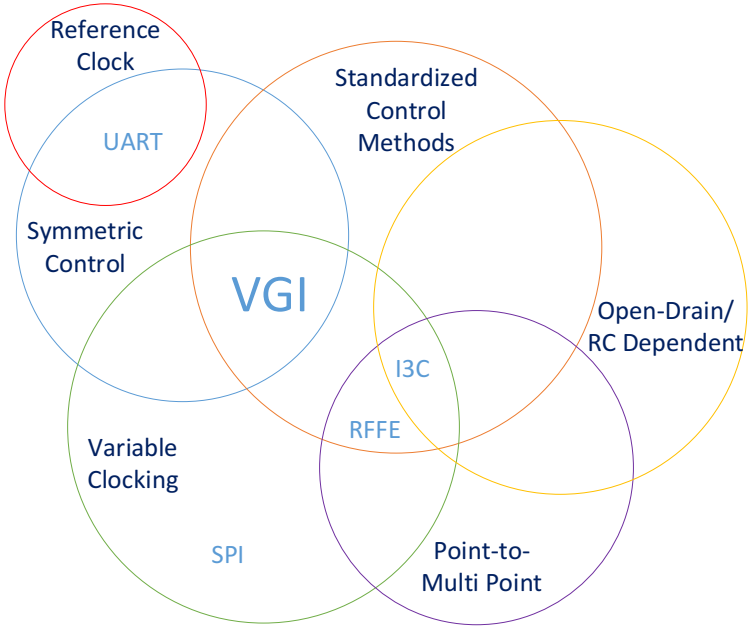
MIPI VGI[SM] FSM Integration with MIPI I3C[SM]

- HW Event sideband signals are eliminated
- VGI-FSM (Finite State Machine) performs I3C[(SM)] message encoding/decoding for HW events and thus frees up the associated CPU on the host-SoC for these tasks.
- Impact is reduced Latency and Power consumption.



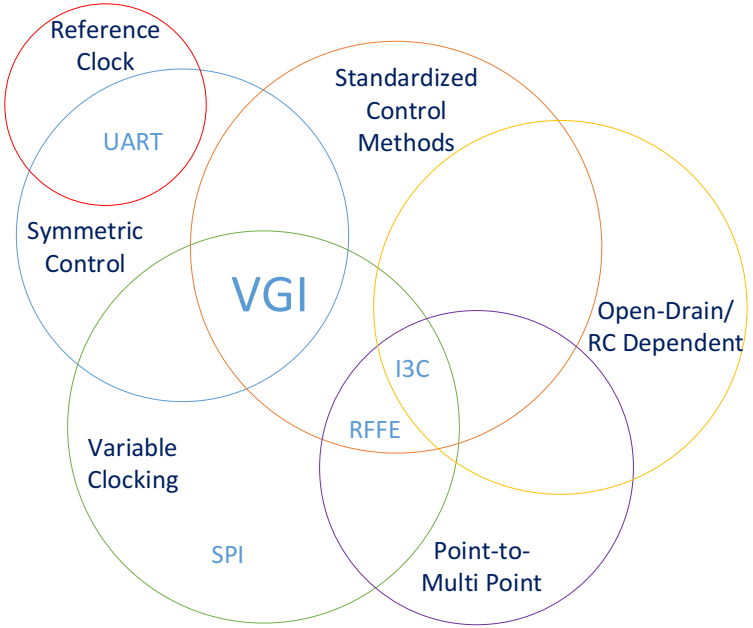
Comparing MIPI VGI℠

- **SPI**
  - Master-Slave approach
  - Custom implementations, no common methods
- **MIPI I3C℠**
  - Multi-Master Multi-Slave, Open-Drain approach
  - In-band interrupts
- **MIPI RFFE℠**
  - Master-Multi Multi-Slave approach
- **UART**
  - Custom implementations, requires reference clocks
- **MIPI VGI℠**
  - Symmetric control approach (No Master No Slave)
  - Initialization from either side

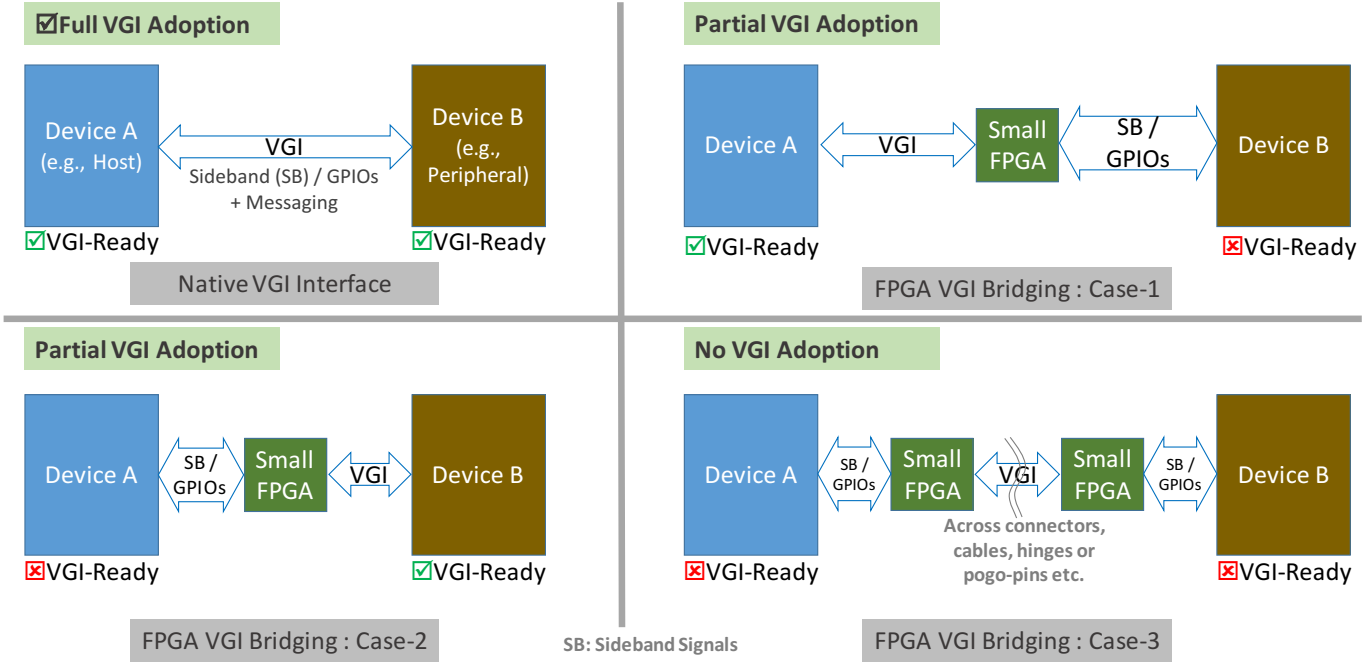


Comparing MIPI VGI[SM] - Clocking

- **UART**
  - Requires Reference Clock with Agreed rates
- **SPI, MIPI I3C[(SM)] , MIPI RFFE[(SM)]**
  - Clock is forwarded from Master to Slave
- **MIPI VGI[(SM)]**
  - Using RO-PWM PHY option, the clocking is forwarded with data
  - Only Transmitter requires clock to create telegrams
  - Receiver captures telegrams without internal clock
    - Useful for devices which power down
    - Useful for very simple write-only devices (LED bank)



Phased MIPI VGI℠ Adoption – Leveraging Smaller FPGAs



Summary

- Sideband GPIOs add to SoC and PCB level cost and complexity
- MIPI VGI consolidates sideband GPIOs and Low-Speed serial messaging interface in P2P configuration to reduce I/O pins
- Both 2 and 3-wire interface options are available
- Common PWM start-up mode ensures interoperability
- The VGI FSM can be combined with any other interface bus of choice, e.g. I3C$^{(SM)}$ VGI
- The MIPI VGI Specification is to be released in 2018


mipi®
DEVCON
THANK YOU
2017
MIPI ALLIANCE
DEVELOPERS
CONFERENCE
HSINCHU CITY, TAIWAN
MIPI.ORG/DEVCON