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DEVCON

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Synopsys

Driving 4K High-Resolution Embedded Displays in New Applications with MIPI DSI℠ and VESA DSC (Synopsys & Arm)

2017
MIPI ALLIANCE
DEVELOPERS
CONFERENCE

HSINCHU CITY, TAIWAN
MIPI.ORG/DEVCON

Agenda

- Rising demand for high resolution displays
- Arm® Mali®-Cetus Display processor
- Synopsys® DesignWare® MIPI DSI℠ Host Controller with VESA DSC Encoder
- Synopsys & Arm solution

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Bandwidth Demand Increases for Embedded Displays

Meets the demands of vivid, detailed and immersive visual experience

- Mobile:
  - More powerful GPU, higher resolution cameras, richer content with high resolution and better visual quality drives the demand for mobile devices having a better displays.
- VR/AR:
  - Virtual reality application requires displays with not only high resolution but high refresh rate
- Automotive:
  - Dashboard/infotainment/mirrorless system displays with customized high resolutions and details demands bandwidth increases

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Arm Mali Display Overview

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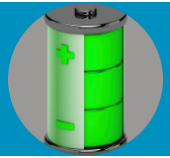
Arm Mali Display in Arm Multimedia Subsystem

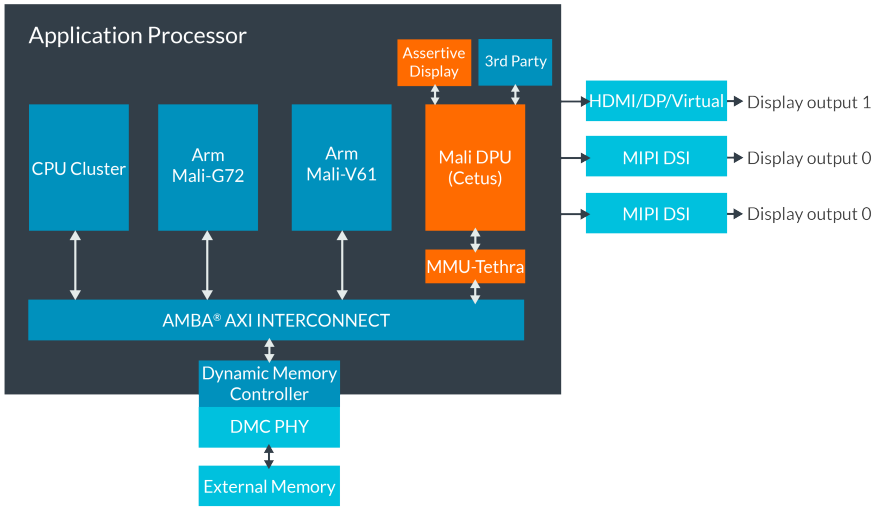
Feature Rich:
- Composition, scaling, rotation
- gamma correction, colour management,
- co-processor interface, dual-display

Low power real-time performance:
- Single pass composition, Arm Frame Buffer Compression (AFBC), Optimized SMMU integration



Optimized software support:
- Android DDK
- Linux KMS
- Arm Mali Multimedia Suite

Supports all major display industry standards:
- MIPI, HDMI, VESA, CEA-861, ITU-R



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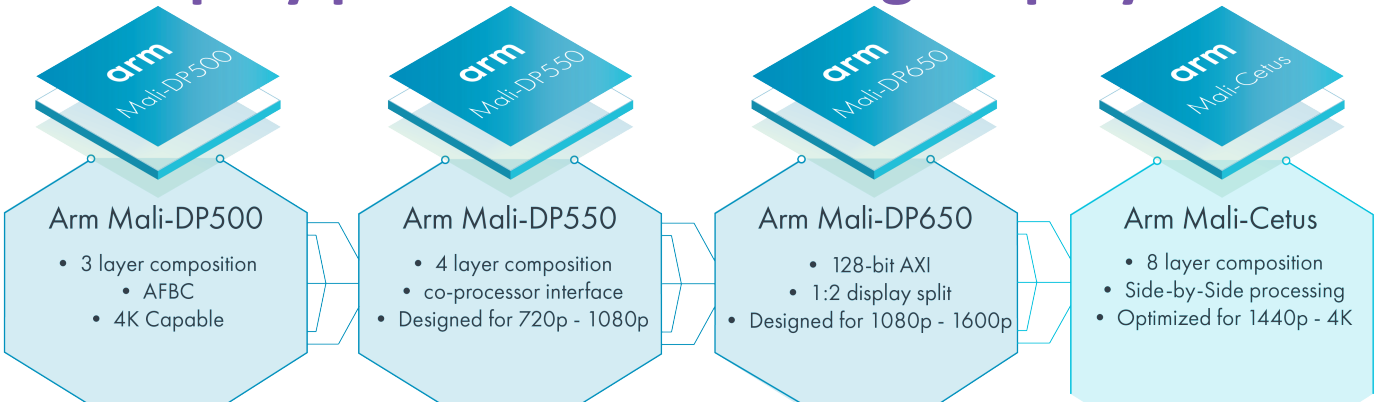
Arm Mali Display processors - Driving Display Technologies



First architecture was designed for 1080p60, 1440p60, 1600p60 mobile/tablet displays

New architecture needed to address:

- Higher performance requirements (up to 4K120fps) driven by VR
- Quad scaling and more layers for Android N+ multi-window use case
- Power and quality optimizations for growing variety of panel and systems
- Composition for new disruptive UHD content (HDR10, HLG)

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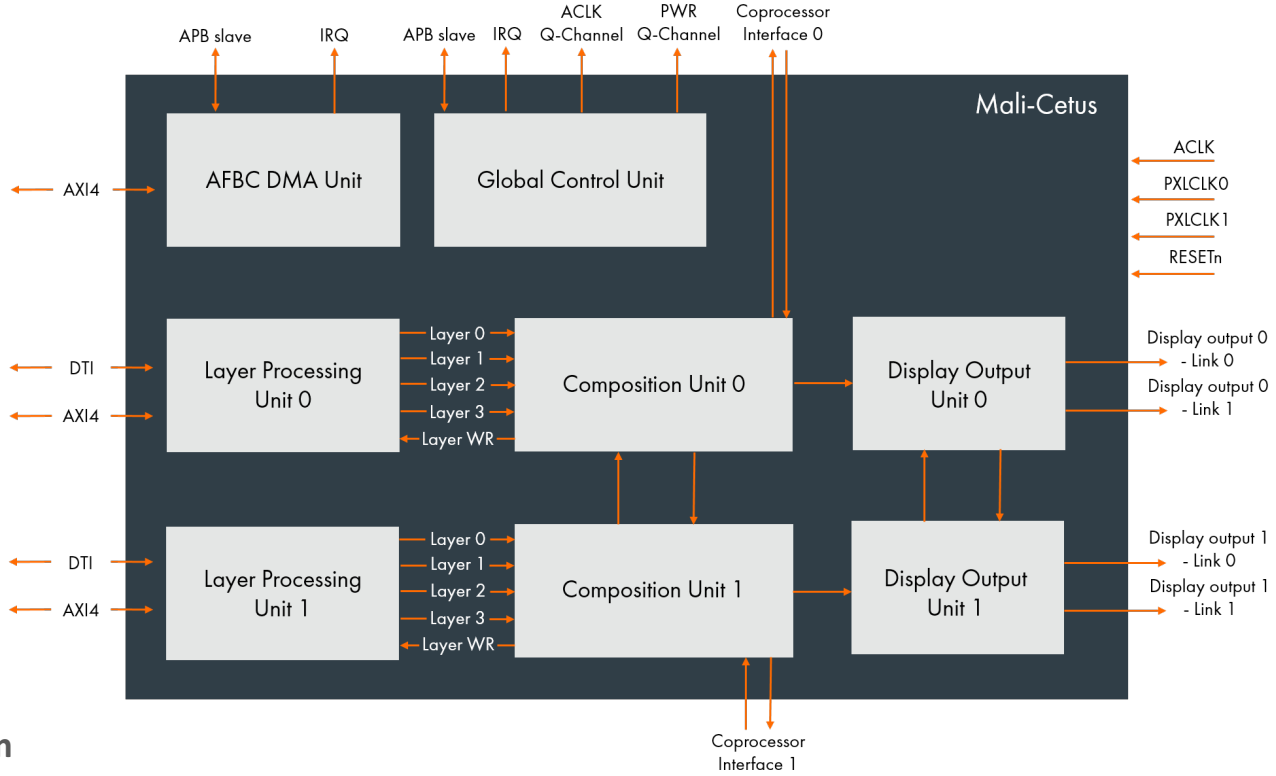
Arm Mali-Cetus Architecture Overview



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Better Android Window Composition Capabilities

- Support for multi-window sessions in Android N
  - Optimized HWC Solver
- 8 composition layers when driving a single display
  - 4 layers per display output for dual display
- 4 scaled layers when driving a single display
  - 2 scaled layers per display output when driving a dual display
- Simultaneous layer + pixel alpha blending
  - Ideal for window animations
- Fully flexible and software programmable Z order

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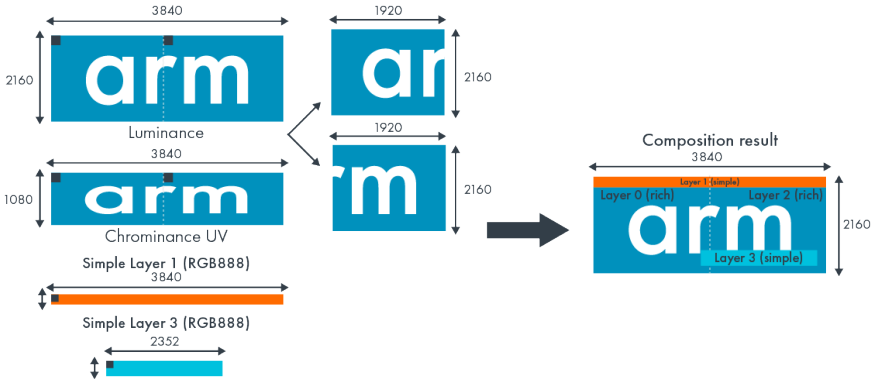
Flexible Use of Display Processor Resources

- Software Layer Split and Layer Merge
- Software layer split and internal layer split of display layers with 2 scaling engines to optimize demanding downscaling use cases

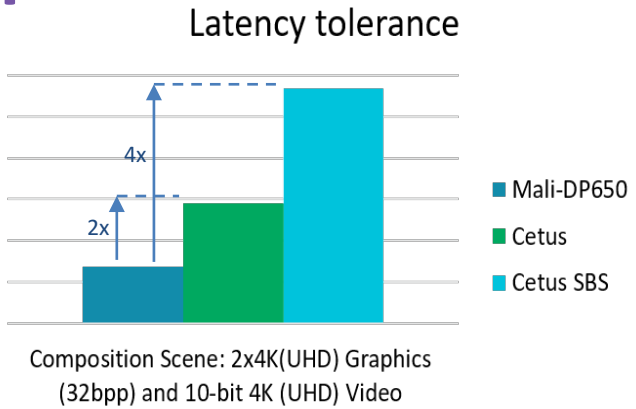


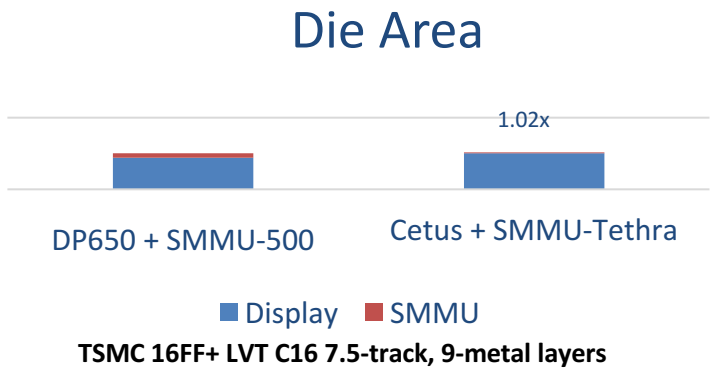
- Side by Side Processing
- Side-by-side processing for low voltage operation at 4Kp60-120fps

Performance, Area Comparison

Additional functionality in Cetus

- 8 composition layers (vs 4 in DP650)
- Side-by-side processing
- Scaling split
- Uncompressed rotation removed from the real time path
- Higher AFBC decoder throughput
- Reduction of MMU latency





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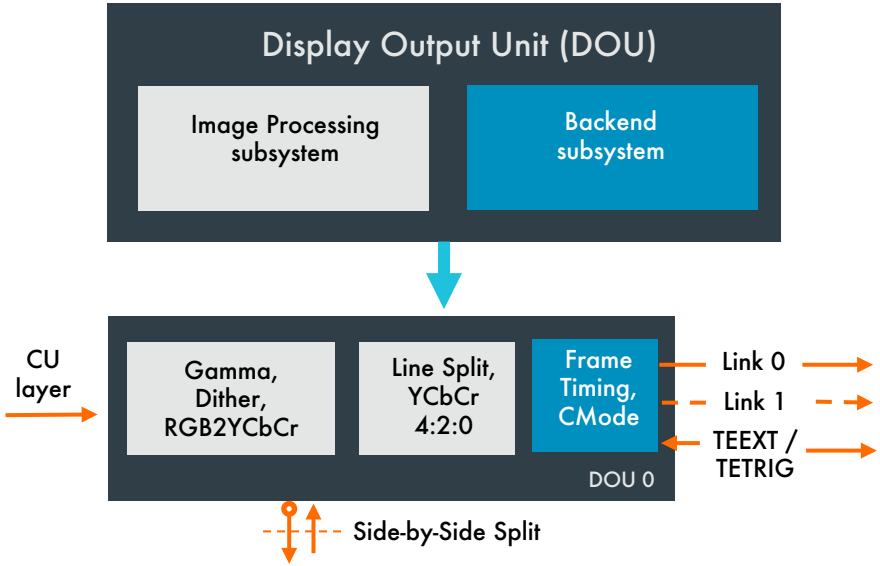
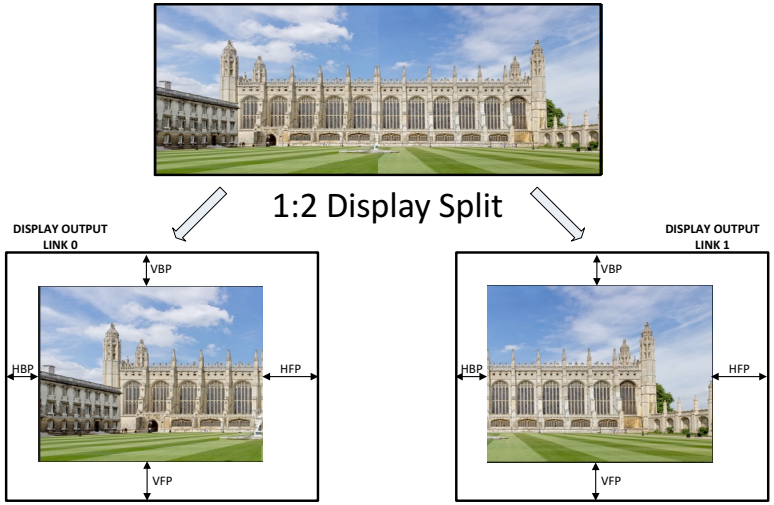
Display Output Unit

Backend Subsystem





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Synopsys & Arm Display Solution

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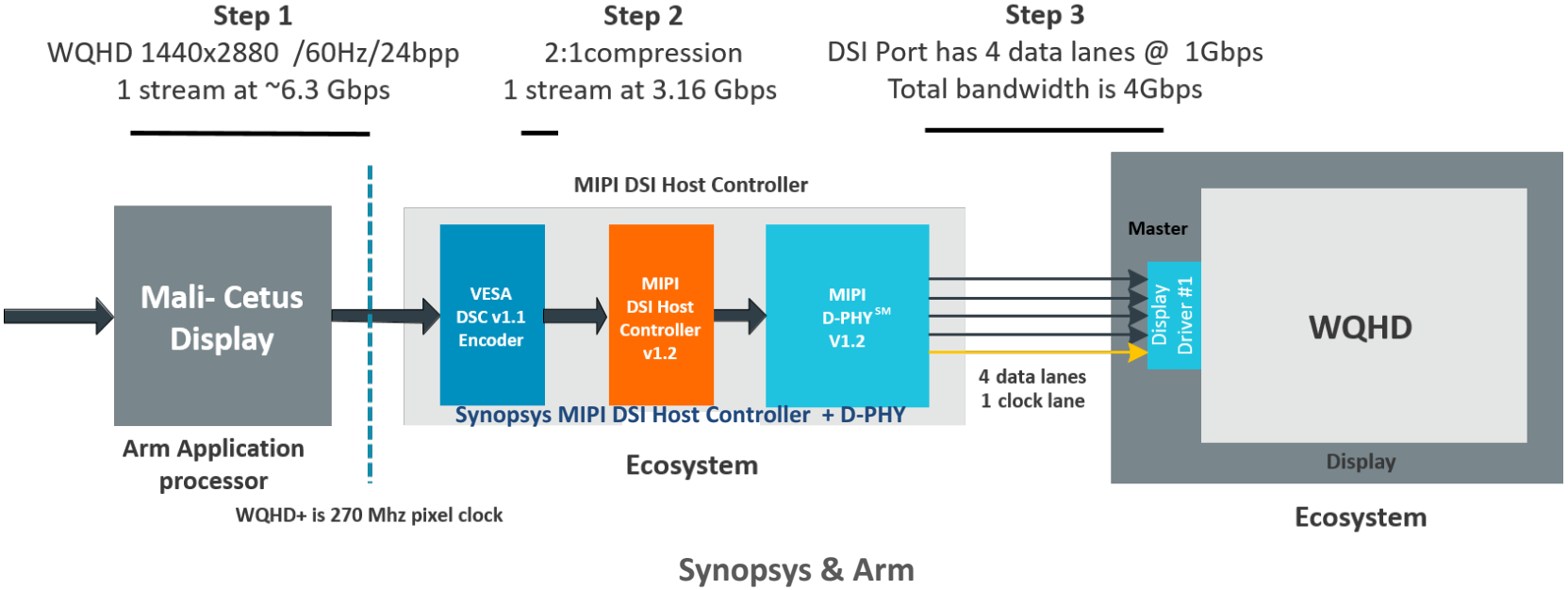
Today's Premium Smartphone

- Smartphone application – WQHD+



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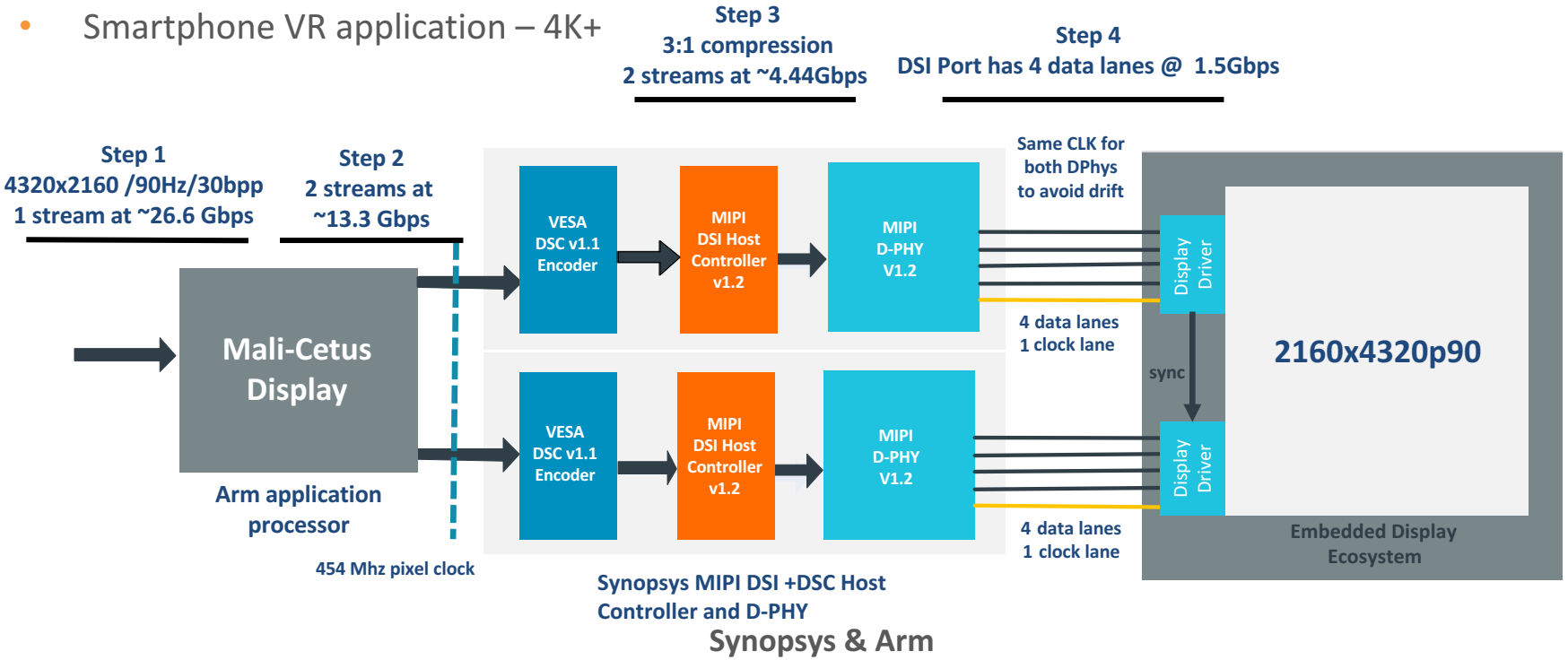
AR/VR and Future Premium Smartphone

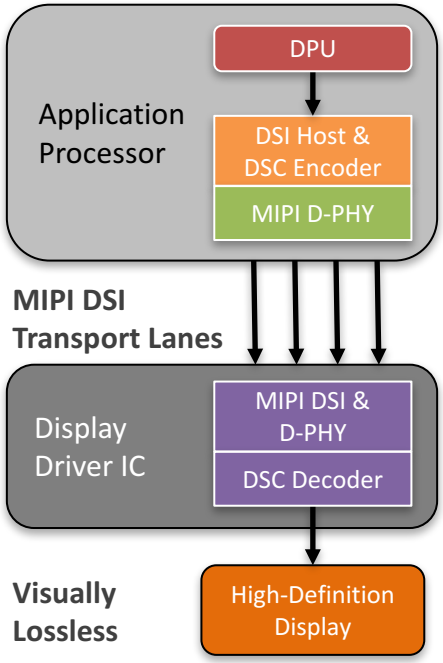
- Smartphone VR application – 4K+



VESA Display Stream Compression (DSC)

Enabling UHD mobile displays

- Visually lossless compression
  - Optimized for compression factor between 2x and 3x
- Intra-frame Constant Bit Rate (CBR) encoder
- Support 8, 10 and 12 bits per component
- RGB and YCbCr 4:4:4
- Based on Delta Pulse Code Modulation (DPCM) with an Indexed Color History (ICH)
- Requires a single line of pixel storage & rate buffer



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DSC with Proven MIPI Specifications

Resolution	Bandwidth	MIPI D-PHY v1.1 @ 1.5Gbps			MIPI D-PHY v1.2 @ 2.5Gbps		
		No compression	2x compression	3x compression	No compression	2x compression	3x compression
FHD (1080x1920)	3.58 Gbps	3 lanes	2 lanes	1 lane	2 lanes	1 lane	1 lane
WQHD (1440x2560)	6.37 Gbps	6 or 8 lanes	3 lanes	2 lanes	3 lanes	2 lanes	1 lane
WQXGA (1600x2560)	7.08 Gbps	6 or 8 lanes	3 lanes	2 lanes	3 lanes	2 lanes	2 lanes
UHD (2160x3840)	14.33 Gbps	N/A	6 or 8 lanes	4 lanes	6 or 8 lanes	3 lanes	2 lanes
WQUXGA (2400x3840)	15.93 Gbps	N/A	6 or 8 lanes	4 lanes	8 lanes	4 lanes	3 lanes
5K (2880x5120)	25.49 Gbps	N/A	N/A	8 lanes	N/A	6 or 8 lanes	4 lanes
8K (4320x8192)	61.16 Gbps	N/A	N/A	N/A	N/A	N/A	N/A

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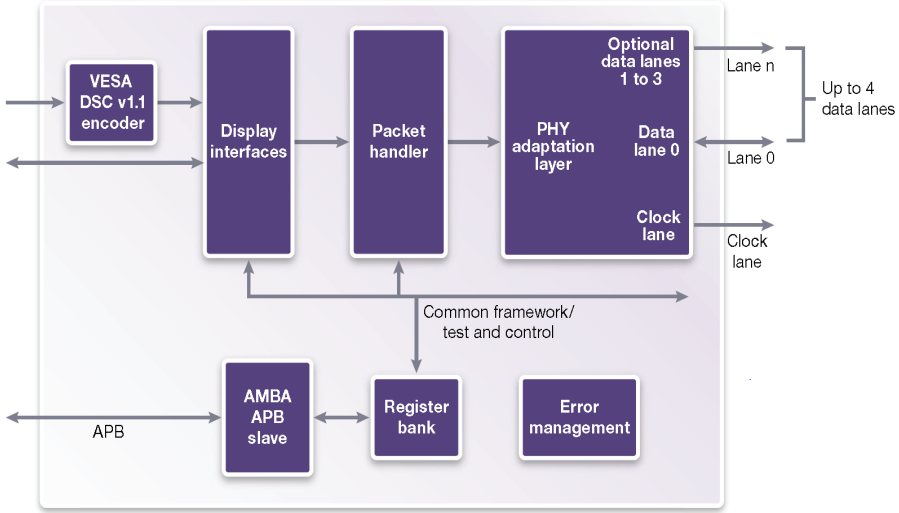
Synopsys MIPI DSI Host Controller with VESA DSC 1.1

Fully integrated, cost-efficient solution to enable supporting ultra-high resolutions MIPI displays

- Complete DesignWare MIPI DSI Host Controller with VESA Display Stream Compression encoder and MIPI D-PHY easily integrates into application processors with less risk
- Integrated MIPI display IP reduces memory size and data transmission bandwidth to lower power consumption, area as well as EMI
- VESA DSC encoder allows higher refresh rates beyond 60Hz for drastically faster responsiveness and fluidity in ultra-high-resolution quad HD or 4K displays



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Integrating MIPI DSI + VESA DSC

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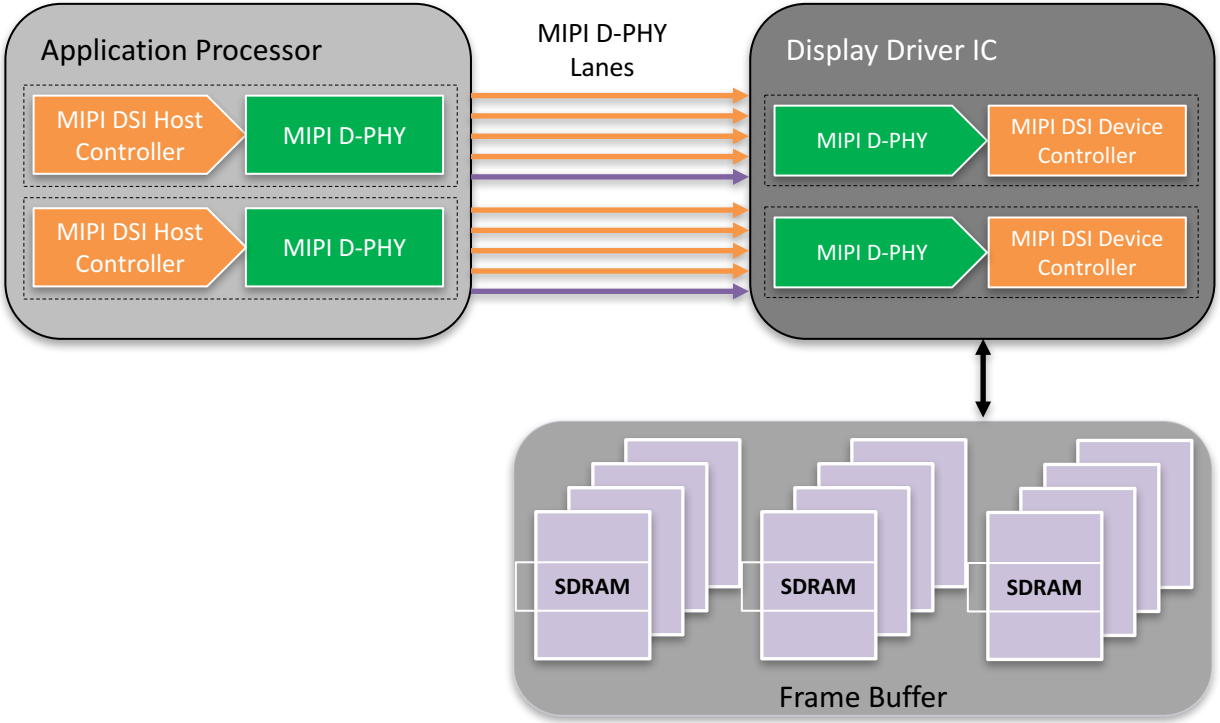
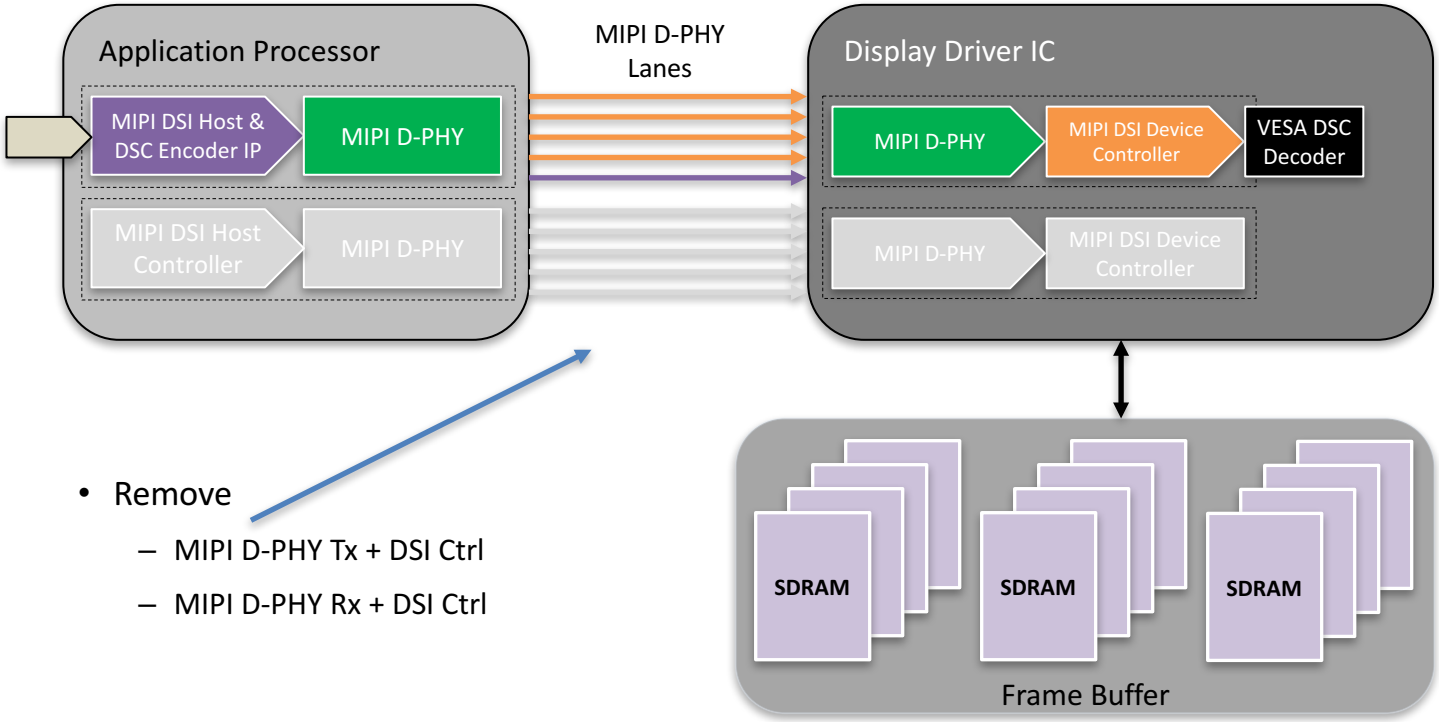
Dual DSI Without DSC



Remove DSI/D-PHY with Integrated DSI/DSC IP

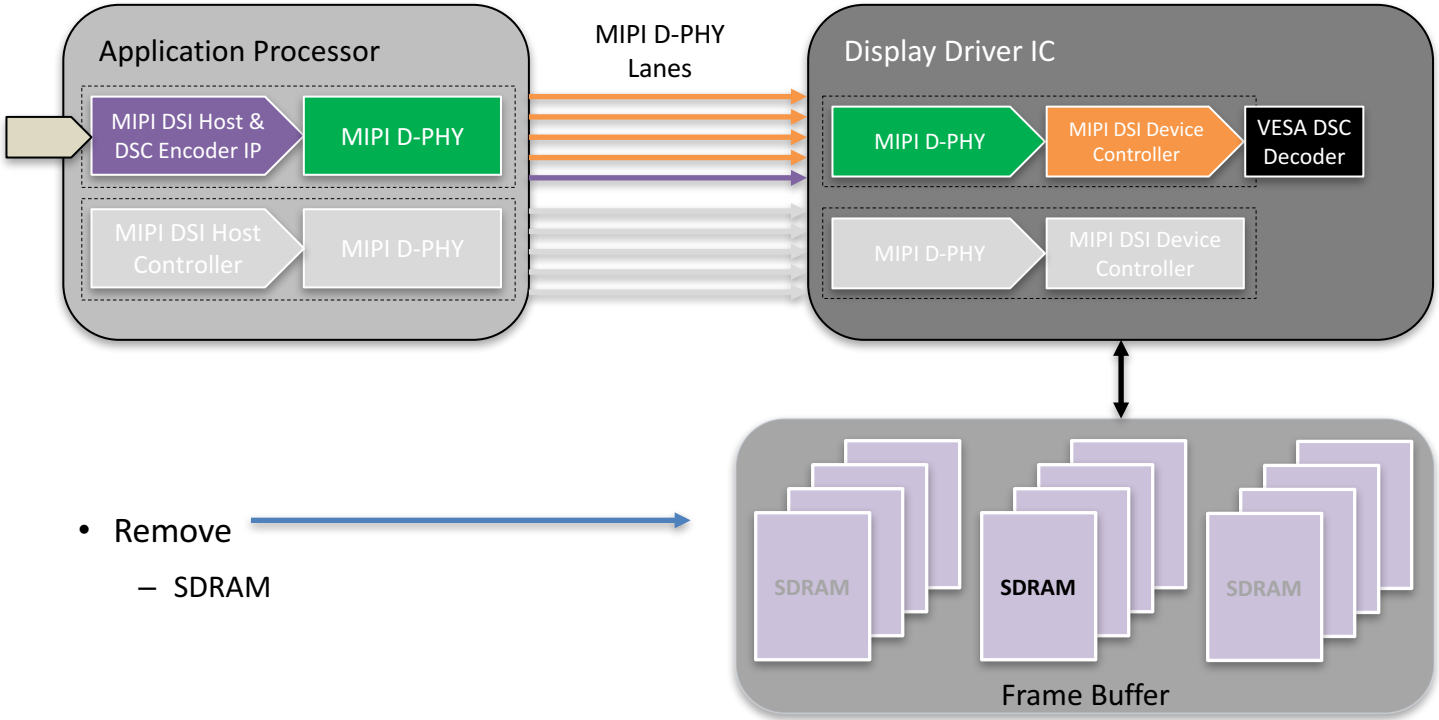
Save Power, Area & Cost



- Remove
  - MIPI D-PHY Tx + DSI Ctrl
  - MIPI D-PHY Rx + DSI Ctrl

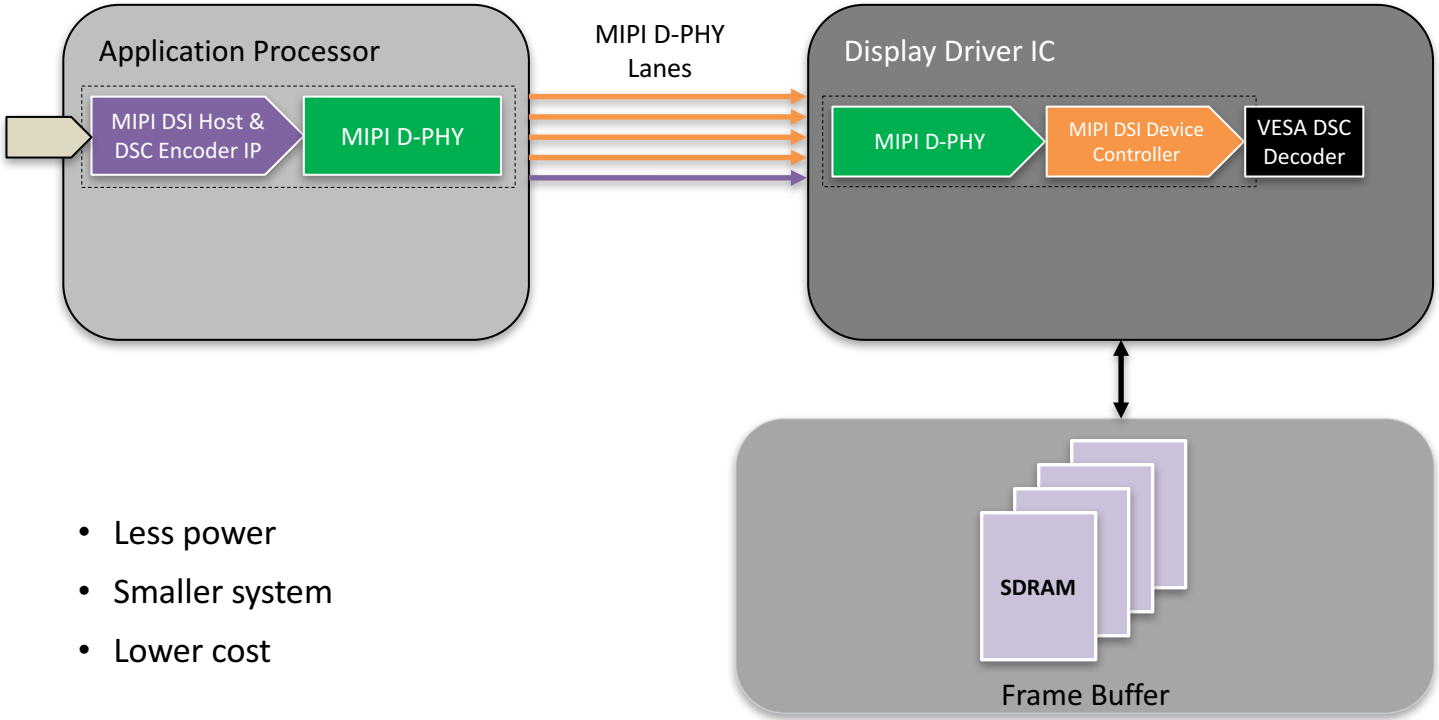
Remove SDRAMs with Integrated DSI/DSC IP

Save Power, Area & Cost



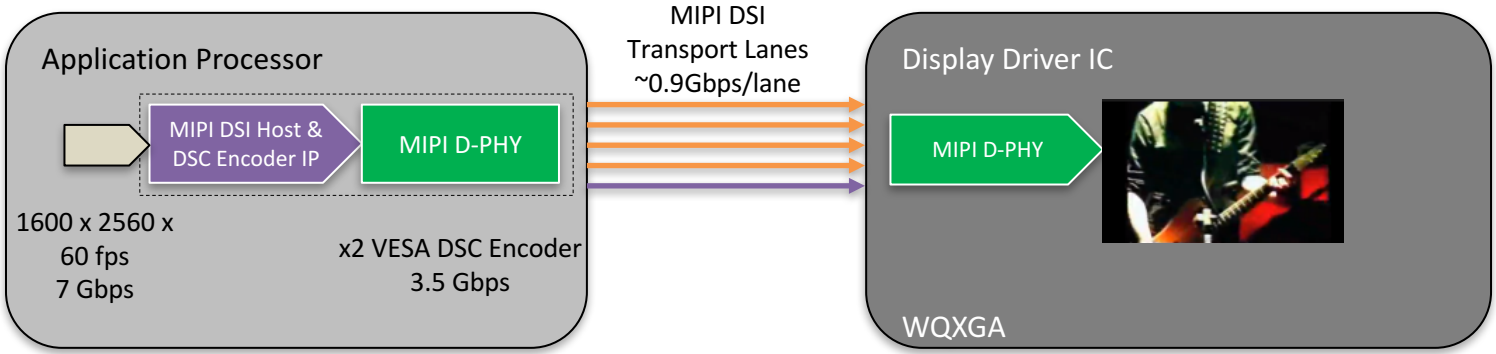
- Remove
  - SDRAM

Save Power, Area and Cost with Scalable Architecture



- Less power
- Smaller system
- Lower cost

Enabling Challenging COG Connectivity



- Chip-on-Glass (COG) offers a thin profile, integrated display
  - At the same time has limitations in supporting high-switching frequencies
- VESA DSC Encoder IP reduces data transmission bandwidth
- Allows use of existing lower switching-speeds for higher-resolution displays

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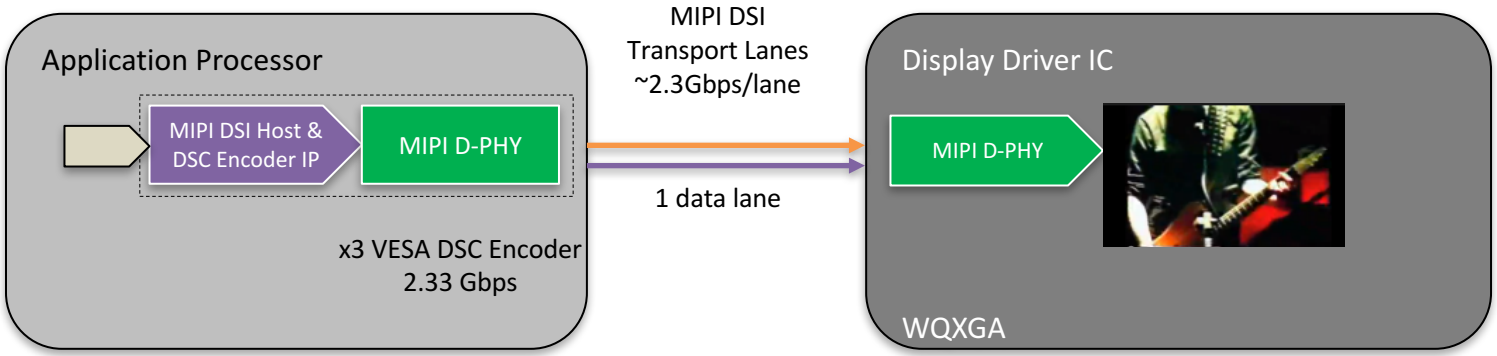
Reducing Number of Pins with D-PHY v1.2



- D-PHY v1.2 is getting adopted widely which enable 2.5Gbps/lane
- VESA DSC Encoder IP reduces data transmission bandwidth
- Allow drastic reduction in # of pins and power consumption
- D-PHY v1.2 capable design enables system flexibility

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Summary

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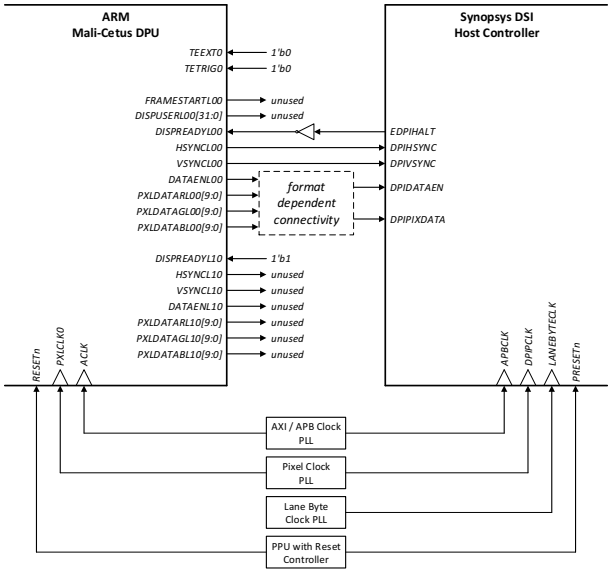
Arm/Synopsys Provide Detailed Integration Guidelines

- Interface connectivity, clock and reset control
- Pixel data transfer in MIPI DSI Video Mode for both single and dual link
- Variable refresh rate in MIPI DSI Video Mode
- Synopsys eDPI interface and MIPI Command Mode operation
- Pixel data transfer in MIPI DSI Command Mode for both single and dual link
- Dynamic resolution change
- Partial update
- VESA Display Stream Compression (DSC) encoder integration
- Power control



Example: Arm Mali DPU and Synopsys DSI Host Controller utilizing DPI interface

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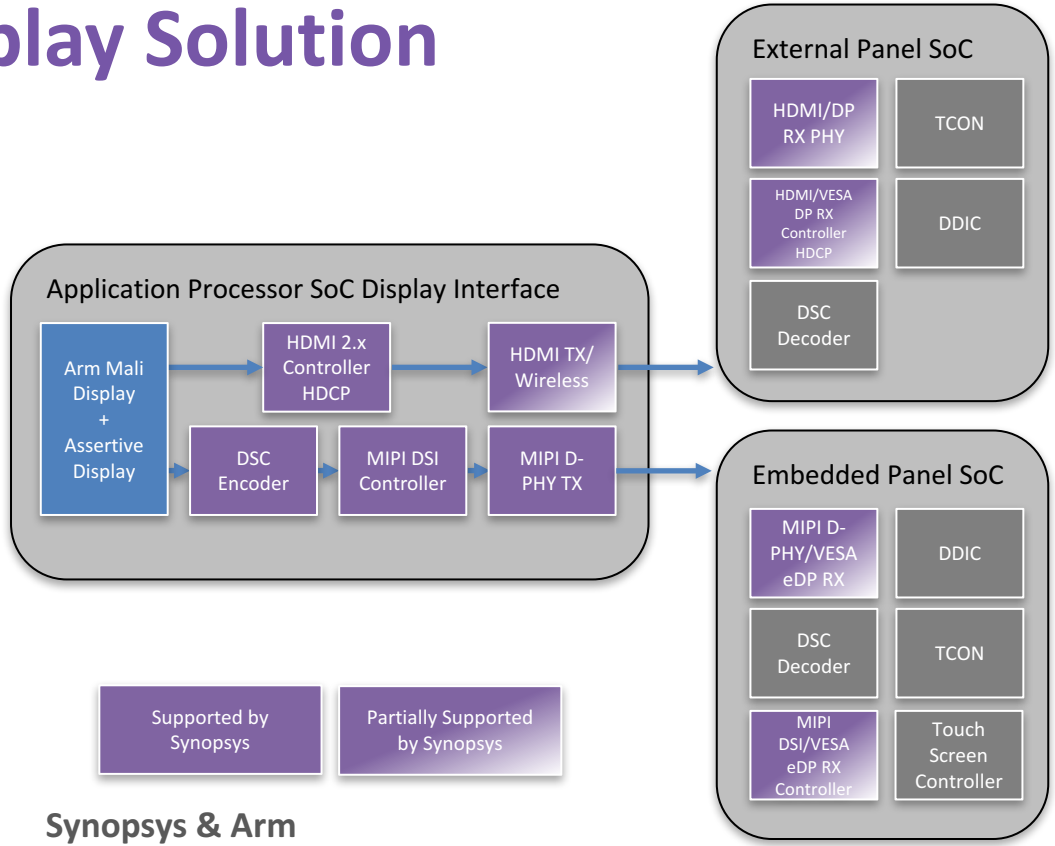
Synopsys & Arm Display Solution

- Arm and Synopsys ensure complete and optimized end-to-end display solutions
- Arm and Synopsys reduce the complexities of porting & integration between apps processor and PHYs
- Joint application note available to our partners upon request providing configuration and integration guidelines



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THANK YOU

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