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DEVCON

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Synopsys

Enabling Higher Data Rates and Variety of Channels with MIPI D-PHY℠

2017
MIPI ALLIANCE DEVELOPERS CONFERENCE

HSINCHU CITY, TAIWAN
MIPI.ORG/DEVCON

Agenda

- Design motivation
- MIPI D-PHY evolution
- Summary of MIPI D-PHY specification
- MIPI channel evolution
- Channel modeling results in ADS
- Specification run through for D-PHY v2.1
- MIPI D-PHY 3.0 approved roadmap

Design Motivation

- Higher data rate
- Adaption to newer technologies
- Longer channel length, channel evolution
- Backward compatible
- Reliable with sufficient margins
- Augmenting existing eco system
- Meeting camera and display present and future needs
- Growing market applications and segments
- The de-facto standard for camera and display
- Target automotive segment for ADAS applications

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MIPI D-PHY Evolution

- D-PHY 1.0 1.0 Gbps
- D-PHY 1.1 1.5 Gbps
- D-PHY 1.2 2.5 Gbps
- D-PHY 2.0/2.1 4.5 Gbps
- D-PHY 3.0 10-14 Gbps

Higher data rate enables high pixel count cameras and displays

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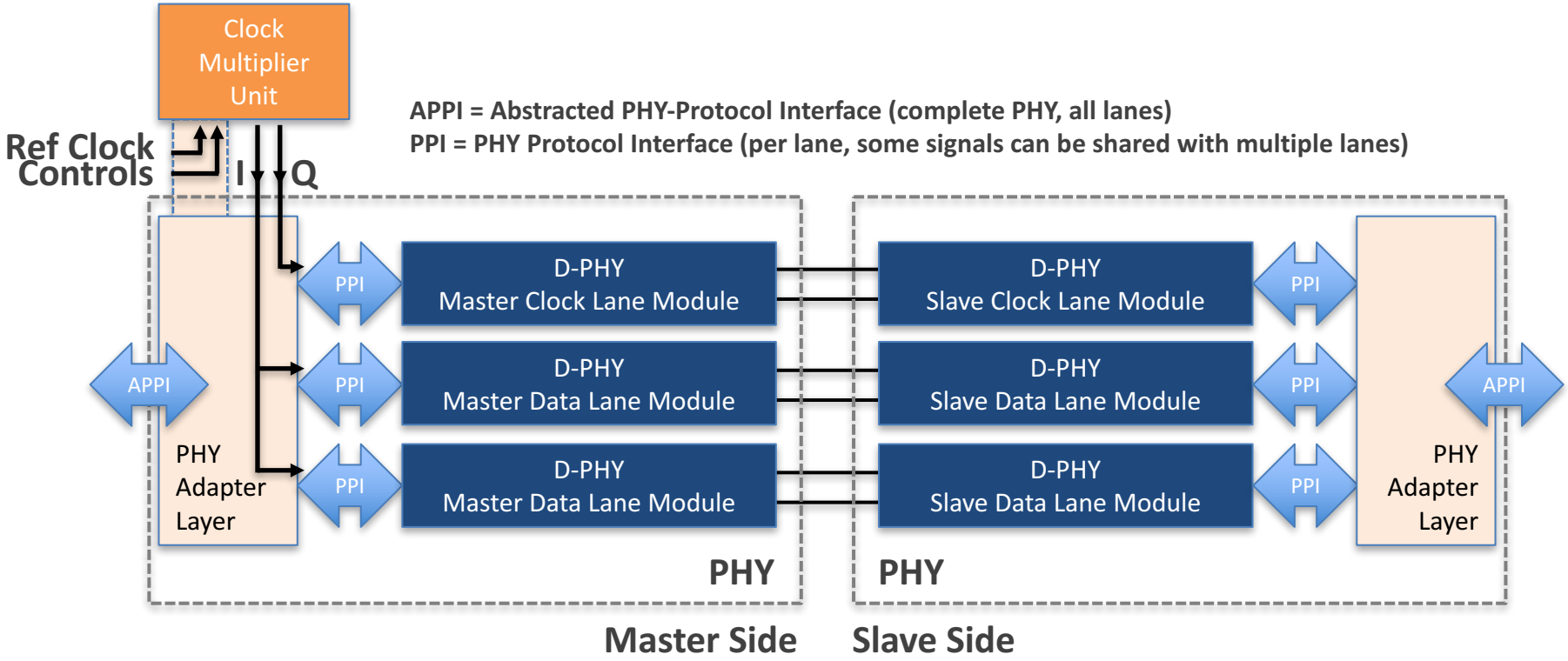
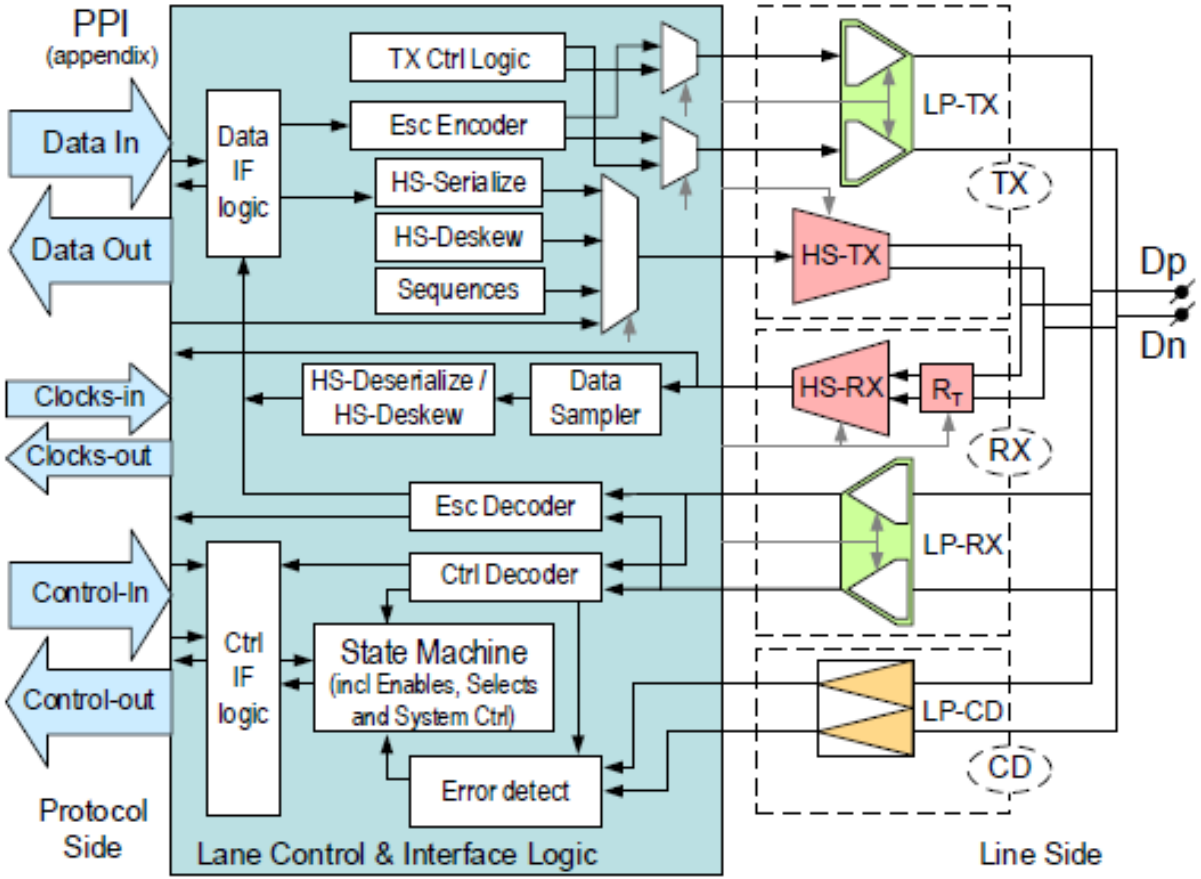
Basic PHY Architecture



Lane Module



Spec Parameters	D-PHY 3.0	D-PHY 2.0/2.1	D-PHY 1.2	D-PHY 1.1	D-PHY 1.0
Data Rate	10-14 Gbps	4.5Gbps	2.5Gbps	1.5Gbps	1Gbps
HS Tx Differential Voltage	140-270mV	140-270mV	140-270mV	140-270mV	140-270mV
HS Tx Single Ended Output Impedance	40-62.5ohms	40-62.5ohms	40-62.5ohms	40-62.5ohms	40-62.5ohms
HS Tx Common Mode Static Voltage	150-250mV	150-250mV	150-250mV	150-250mV	150-250mV
HS Tx Rise/Fall Times (20-80%)	TBD	30-100ps(4.5Gbps)	50ps-0.4UI	100ps-0.35UI	100ps-0.3UI
Tx Cpad Target (Driven by return loss in the spec)	TBD	3pF	3.3pF	3pF	3pF
HS Tx De-emphasis	TBD	-3.5dB(+/-1dB) -6dB(+/-1dB)	None	None	None
Spread Spectrum Clocking	ModulationRate~30-33KhZ SSC Deviation~-5000PPM Down Spread	ModulationRate~30-33KhZ SSC Deviation~-5000PPM Down Spread	None	None	None
Scrambling	Yes Need to be supported by the Controller	Yes Need to be supported by the Controller	None	None	None

Spec Parameters	D-PHY 3.0 (In progress)	D-PHY 2.0	D- PHY 1.2	D-PHY 1.1	D- PHY 1.0
HS Tx Timing	TBD	TJ~0.3UI DJ~0.2UI RJ~0.1UI All Jitter relative to clock Static Skew Clock to Data~-0.2 to 0.2UI	TJ~0.3UI All Jitter relative to clock. Static Skew Clock to Data~-0.2 to 0.2UI	Data to Clock Skew~-0.2 to 0.2UI	Data to Clock Skew~-0.15 to 0.15UI
HS Tx AC CM Noise	15mVrms(>450MhZ) 25mVpk-pk(50-450MhZ)	15mVrms(>450MhZ) 25mVpk-pk(50-450MhZ)	Same as DPHY2.0	Same	Same
BER	1e-12	1e-12	1e-12	1e-12	1e-12
LP Tx Output High Level	TBD	0.95-1.05	0.95 to 1.3V	1.1-1.3	1.1-1.3V
LP Tx Min Slew Rate	TBD	25mV/ns	25mV/ns	30mV/ns	30mV/ns
LP Tx Max Slew Rate	TBD	500mV/ns(0pF Load) 300mV/ns(5pF Load) 250mV/ns(20pF Load) 150mV/ns(70pF Load)	Same as DPHY2.0	Same	Same
Channel Loss	MPHY Spec Channel2 (7-14inch)	MPHY Spec Channel2 (7-14inch)	MPHY Spec Channel2 (7-14inch)	DPHY Spec Channel (5-11inch)	DPHY Spec Channel (5-11inch)
Channel ISI	TBD	0.2UI	0.2UI	+/-0.1UI	+/-0.2UI
Channel Clk to Data Statix Skew	TBD	+/-0.1UI	+/0.1UI	None(Included in Channel ISI)	None(Included in Channel ISI)

Spec Parameters	D- PHY 3.0	D- PHY 2.0	D- PHY 1.2	D- PHY 1.1	D- PHY 1.0
HS Rx Deskew	Internal Clock to Data using Tx Calibration Pattern	Internal Clock to Data using Tx Calibration Pattern	Internal Clock to Data using Tx Calibration Pattern	None	None
HS Rx Differential Input Threshold	TBD	+40mV to -40mV	+40mV to -40mV	+70mV to -70mV	+70mV to -70mV
HS Rx Common Mode DC	TBD	70-330mV	70-330mV	70-330mV	70-330mV
HS Rx Differential Input Impedance	80-125ohms	80-125ohms	80-125ohms	80-125ohms	80-125ohms
HS Rx Common Mode Noise Tolerance	TBD	100mV(pk-pk)	100mV(pk-pk)	200mV(pk-pk)	200mV(pk-pk)
HS Rx Jitter Tolerance	TBD	Tjtol~0.5UI DJ~0.4UI RJ~0.1UI	Tjtol~0.5UI	No Independent Jitter Spec	No Independent Jitter Spec
HS Rx Skew Tolerance	TBC	Static Skew of +/-0.3UI between Clock and data	Static Skew of +/-0.3UI between Clock and data	Setup/Hold~0.2UI	Setup/Hold~0.15UI
HS Rx Common Mode Voltage DC	TBD	70-330mV	70-330mV	70-330mV	70-330mV
HS Rx Common Mode Termination	TBD	14pF-60pF	14pF-60pF	2-60pF	2-60pF

Spec Parameters	D-PHY 3.0	D-PHY 2.0	D-PHY 1.2	D- PHY 1.1	D- PHY 1.0
LP Rx Min Input Voltage	TBD	740mV	740mV	880mV	880mV
LP Rx Min Pulse Width	TBD	20ns	20ns	20ns	20ns
PPI Data Bus Width	TBD	8/16/32 bit	8bit	8bit	8bit
COG Channel Support for Displays	Yes WIP Plan to support higher channel loss for displays.	Yes WIP Plan to support higher channel loss for displays.	None	Not Known	-

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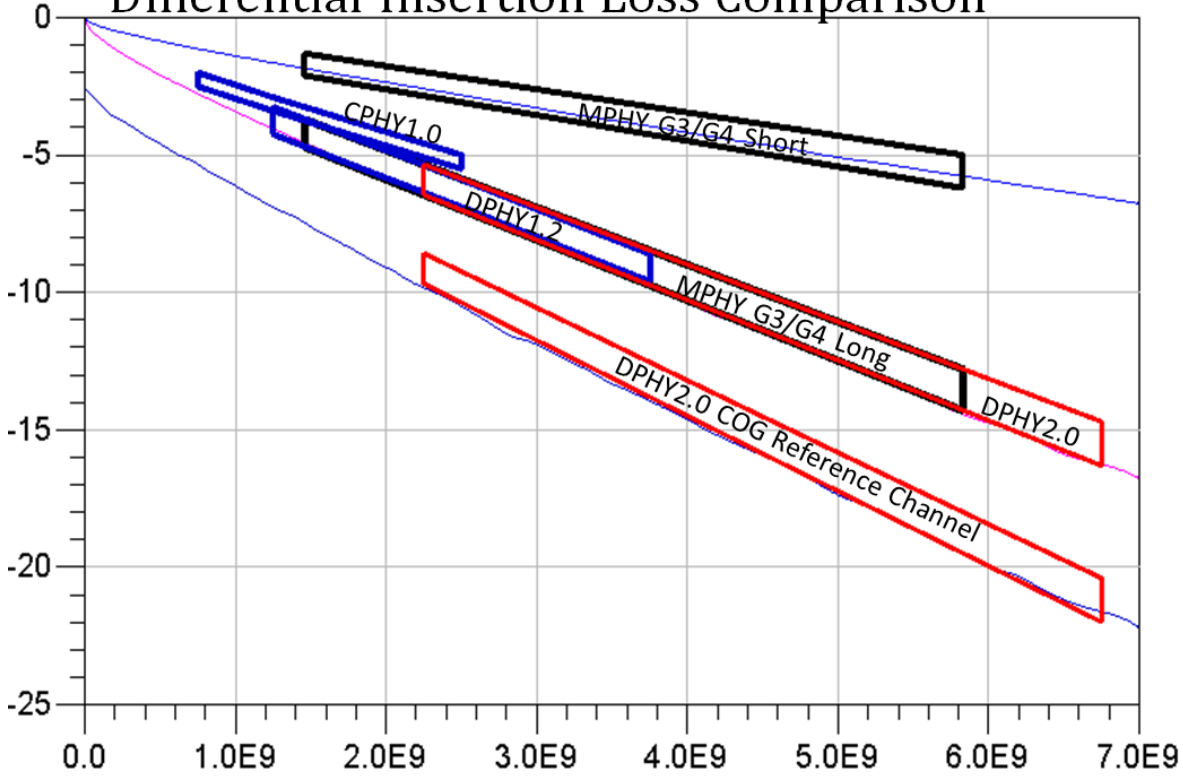
Differential Insertion Loss Comparison



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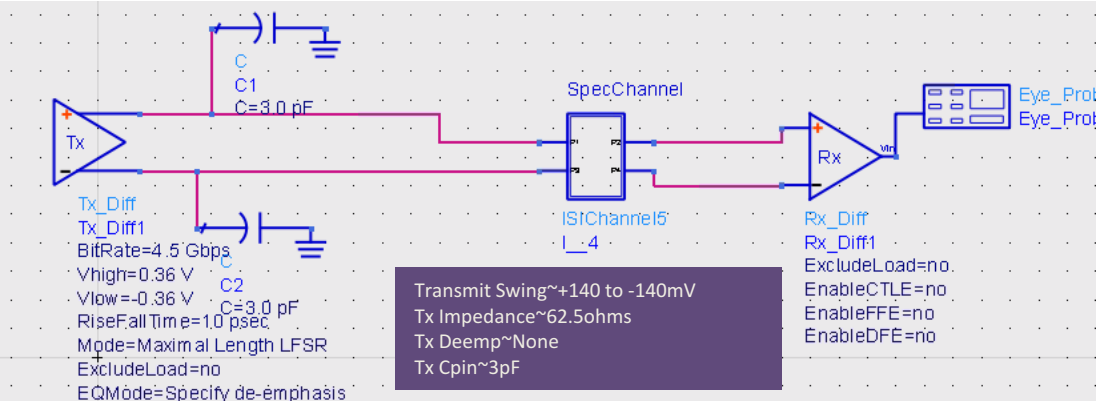
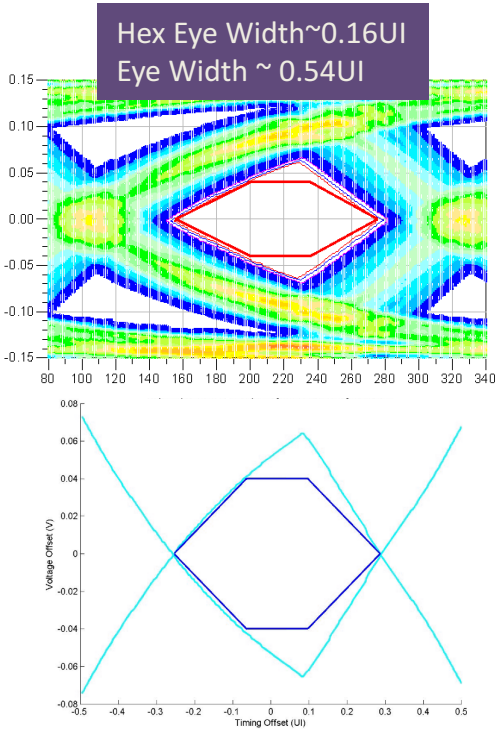
Tx+ Short Channel+ Termination (Tx Eye Diagram)





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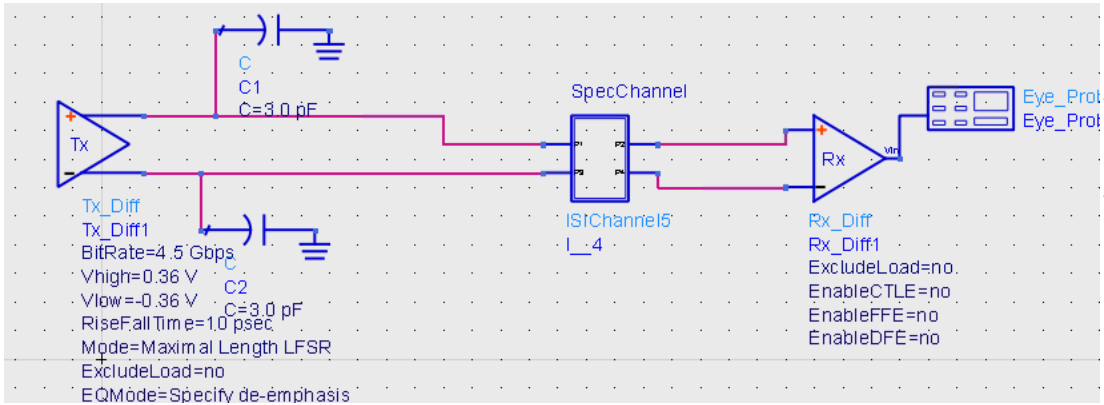
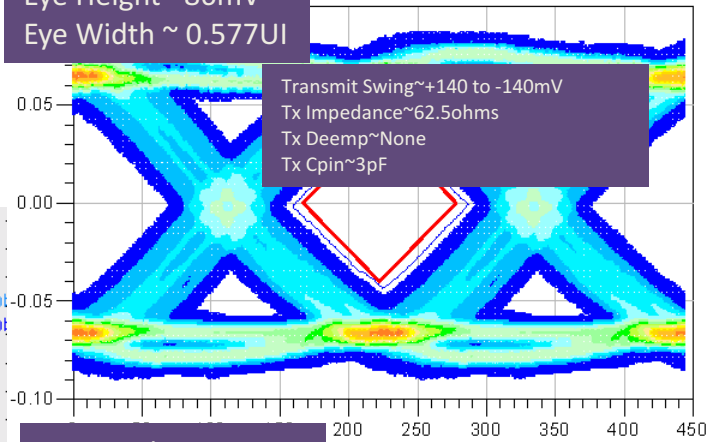
Tx+ SpecChannel + Termination

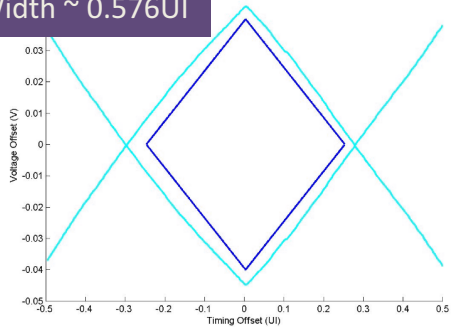


Eye Height ~86mV
Eye Width ~ 0.577UI

Transmit Swing~+140 to -140mV
Tx Impedance~62.5ohms
Tx Deemp~None
Tx Cpin~3pF



Eye Height ~88mV
Eye Width ~ 0.576UI



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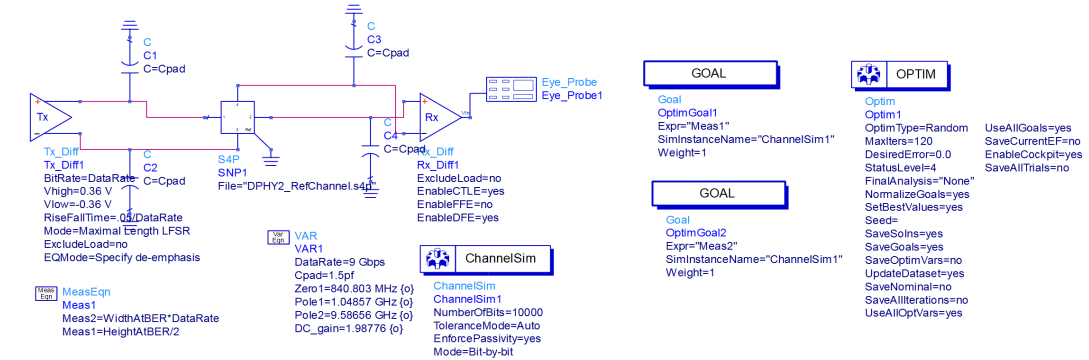
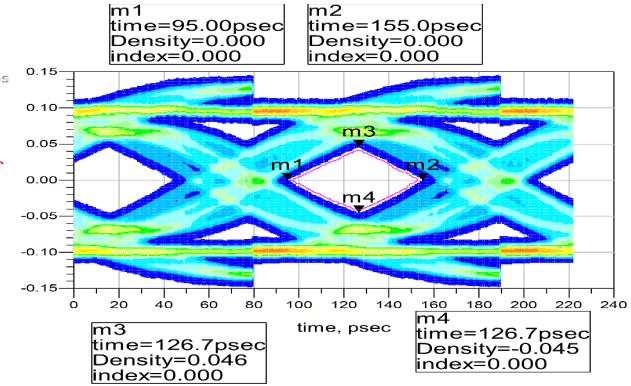
Tx+ SpecChannel + Termination (9Gbps)





- Data Rate = 9 Gbps
- Pattern PRBS9
- Tx de-emphasis = 7dB
- Tx output impedance 125 ohm
- Cpad = 1.5 pf
- Channel Reference 2
- Rx termination 80 ohm
- Rx equalization CTLE adaptable.
- Zero1 = 840 Mhz
- Pole 1 =1.048 Ghz
- Pole 2 = 9.586 Ghz
- DC_gain 1.98776
- Rx DFE Adaptive 2 tap

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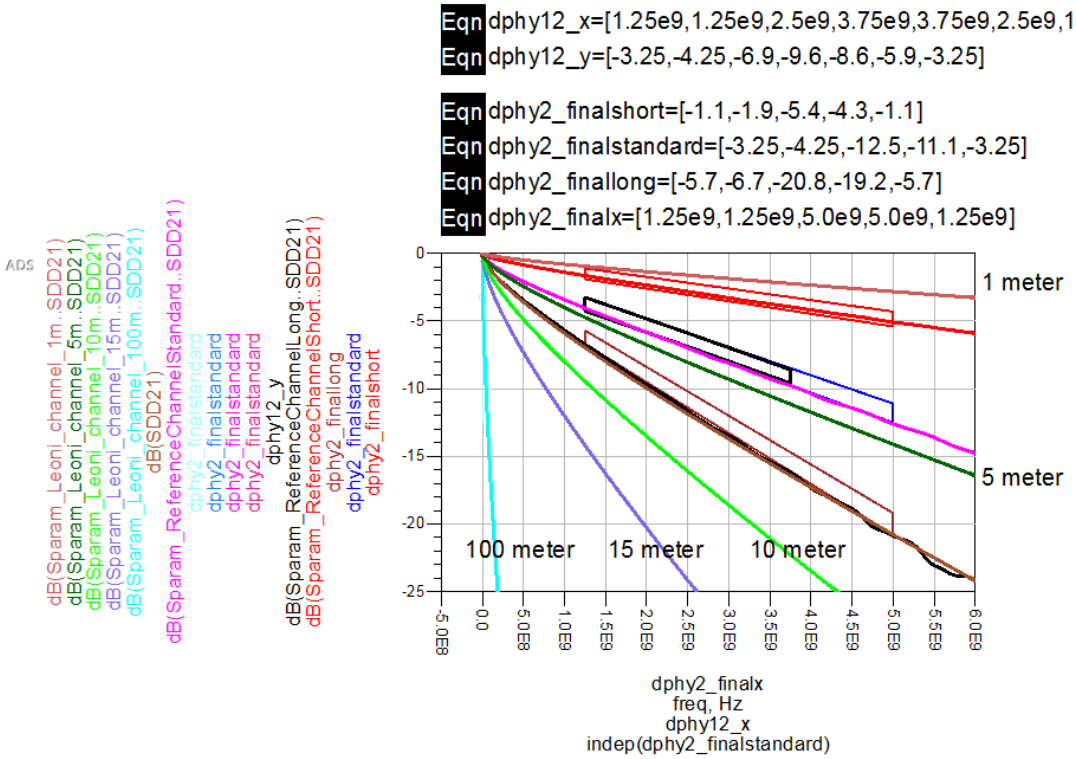
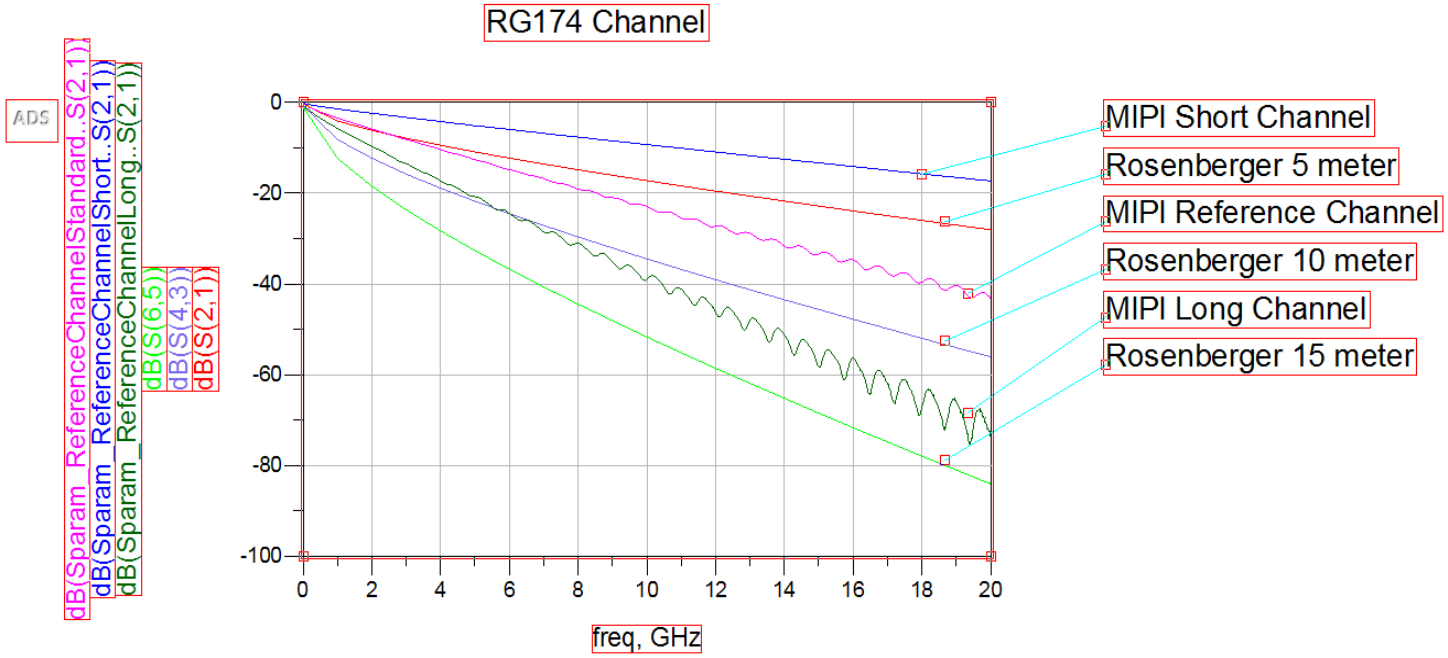
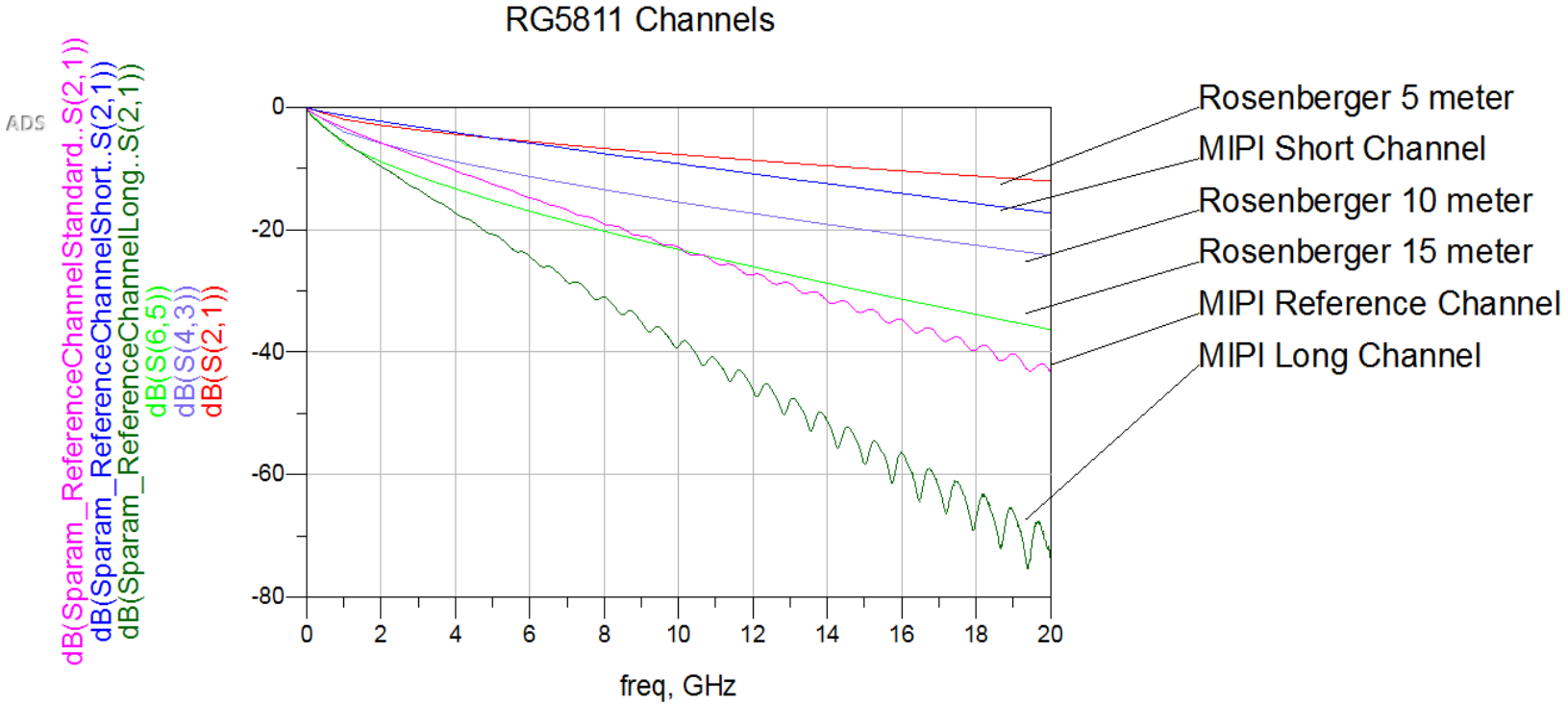
Overall Leoni Channel Performance



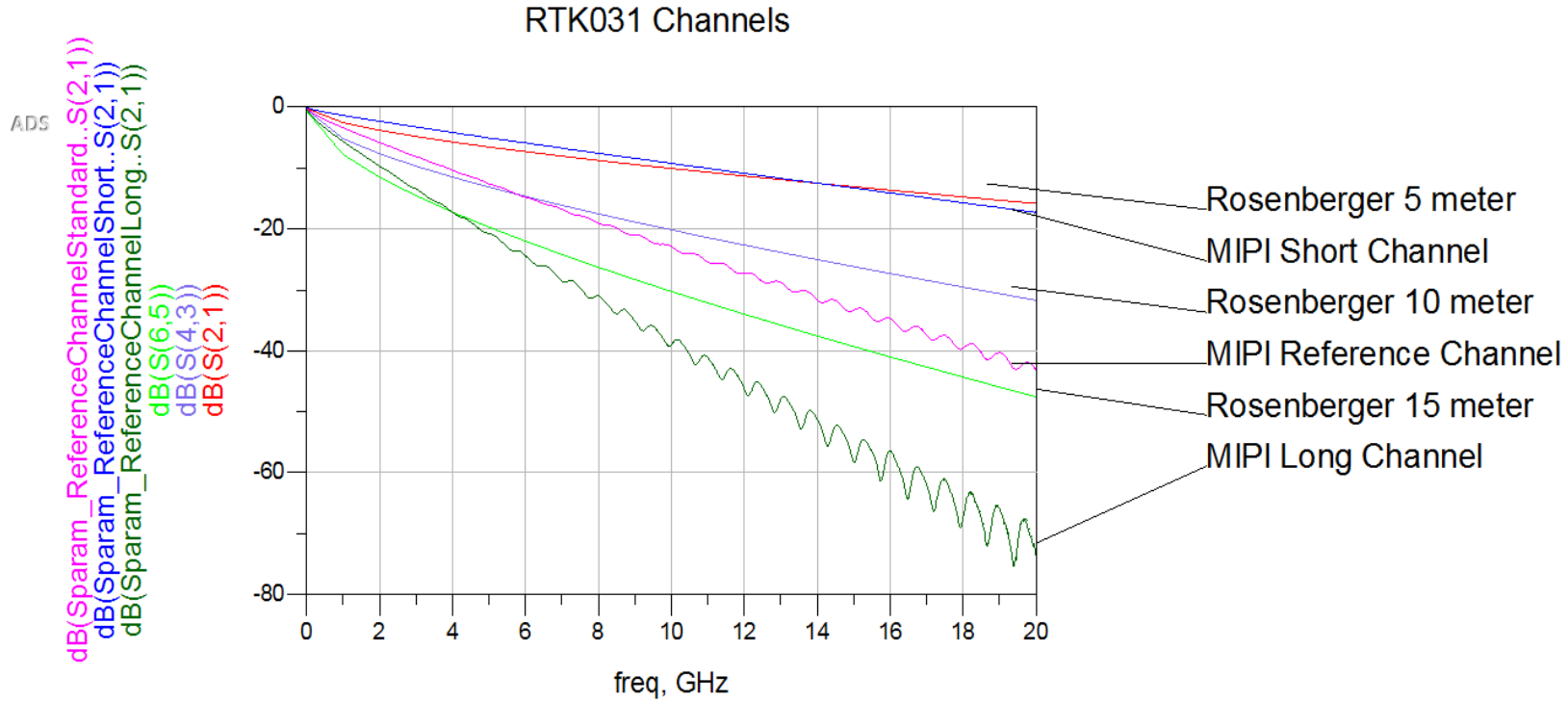
Rosenberger RG174



Rosenberger RG5811



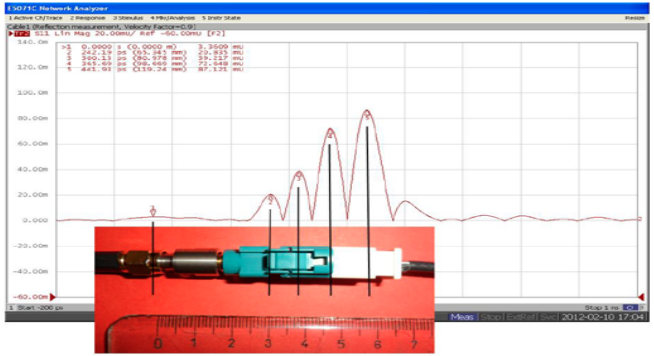
Rosenberger RTK031

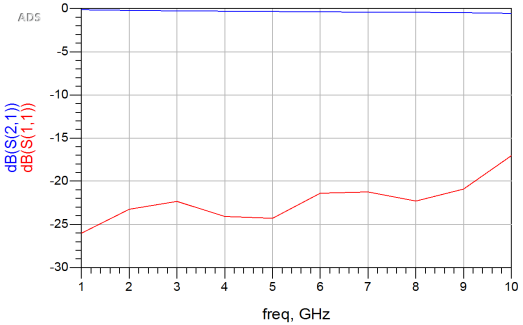


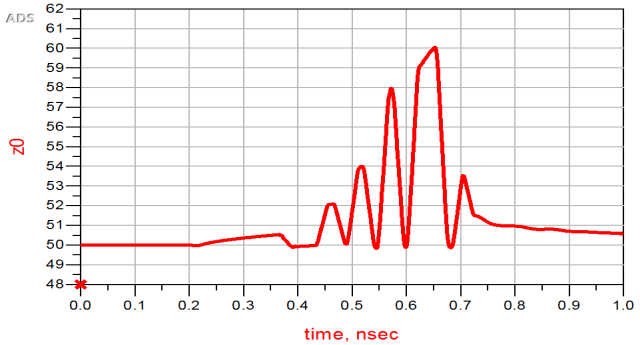
Fakra Connector Modeling

- TDR performance:
  - ADS generated equivalent models
  - S-parameter model/TDR profile

Coaxial cable with adapter and Fakra connector







Source Keysight Technologies

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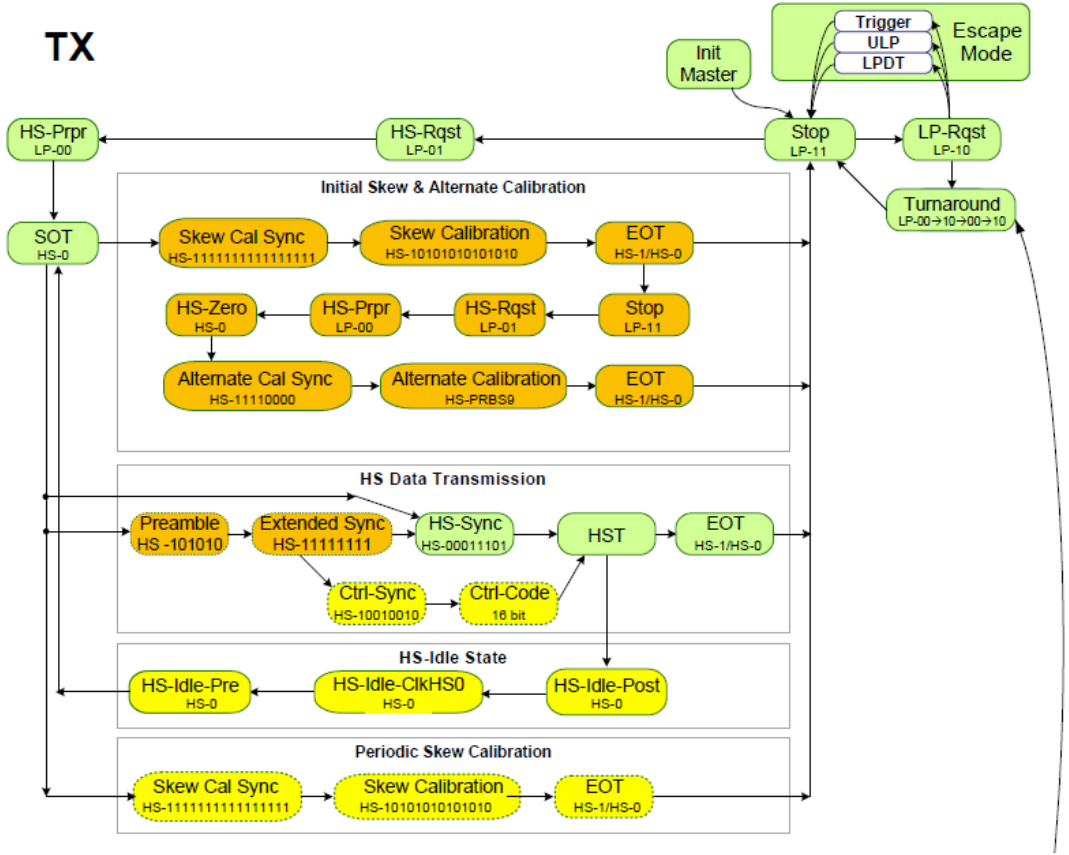
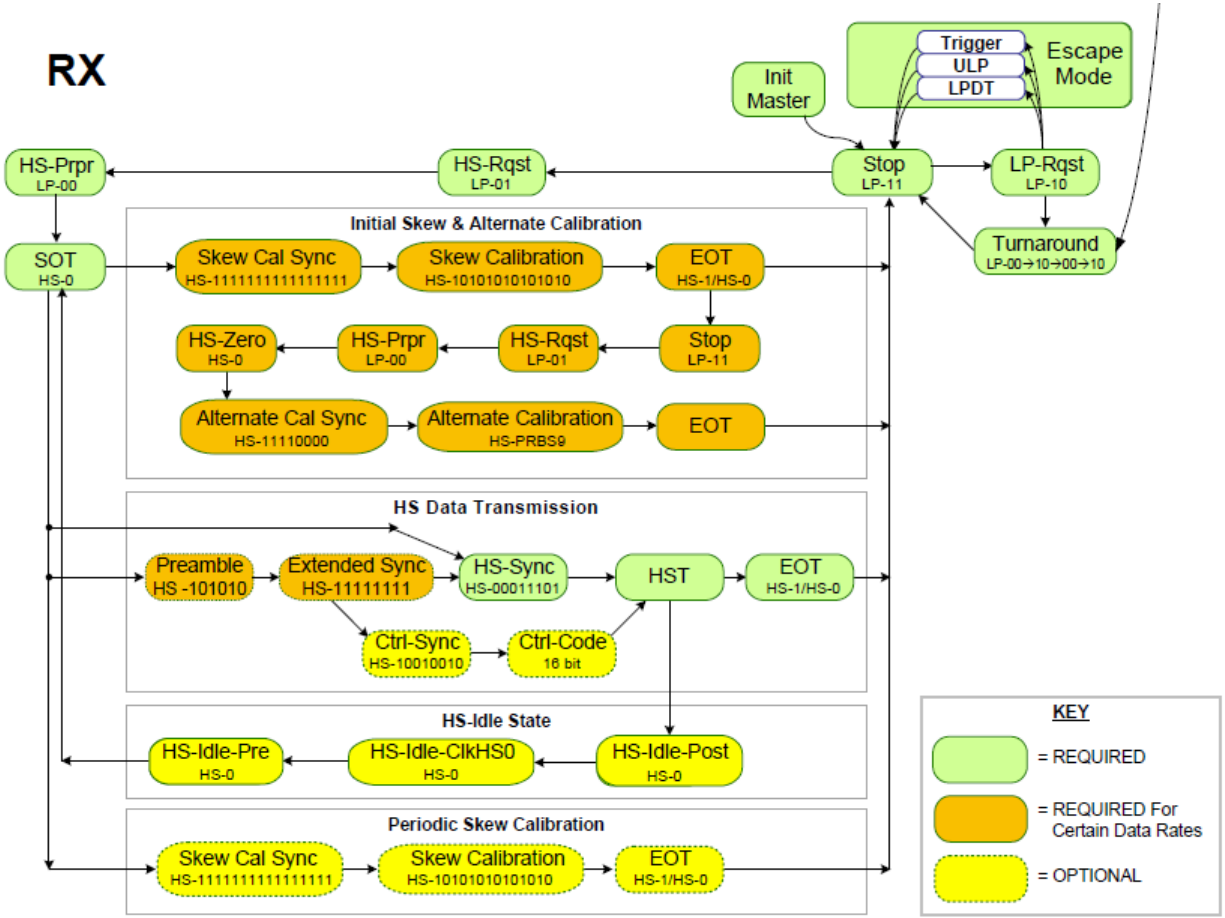
Modes of operation





Summary

- MIPI D-PHY
  - Is the de-facto standard for camera and display connectivity
  - Operates at 4.5 Gbps over multiple lanes
  - Enables SoCs for emerging applications: automotive infotainment and advanced driver assistance systems (ADAS), allowing higher data transmission over longer channels
  - Provides flexibility, speed, power and cost benefits
  - Uses low-latency transitions between high-speed and low-power modes with high noise immunity and high jitter tolerance

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MIPI D-PHY 3.0

- Data rate 10 to 14 Gbps
- Support for automotive grade PHY requirements with long channels
- Transitions to embedded clock above a defined data rates
- Remains backward compatible to MIPI D-PHY 2.1

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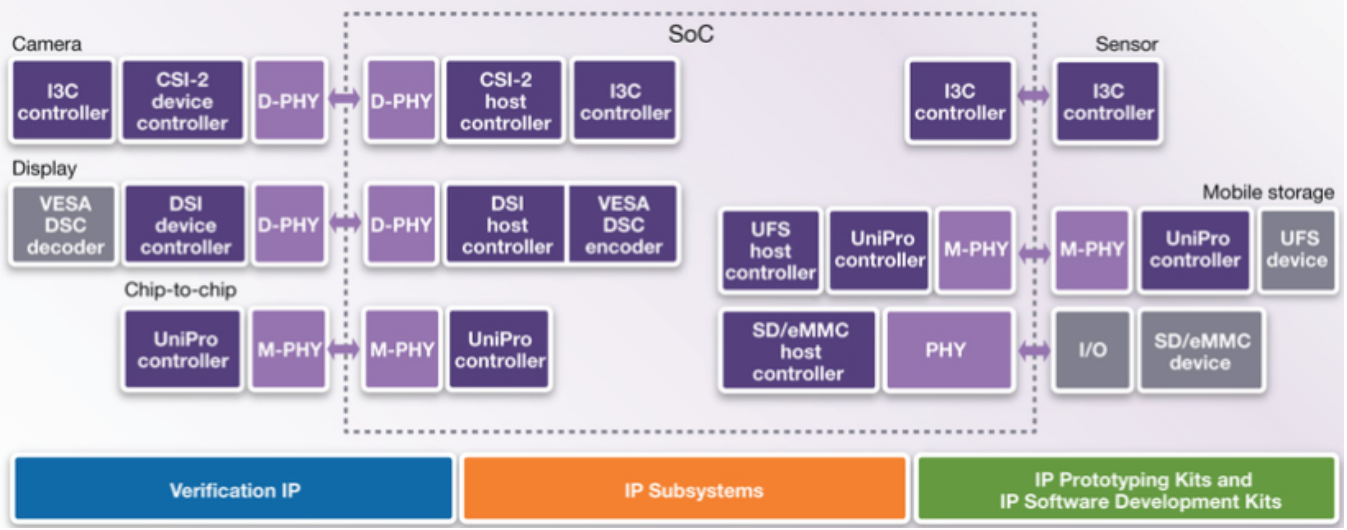
Synopsys® DesignWare® MIPI IP Portfolio



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THANK YOU

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