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Alain Legault
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Next-Generation Mobile, AR/VR, & Automotive Displays With VESA VDC-M & MIPI® DSI-2SM

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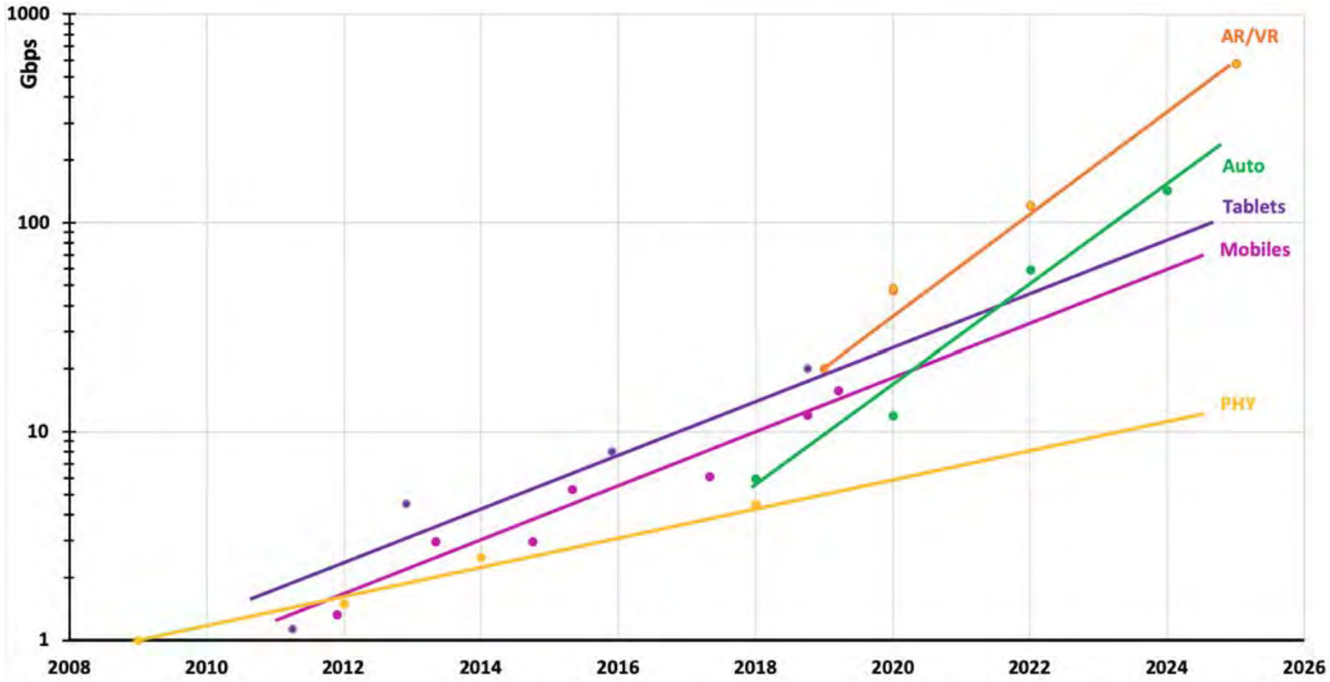
Bandwidth Challenge for Video Connectivity



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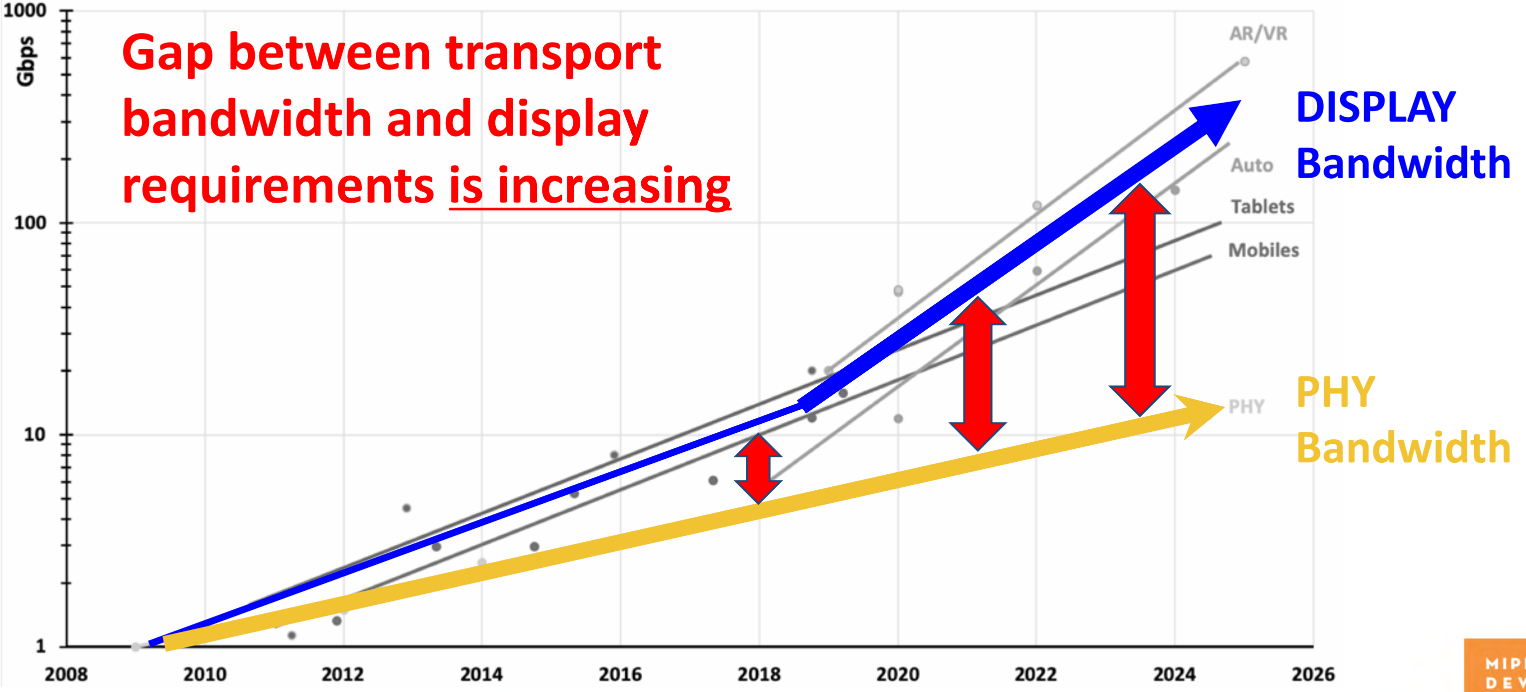
Gap Between Transport & Display Bandwidth



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Possible Solutions vs. Trade-offs

1. Add transport lanes →
   - More pins/cables needed
   - Real estate increase
   - Weight increase
   - Cost increase
   - Power consumption increase
   - EMI noise increase

2. Use video compression →
   - Potential visual artifacts
   - Greater design complexity
   - Increased latency

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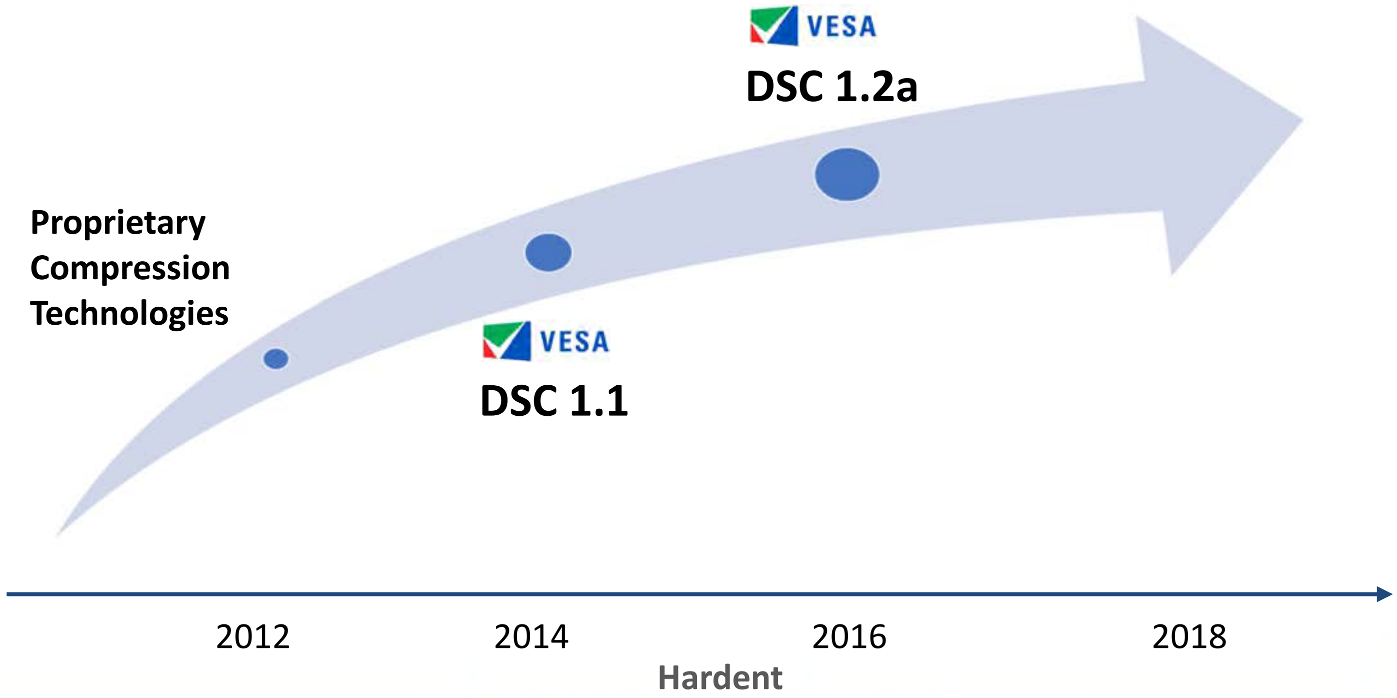
Industry Compression Timeline



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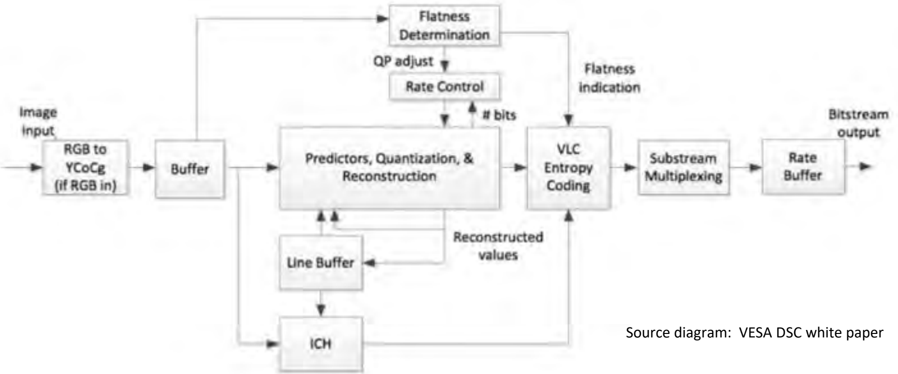
Display Stream Compression (DSC) Overview

- Visually lossless video compression standard
- Up to **3X** compression (**8 bpp**) without any perceptible differences
- Extremely low latency **(< 0.5 usec)**
- Video quality excellent with all types of content
  - Natural and test images, text, and graphics
- Requires a single line of pixel storage + rate buffer



Source diagram: VESA DSC white paper

- Intra-frame Variable Bit Rate Encoder
- Constant Bit Rate (CBR) transmission
- Based on Delta Pulse Code Modulation (DPCM)
- Mid Point (MPP), Block Predictor (BP)
- Modified Median Adaptive Predictor (MMAP)
- Indexed Color History (ICH)

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Transport Standards Using DSC

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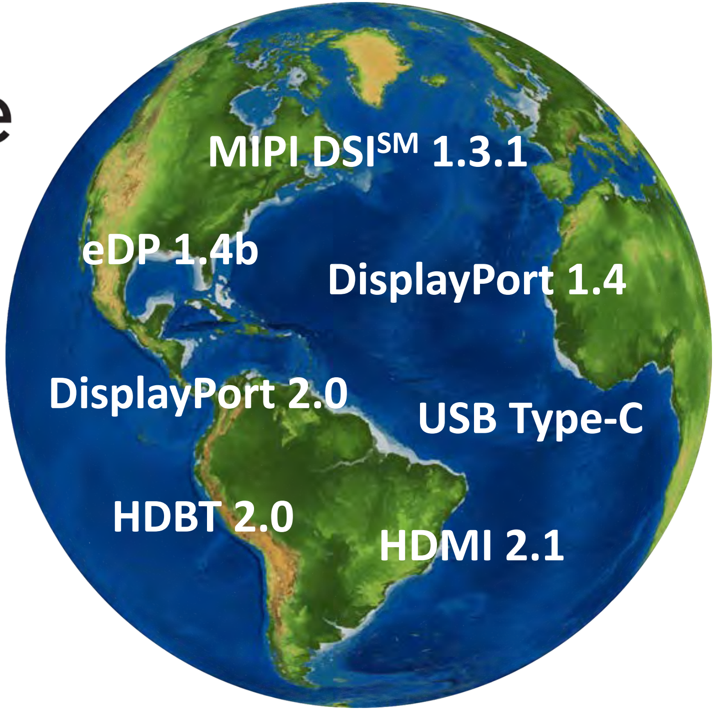
HDMI
HIGH DEFINITION MULTIMEDIA INTERFACE

DisplayPort



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HDBaseT

USB
UNIVERSAL SERIAL BUS

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Applications Using DSC

- Mobiles
- Tablets
- GPUs
- AR/VR head-mounted displays
- In-car video systems
- Video transport
- UHD / 8K TVs
- DTV STBs
- High-resolution monitors

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Some Applications Require Even More Bandwidth

Mobile Displays

- Need to support gaming
- Need to be “AR/VR ready”
- Require higher display resolutions & frame rates

AR/VR Displays

- Need to drive two displays
- Require higher pixel density (ppi) & frame rates

Automotive Displays

- Are increasing rapidly
- Require higher display resolutions

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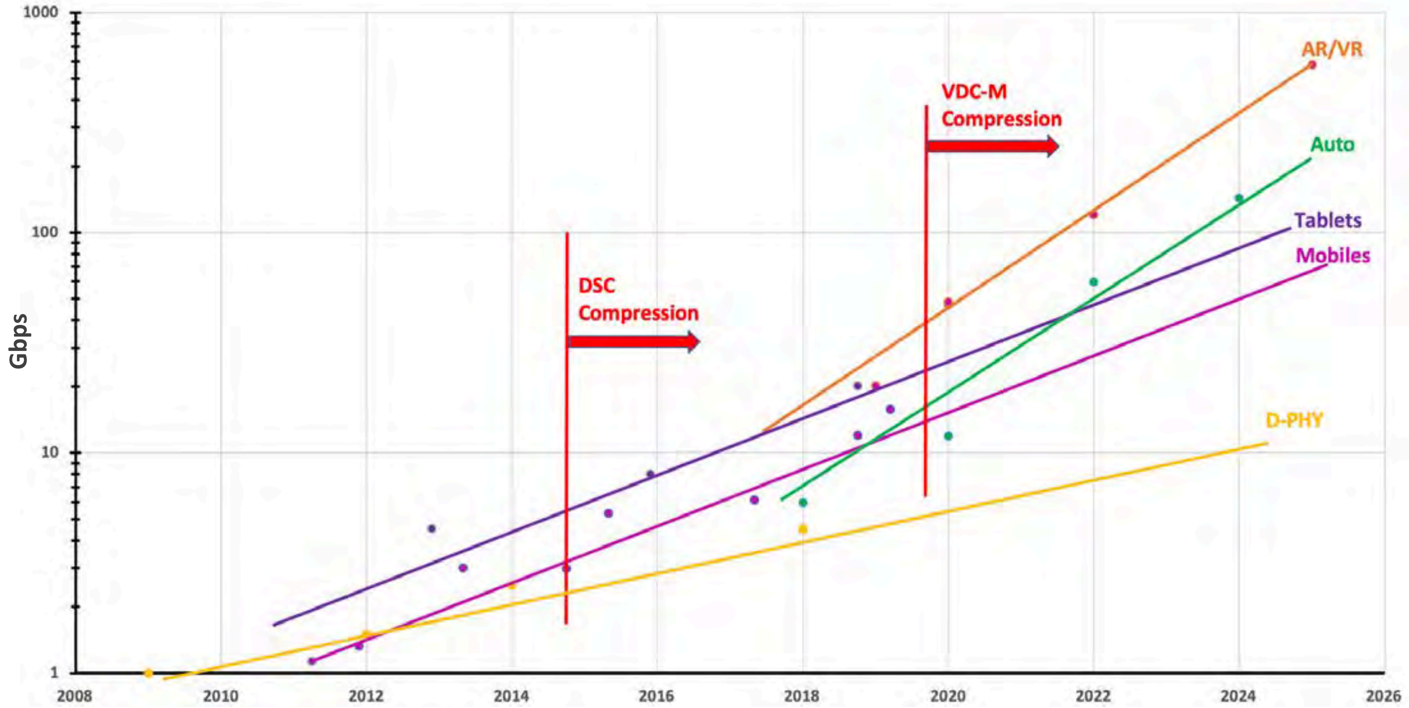
Product Display Bandwidth Trends



VDC-M = VESA Display Compression for Mobile

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DSC vs. VDC-M

	DSC	VDC-M
Encoding Block Structure	3x1 pixels	8x2 pixels
Encoding Tools	• Mid Point (MPP) • Block Predictor (BP) • Modified Median Adaptive Predictor (MMAP) • Indexed Color History (ICH)	• Mid Point (MPP) • Enhanced Block Predictor (BP) • Transform (DCT and Hadamard) • Enhanced Quantization
Visually Lossless Performance	8 bpp (bits per pixel)	5-6 bpp (bits per pixel)
IC Complexity	Low	Medium
RAM Usage	Single line	2.5 lines
Latency (end-to-end) (UHD 3840x2160 example)	<0.5us <2H line	<1.2us <5H line
Pixels / Clock Architecture		
Encoder	1	2
Decoder	3	4

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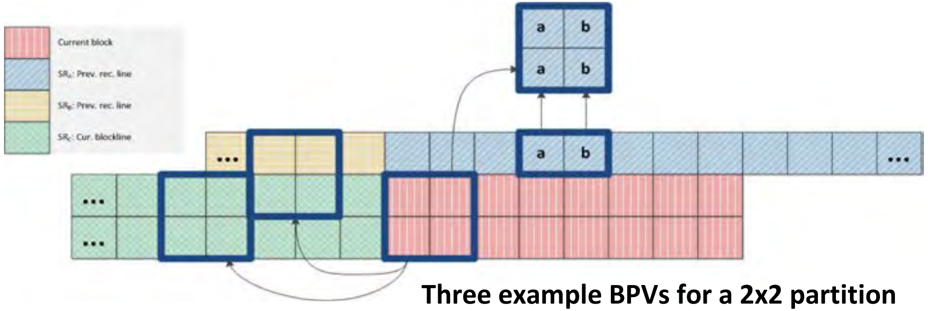
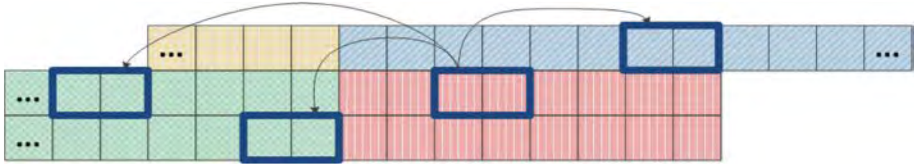
VDC-M Enhanced Block Prediction Mode

- Block prediction is performed on 2x1 or 2x2 partitions
  - One block prediction vector (BPV) for all color components of each partition
- Block prediction uses a large and regular search area
  - 64 potential BPVs for each partition

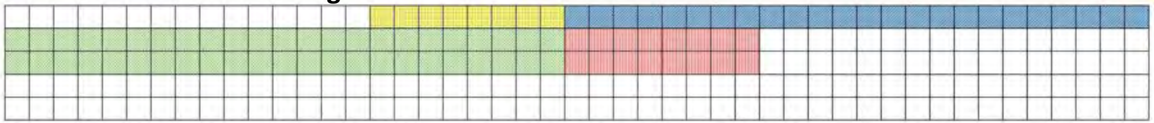


Three example BPVs for a 2x2 partition



Three example BPVs for a 2x1 partition

Search Range



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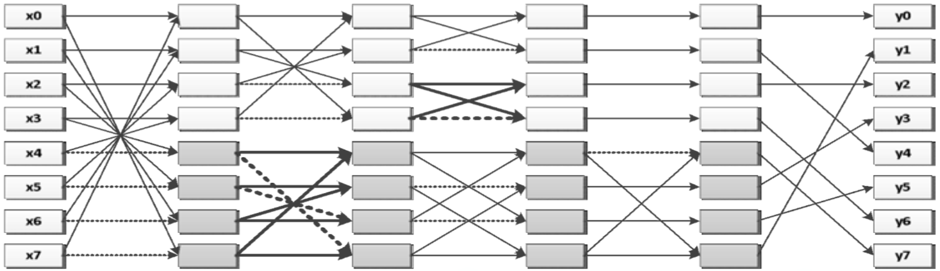
VDC-M New Transform Mode

- Transforms residuals of best of 8 intra-predictors
  - DC, Vertical, Vertical Left, Vertical Right, Diagonal Left, Diagonal Right, Horizontal Left, Horizontal Right
- Transform is done for each color component on 8x2 block (or 4x2 block for YUV 4:2:x chroma)
  - Uses Butterfly DCT in horizontal direction and Hadamard transform in vertical direction
  - Separates higher frequencies (which the eye is less sensitive to) from lower frequencies
  - Similar transform to what is done in MPEG and JPEG encoding



Source: VESA VDC-M Slides

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Transport Standards Using VDC-M

- VDC-M was officially released in May 2018
- MIPI Alliance adopted VDC-M 1.2 as part as their new DSI-2 v1.1 specification
- VDC-M is now being considered by other transport specifications

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Mobile Market Trends

- Mobile devices need to be VR-ready
- Movement from LCD to OLED displays
  - Ultra-high resolutions and pixel density (up to 1500 ppi)
  - High dynamic range
  - Higher frame rate
  - Optical compensation
  - Foldable, rollable displays
  - Lower power consumption
  - Non-uniformity compensation
- DDIC frame buffer going from 10 to 100 Mbits

	2010	2020
Display Resolution	1280 x 720 HD	3840 x 2160 4K
Frame Rate	60 fps	120 fps
Pixel Depth	24 bits	30 bits
Interface	0.5 Gbps / lane	2.0 Gbps / lane
Display Bandwidth	1.3 Gbps	29.9 Gbps

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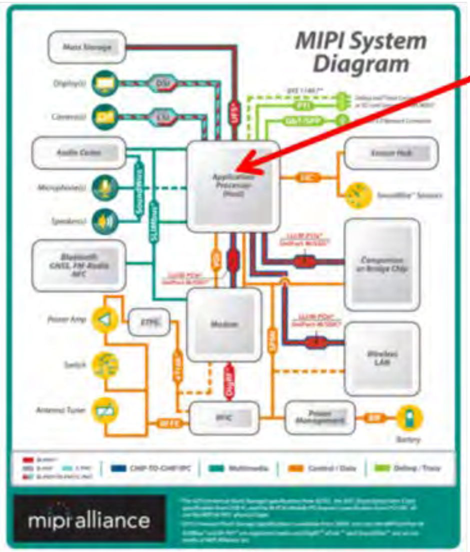
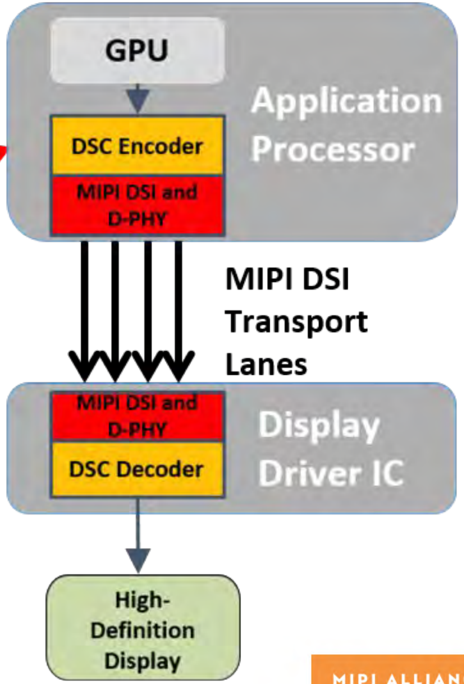
Use Case: Mobile and Tablet Applications

- Application processor
- DDIC (Display Driver IC) and touch panel controller
- **Benefits**
  - **Reduce bandwidth**
  - **Save power**
  - **Save on cost**
  - **Lower EMI**





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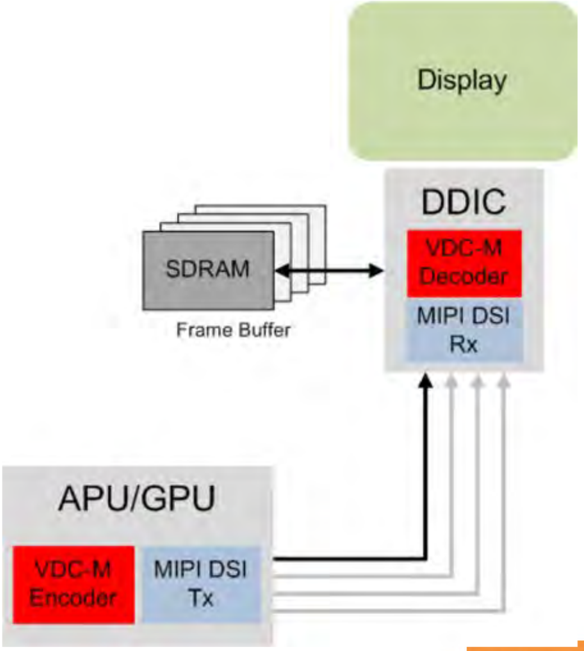
VDC-M Mobile/Tablet Use Case

- Additional DSI lane saving
- Power consumption saving
- Smaller SDRAM frame buffer



Examples

- WQUXGA Display (2400x3840) 24bpp 60fps
  - D-PHY[SM] 2.5Gbps: only 2 lanes required
  - SDRAM 4 times smaller
- UHD Display (2160x3840) 30bpp 120fps
  - D-PHY 2.5Gbps: only 3 lanes required
  - SDRAM 5 times smaller

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AR/VR Market

- Console market
  - Oculus, HTC Vive, Sony Playstation, Windows MR,...
  - Cables are running out of bandwidth
    - Requires 2 displays at higher resolution, higher ppi, higher refresh rates

- Standalone market
  - Microsoft Hololens, Google Daydream, Oculus Go, HTC Vive Focus,...
  - Bandwidth, power management, and miniaturization are huge obstacles
  - Optimized silicon is emerging
    - Qualcomm Snapdragon XR, ARM Mali-D77, NVidia Tegra

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Use Case: AR/VR Head-Mounted Display

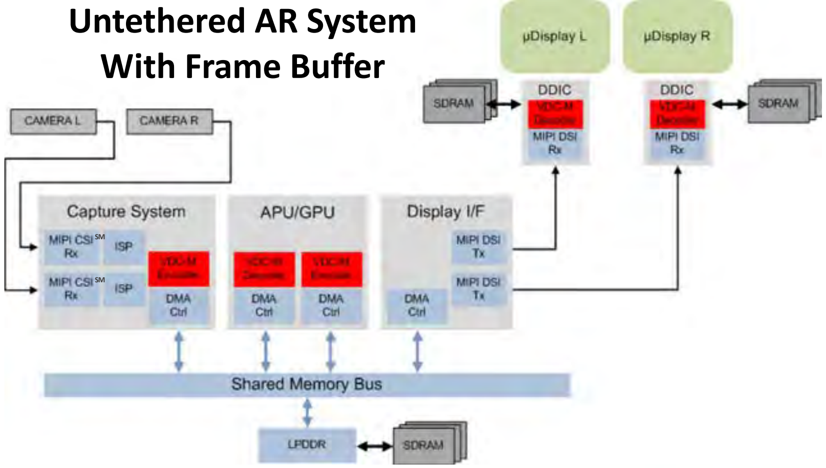
Applications

- Video capture
- Application processor and GPU
- Micro-display driver IC

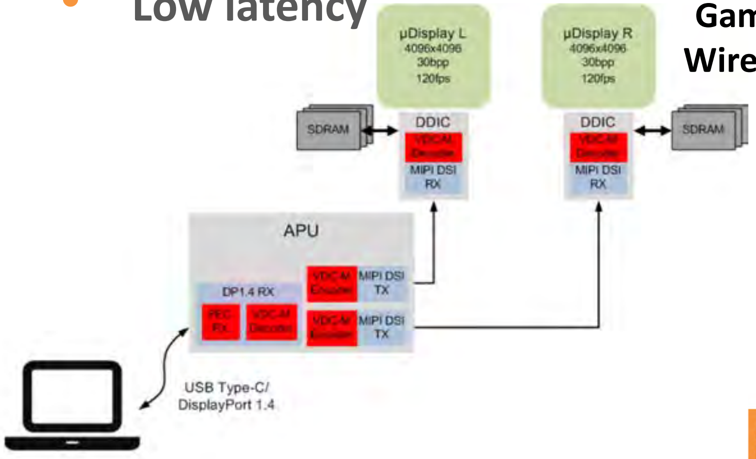
Benefits

- **Lower bandwidth**
- **Smaller RAM buffer**
- **Power and $ savings**
- **Low latency**

Untethered AR System With Frame Buffer



Game Console - Wired VR System



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VDC-M to Fulfill Future AR/VR Requirements

VESA members AR/VR Task Group Survey Summary

1. Resolutions per eye will increase over time from 2K x 2K in 2019 to **8K x 8K in 2025**

2. It is believed that very few people see a difference beyond 8K x 8K per eye
   a. This is about **60 pixels per degree** for 273 degrees horizontally
   b. It allows 220 degrees plus 25 degrees of overlap between the eyes

3. Refresh rates required is between **120 to 240Hz** to meet human perception limits

4. Pixel resolution of 12bpc will be required by 2025

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AR/VR Use Cases & VDC-M

- All resolutions/frame rates below are "per eye"

Transport	Transport Bandwidth Available	DSC 8bpp	VDC-M 6bpp	VDC-M 5bpp
10 Gbits/sec 2 lanes	19.3 Gbits/sec	2.8Kx2.8K 120Hz	4Kx4K 100Hz	4Kx4K 120Hz
10 Gbits/sec 4 lanes	38.7 Gbits/sec	4Kx4K 120Hz	5Kx5K 120Hz	5Kx5K 120Hz
20 Gbits/sec 2 lanes	38.7 Gbits/sec	4Kx4K 120Hz	5Kx5K 120Hz	5Kx5K 120Hz
20 Gbits/sec 4 lanes	77.3 Gbits/sec	5Kx5K 120Hz	8Kx8K 100Hz	8Kx8K 120Hz

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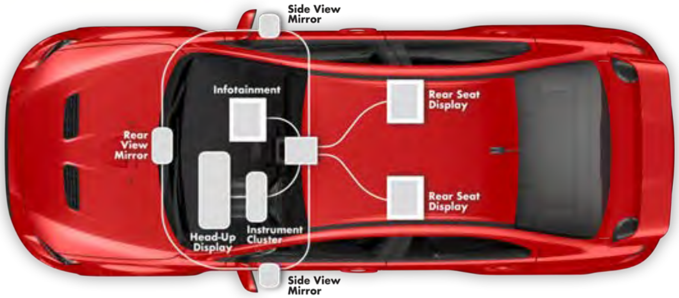
Digital Car Market



- Number of displays in cars is increasing rapidly
  - ADAS, infotainment, control panels, rear seat displays, head-up displays, side and rear view mirrors, …
    - 1-3 displays → 10-12 displays
    - 1 camera → 5-10 cameras
    - 2-5 sensors → 10-20 sensors

Display Type	Spatial Resolution		DPI (pix / inch)	Bandwidth Req. @ 60 Hz refresh
Mid-range car	HD	1280 x 720	100	1.8 Gbps
High-end car	FHD	1920 x 1080	200	3.6 Gbps
Next-gen. car	UHD	3860 x 2160	400	14.4 Gbps

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Automotive Transport Link Technologies Today

- Several technologies available: Maxim GMSL, Inova APIX, Valens HDBaseT, TI FPD-Link
- Link speed ranges between 1.0 - 6.0 Gbps typically over a 15 meter coaxial or shielded twisted pair cable
- Automotive environment is demanding: higher bitrate (> 6 Gbps) adds significant challenges
  - Electromagnetic noise immunity, reliability, cost, etc.
  - Adoption/certification of high-speed serial link technology is a long & expensive process
  - Using multiple links per screen is expensive

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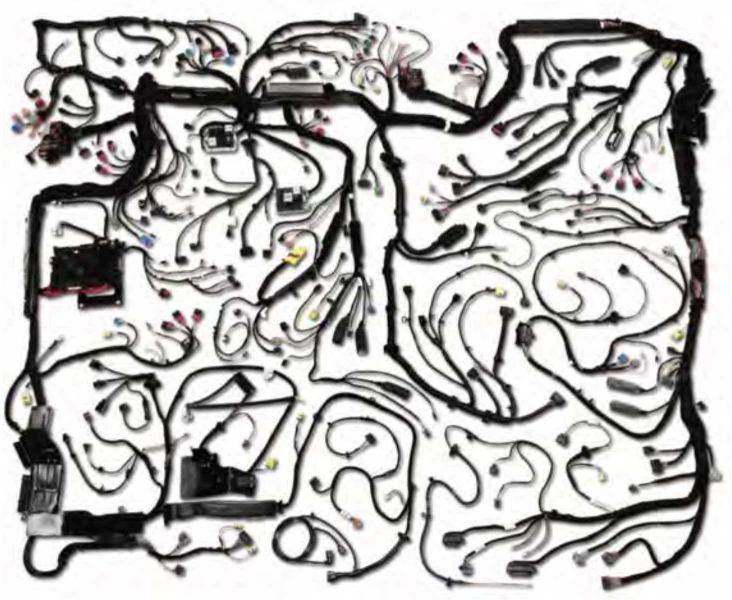
More Cables Is NOT The Solution



- Wiring harness is the 3rd highest cost component in a car (behind engine and chassis) comprising 50% of the cost of labor for the entire car

- 3rd heaviest component
(after the chassis and engine)*

- EMI and signal integrity is a major challenge

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* Source: Delphi, Inc.

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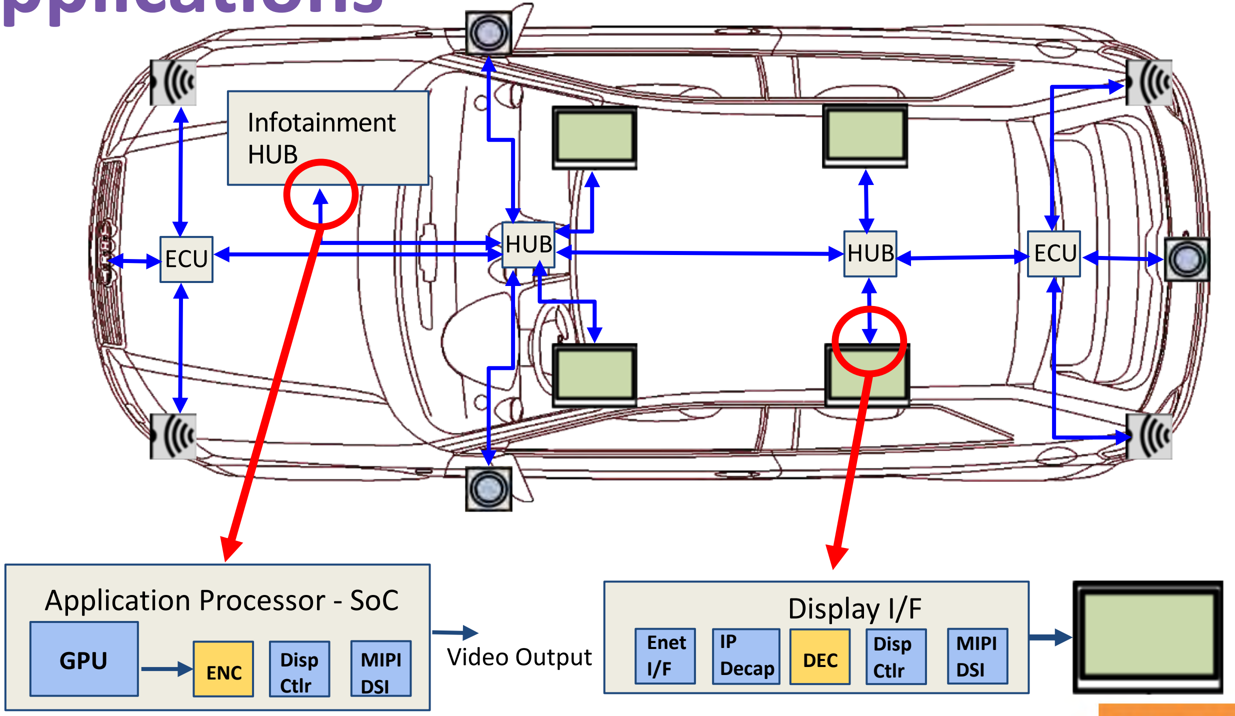
In-Car Video Applications

- Benefits
  - Smaller bandwidth for multiple feeds
  - Low latency
  - Save on expensive cabling
  - Lower EMI



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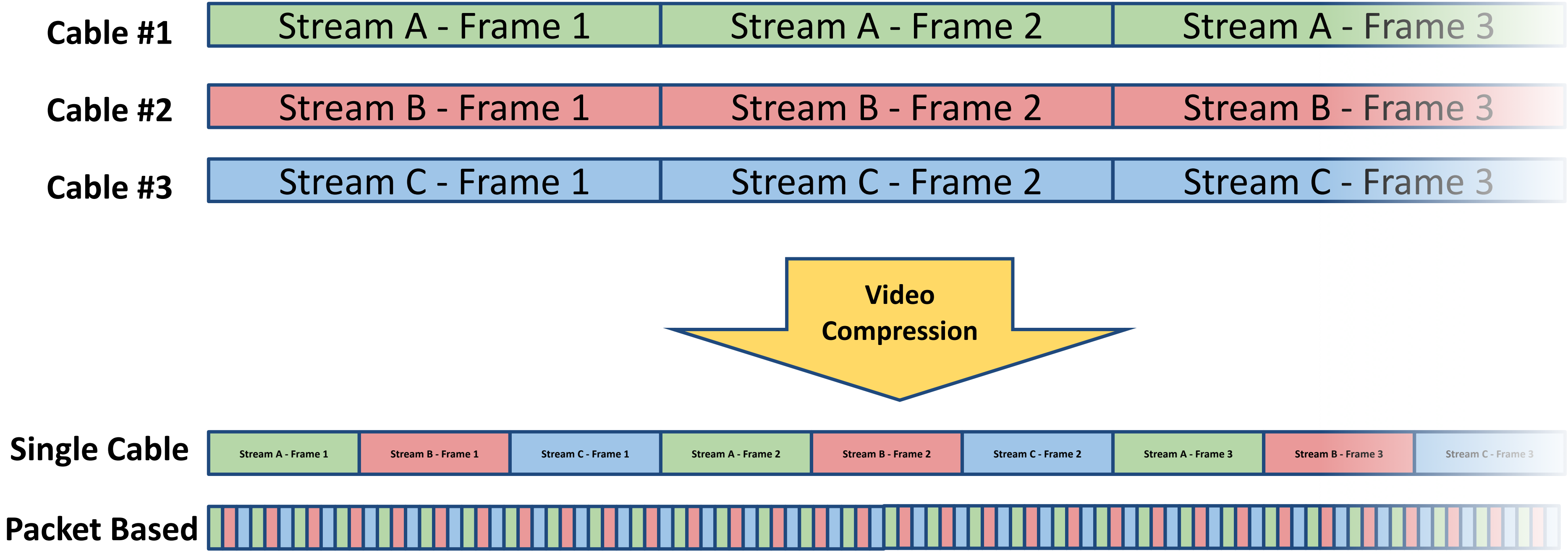
Compressed Multi-Stream Transport



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VDC-M Automotive Use Case

- Number of displays in cars is increasing rapidly

- Display physical size may not increase due to car physical limitation, but resolution is increasing
  - High-end displays now support FHD (150-200 ppi)
  - Next-generation aiming at UHD (300-400 ppi)

- VDC-M extends life cycle of existing link technology
  - Limitations to increase transmission link speed between head unit and multiple displays
  - Automotive environment is demanding, higher bitrate (> 6Gbps) adds significant challenges
    - Electromagnetic noise immunity, reliability, cost, etc.
  - Adoption/certification of high-speed serial link technology is a long and expensive process
  - Using multiple links per screen is expensive
  - Potential use of self-healing ring cuts available link bandwidth

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Use Cases: Display / Link Compression Requirements

- Projected automotive link speed in the future = 12 Gbps
- Future display requirements:
  - 12 UHD displays
  - Bandwidth per display = 600 MPixels/sec = 14.4 Gbps for 24-bit pixels

Compression	Target bpp	Comp. Factor	Bandwidth Req.	# of UHD Displays / Links	# of Links Required For 12 Displays
Uncompressed	24	1X	14.4 Gbps*	1 or 2	12 or 24
VESA DSC	8	3X	4.8 Gbps	2	6
VESA VDC-M	6	4X	3.6 Gbps	3	4
	5	4.8X	3.0 Gbps	4	3

* Slightly exceeds available bandwidth

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Compression For Automotive Displays

Is it safe?

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Automotive Functional Safety

- Governed by **ISO 26262** - Functional Safety for Road Vehicles standard
- 4 safety levels: ASIL A (lowest) to ASIL D (highest)

	ASIL B	ASIL C	ASIL D
Single Point Fault Metric	> 90%	> 97%	> 99%
Latent Fault Metric	> 60%	> 80%	> 90%
Probabilistic Metric for Hardware Failures	$< 10^{-7}$/h	$< 10^{-7}$/h	$< 10^{-8}$/h

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Example: Head Unit Display

- Display shows a video coming from a backup camera
- **Safety Goals** for the end-to-end video path (hardware level):
  - Safety goal #1: stream displayed has **no corrupted pixels**
  - Safety goal #2: stream displayed has **no frozen frame**

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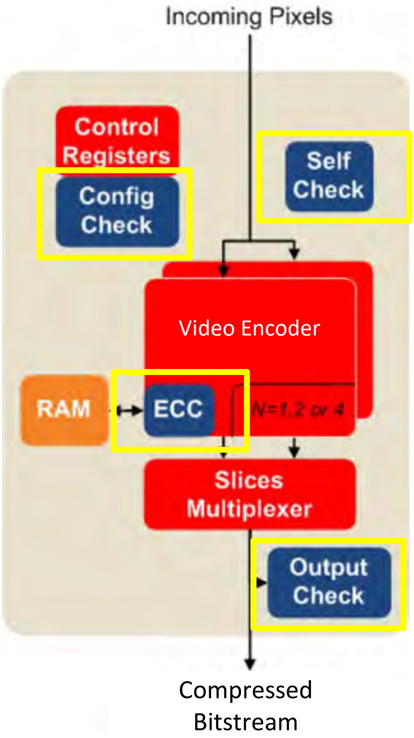
Video Encoder Safety Mechanisms

- Internal Safety Diagnostic Mechanisms
  - Fault avoidance mechanism
    - Reset performed at the beginning of every frame
  - Additional circuits added to the compression IP core (**in blue**)
    - Self Check
    - Control output diagnostics (Output Check)
    - RAM ECC correctable and uncorrectable errors
    - Configuration register protection (Config Check)
- External Safety Diagnostic Mechanisms
  - Offers maximum reliability
  - Implemented to protect against faults not detected by the internal safety mechanisms, e.g.:
    - Interrupt pin validation
    - Frame start/done monitoring
    - Test of internal safety mechanisms
    - **Watermark video frames (detects frozen frames)**



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Conclusion

- There is a clear need within the industry for the additional bandwidth savings offered by VDC-M compression
- VDC-M is already supported by MIPI DSI-2℠
  - VDC-M will be supported by other transport technologies in the future
- The VDC-M compression algorithm is complex
  - Each application has its own unique requirements
- **Visit our demo in the exhibitor area to see a live VDC-M demo & find our more about using compression in your next design**

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ADDITIONAL RESOURCES

- VESA Website

  https://vesa.org/vesa-display-compression-codecs

- MIPI Website

  https://www.mipi.org/specifications/dsi-2

- Hardent Website
  - https://www.hardent.com/ip-products-vdc-m/

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