mipi® DEVCON
MIPI ALLIANCE DEVELOPERS CONFERENCE

28-29 SEPTEMBER 2021

Azusena Lupercio
Juan Orozco
Nestor Hernandez
Intel Corporation

I3C® Signal Integrity Challenges on DDR5 Based Server Platform Solutions

Agenda

- Introduction
- DDR5 SPD server connectivity and bus characteristics
- I2C and MIPI I3C Retro-compatibility challenges
  - Non-dynamic pullup impact
  - Dynamic pullup on open-drain
- Buffer R_{ON} design implications
- Critical time margin calculation
  - Frequency and AC/DC parameters impact
- Non-monotonic signal behavior
- Slope reversal capability and timing improvement
- Summary

mipi® DEVCON

MIPI ALLIANCE DEVELOPERS CONFERENCE

28-29 SEPTEMBER 2021

Introduction

Introduction

- The MIPI I3C Improved Inter-Integrated Circuit interface is first introduced in a server application for the DDR5 DIMM Serial Presence Detect (SPD) function.
- Its implementation exceeds by far the bus capacitance/loading specification, which was defined for low capacitance Mobile/IoT applications.
- This presentation covers the interoperability challenges of the dynamic push-pull and open-drain operating modes on I3C BASIC server applications.
  - Covering an in-depth analysis of the implications of long PCB traces, multiple DIMM routing branches, several loads, to the electrical and timing parameters.

Introduction cont'd

- I3C Communication Bus specification was released by MIPI Alliance in 2016, as an improved communication protocol compared to its predecessor I2C, but the implementation of I3C, in a Data Center (Server) application was materialized until 2020.

- The main enhancements in I3C adopted by the DDR SPD function are:
  - Higher bit rate: up to 12.5MHz, compared to 100KHz-1MHz I2C SPD in prior DDR generations (125x to 12.5x higher bit rate).
  - Better IO electrical interface: Push-pull driver vs Open Drain only.
  - In-band interrupts (IBI) support – Not supported in DDR5 now, but looking for support in the future (or in other Server use cases).
  - In band Common Command Codes (CCCs) – Direct or Broadcast.
  - Reduced interface power (1.0V IOs).

Introduction cont'd

- The DDR5 SPD interface transitioned from I2C to MIPI I3C based on the following requirements for the next generation DDR DIMM technology:
  - Lower IO operating Voltage (as low as **1V** aligned to advanced process node)
    - DDR4 SPD IO voltage was **2.5V**
  - Higher interface bit rate (**400KHz** to **8-12.5MHz** in real applications) due to the increased number of devices per DIMM to be managed
    - DDR4 had **two** devices per DIMM vs **five** devices in DDR5
    - Considering 8 DIMMs per SPD segment, this is 16 vs 40 devices
  - Higher bit rate to reduce boot time (diminishing Memory Reference code execution time)

mipi® DEVCON

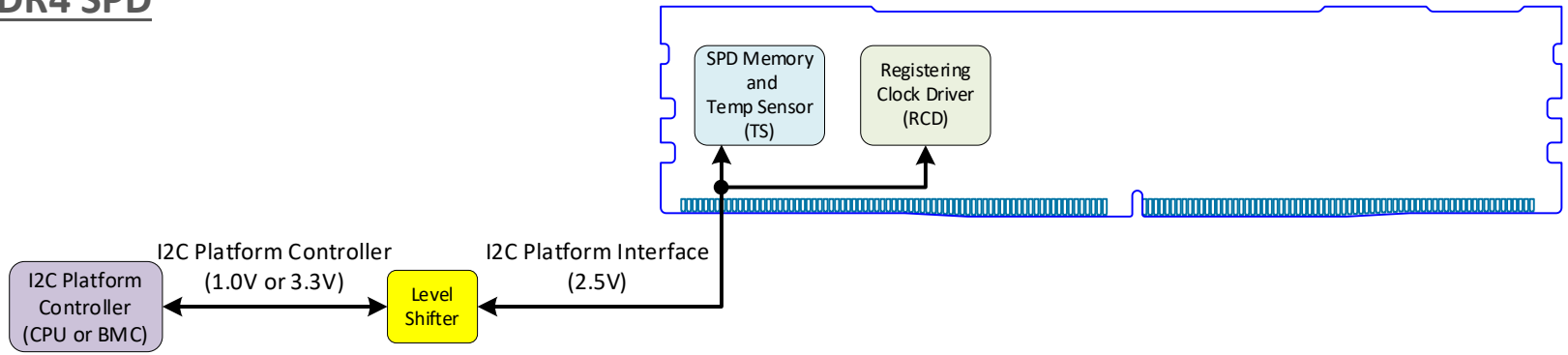
MIPI ALLIANCE DEVELOPERS CONFERENCE

28-29 SEPTEMBER 2021

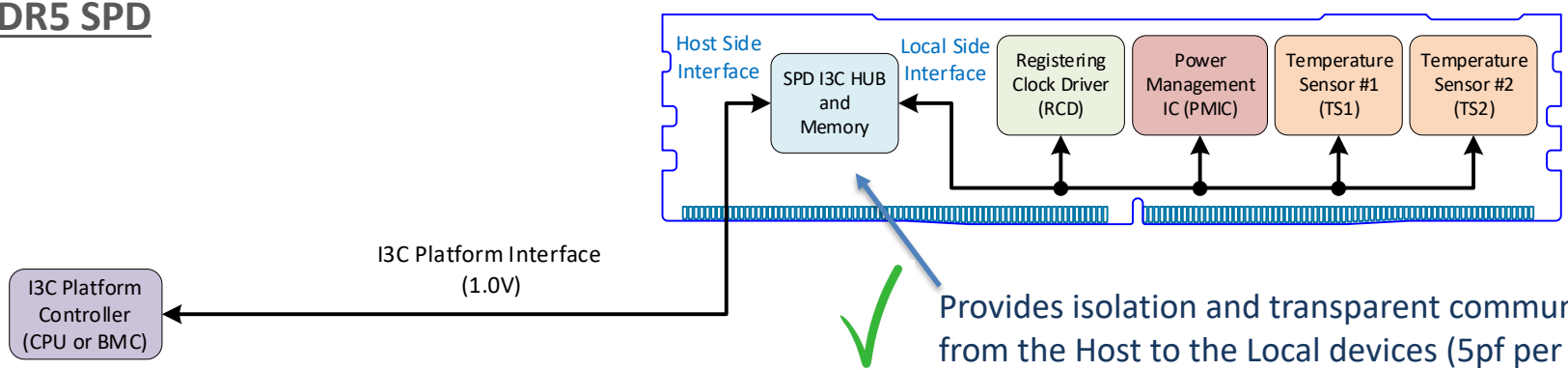
DDR5 SPD Server connectivity and bus characteristics

DDR4 vs DDR5 SPD DIMM Connectivity

- **DDR4 SPD**

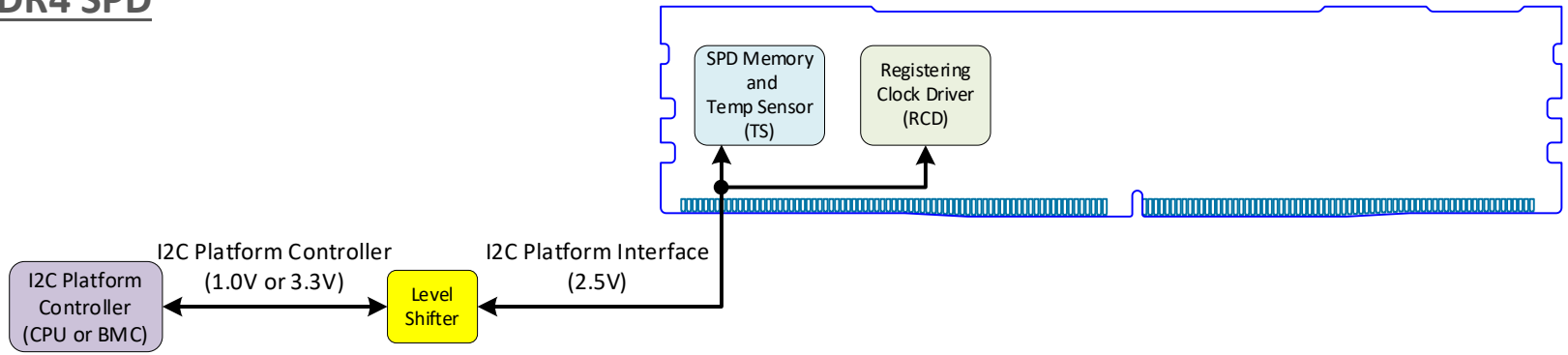


- **DDR5 SPD**

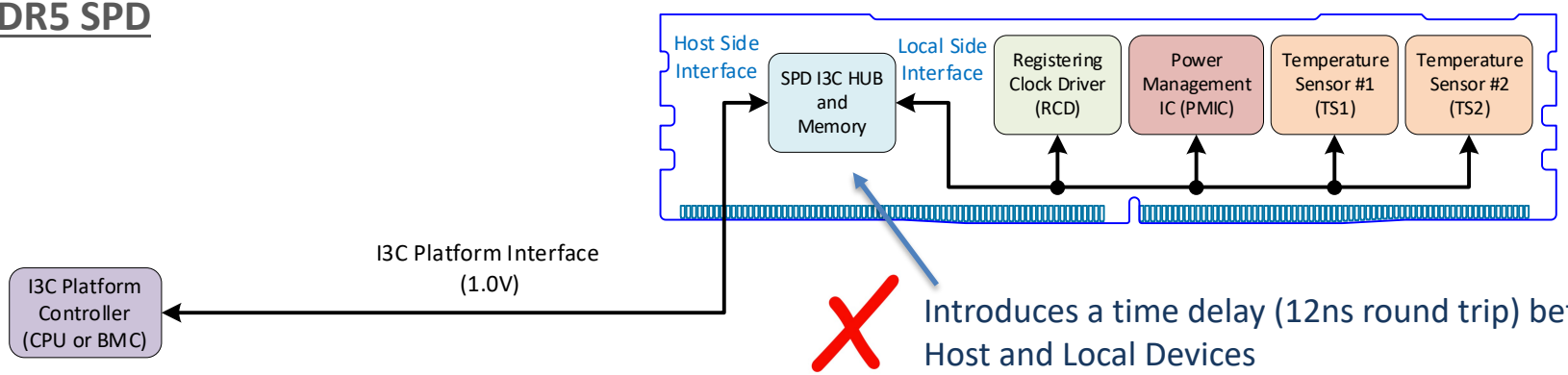


DDR4 vs DDR5 SPD DIMM Connectivity

- **DDR4 SPD**



- **DDR5 SPD**



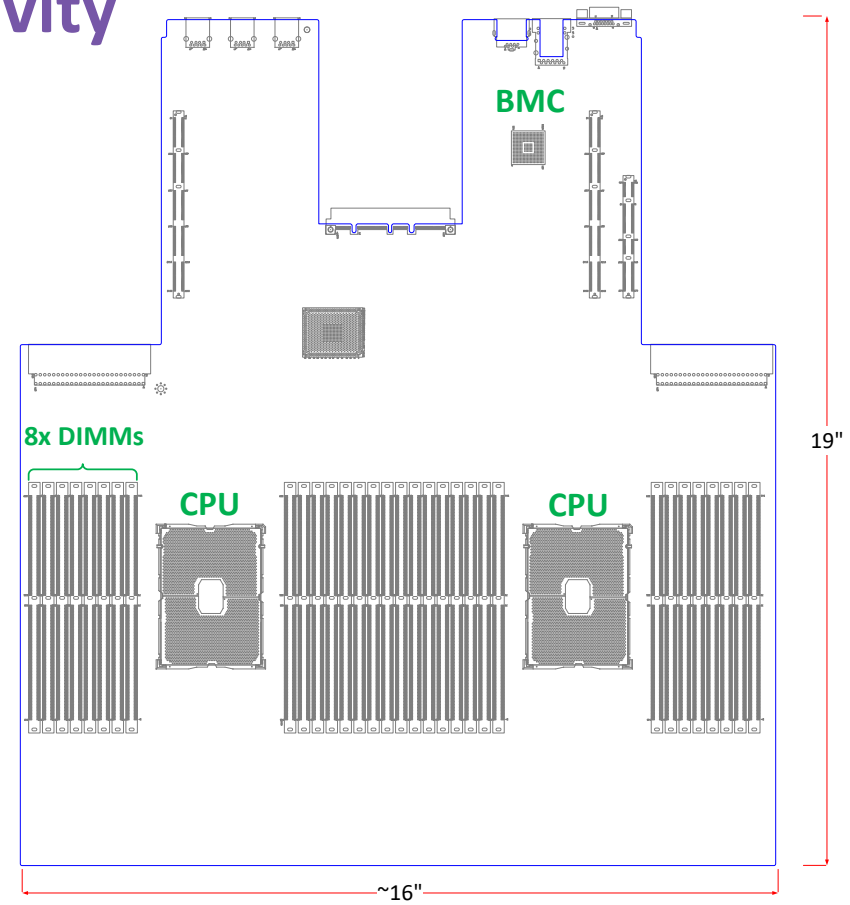
mipi® DEVCON
MIPI ALLIANCE DEVELOPERS CONFERENCE

28-29 SEPTEMBER 2021

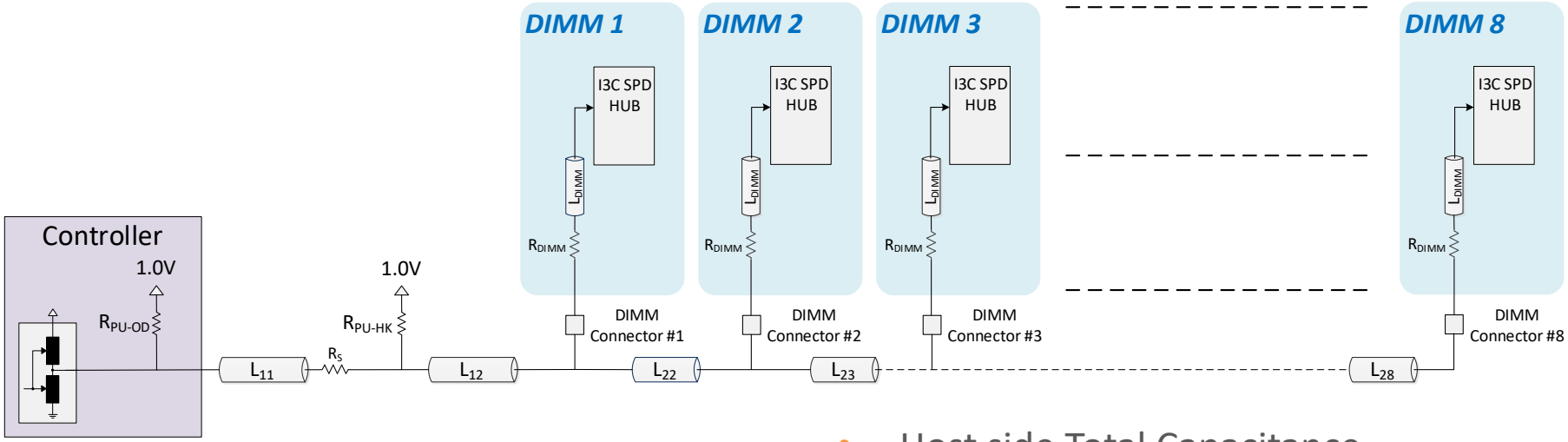
DDR5 SPD Bus Characteristics

DDR5 SPD Platform Connectivity

- Host side Server PCB routing
  - Total length could exceed 50”
    - Server motherboards are BIG: up to 16”x 19”
      - BMC controller is located at the North side
      - DIMMs are located at the South side
      - CPU to DIMM SPD routing has lower priority than high speed IO routing (DDR5, PCIe G4/G5, etc.)



Routing length and capacitance



- Host side Server PCB routing
  - From Controller to DIMMs (L_{11}+L_{12}+L_{2x}): ~25”
  - DIMM routing (L_{DIMM}): 3.5”/DIMM, 28” 8x DIMMs
  - Total PCB trace length: ~53”

- Host side Total Capacitance
  - Each device apports 5pF
    - 1 CPU + 8 HUBs =45pF
  - PCB routing is ~3pF/in
    - 53” * 3pF = ~159pF
  - **Totaling:**
    - **Dev (45pF) + PCB (53pF) =~204pF**

mipi® DEVCON
MIPI ALLIANCE DEVELOPERS CONFERENCE

28-29 SEPTEMBER 2021

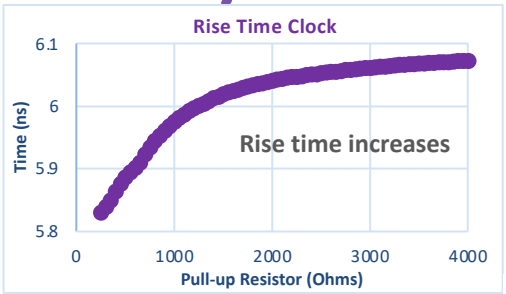
I2C and MIPI I3C Retro-compatibility Challenges

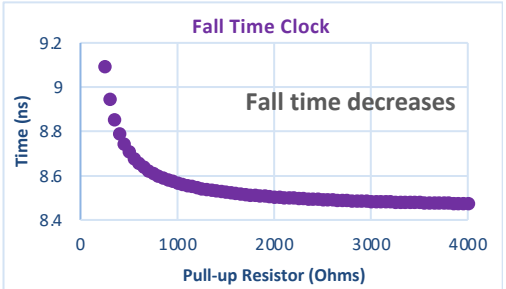
I2C and MIPI I3C Retro-compatibility Challenges

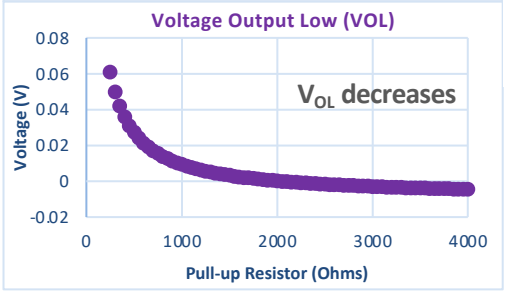
- There are three operating modes supported by the I3C protocol:
  - I2C mode with Open-Drain(OD) buffer class.
  - I3C mode with Open-Drain buffer class.
  - I3C mode with Push-Pull(PP) buffer class.
- The OD class requires a pullup to set a stable “Logic-high”.
  - The pullup is set accordingly with the total capacitance on the bus.
  - High capacitance busses requires a **“Strong pullup”**
    - **Strong pullup guarantees rise time specification to pass.**
- The PP class requires a High-Keeper pullup.
  - A “Weak pullup” is required to the target device with low current can pull SDA signal low within a minimum low period.
    - **Weak pull-up lessens the voltage levels disturbances**

MIPI I3C Basic Spec requires Dynamic pull-up control to switch between “strong pull-up” and “weak pull-up” to optimize open-drain and push-pull timing requirements.

Non-Dynamic Pullup impact in a 204pF bus







←Push-Pull

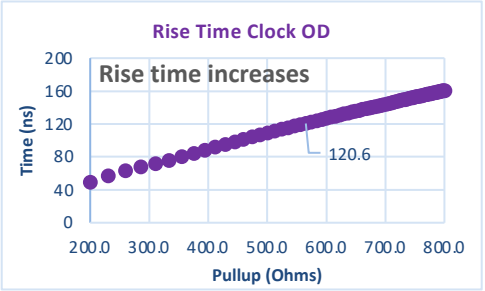
Open-Drain→

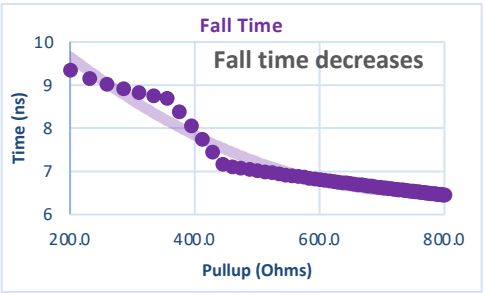
The Highest the PU

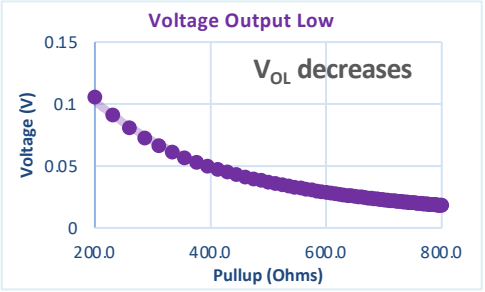
- VIH never reached with pull-up higher than 800Ω
  - Limit max operating frequency

- On-Board PU can guarantee an OD max operating frequency.
  - A parallel equivalent R_{PU_HK} || R_{PU_OD} of 333.3Ω
    - Rise time=75.3ns
  - A pullup ≥ 550Ω negatively affects both rise time and operating frequency

A trade-off among pull-up value, rise time and V_{OL} is required to meet the highest operating frequency





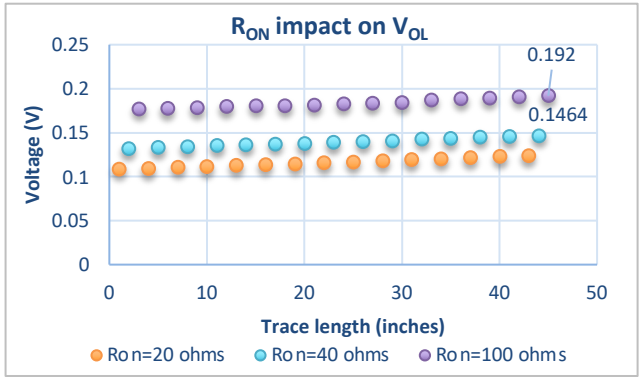


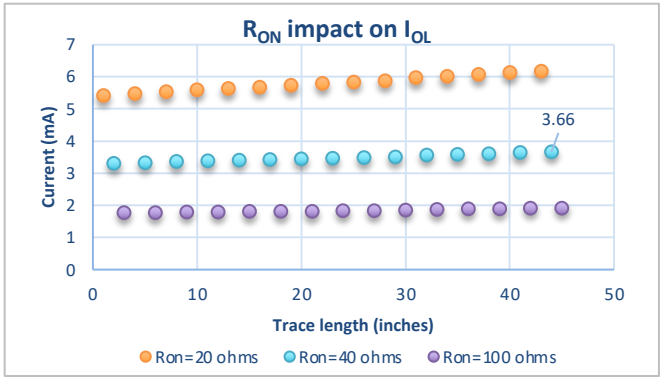
mipi® DEVCON
MIPI ALLIANCE DEVELOPERS CONFERENCE

28-29 SEPTEMBER 2021

Buffer R_{ON} design implications

Buffer R_{ON} value design implications





- The bigger the R_{ON} the higher the V_{OL} is:
  - Increasing trace length results in higher V_{OL}
    - With the longest trace length, V_{OL}= 192mV,
      - Assuming V_{IL}=0.3V then the transition margin is 108mV
        - » **Low transition margin can cause idle states**
- Setting the R_{ON} at 40Ω reduces the V_{OL}
  - With the longest trace length V_{OL}= 146mV,
    - If VIL=0.3V then the transition margin is 154mV
  - Notice that at the longest trace length with V_{OL}=146mV the **I_{OL} is 3.66mA**

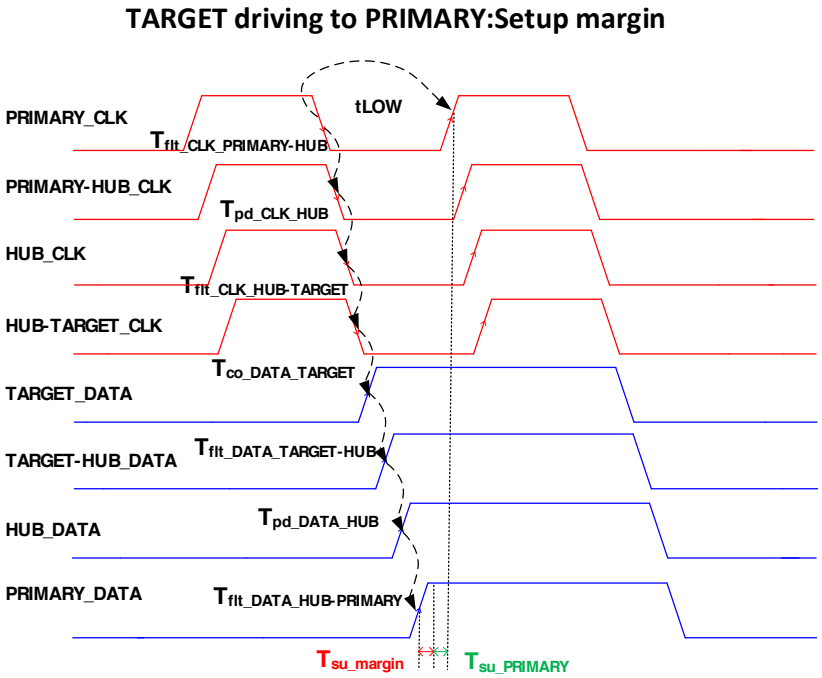
By limiting Ron into a max range of 40Ω ensures a healthy V_{OL} by setting a max I_{OL} bigger than 3mA

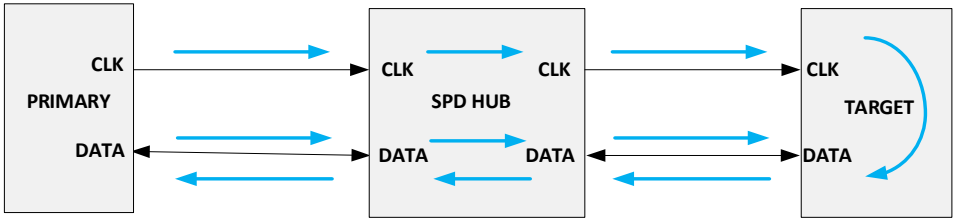
mipi DEVCON
MIPI ALLIANCE DEVELOPERS CONFERENCE

28-29 SEPTEMBER 2021

Critical time margin calculation

Critical time margin calculation



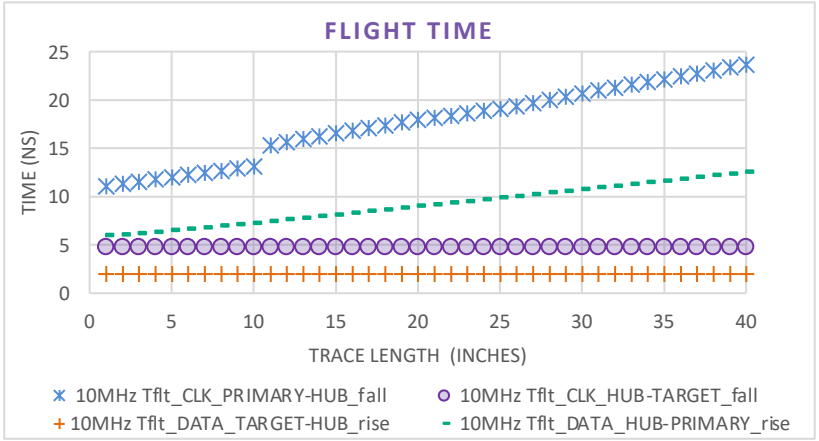


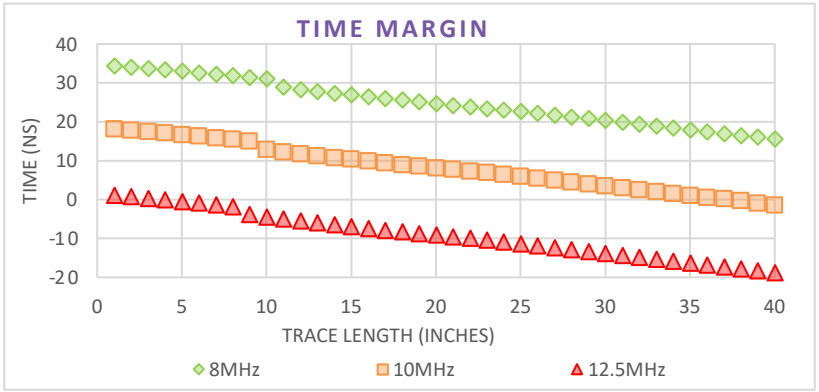
TARGET driving to PRIMARY: Setup margin

$$T_{su_{mar}} = t_{LOW} - (T_{flt_{CLK_{PRIMARY \rightarrow HUB_{fall}}}} + T_{pd_{CLK_{HUB}}} + T_{flt_{CLK_{HUB \rightarrow TARGET_{fall}}}} + T_{co_{DATA_{TARGET}}} + T_{flt_{DATA_{TARGET \rightarrow HUB_{rise}}}} + T_{pd_{DATA_{HUB}}} + T_{flt_{DATA_{HUB \rightarrow PRIMARY_{rise}}}}) - T_{su_{PRIMARY_{max}}}$$

Critical time margin calculation

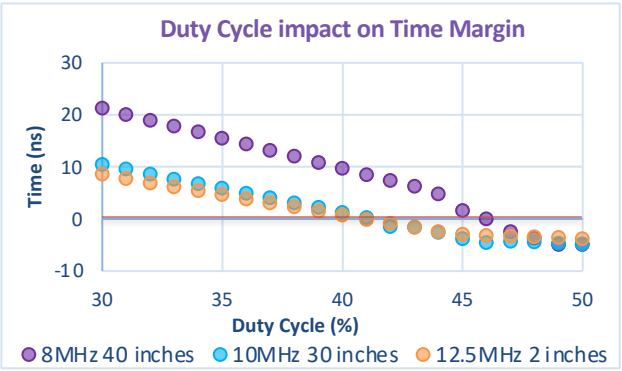
Frequency	10	MHz
Duty cycle	35	%
tLOW	**65**	ns
tflt_CLK_PRIMARY-HUB_fall	**19.1**	ns
tpd_CLK_HUB	**6**	ns
tflt_CLK_HUB-TARGET_fall	4.7	ns
tco_DATA_TARGET	12	ns
tflt_DATA_TARGET-HUB_rise	1.972	ns
tpd_DATA_HUB	**6**	ns
tflt_DATA_HUB-PRIMARY_rise	9.8	ns
tsu_PRIMARY_max	3	ns
Setup Margin	**2.253**	**ns**

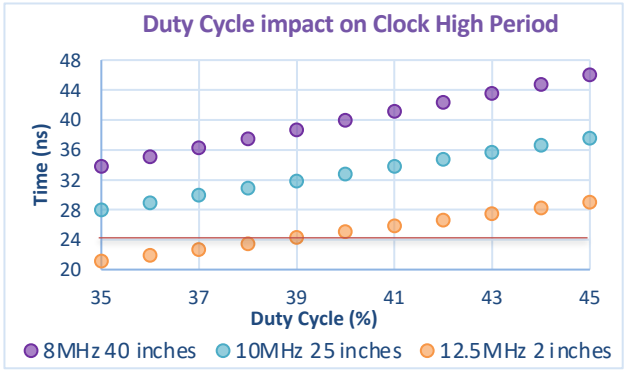


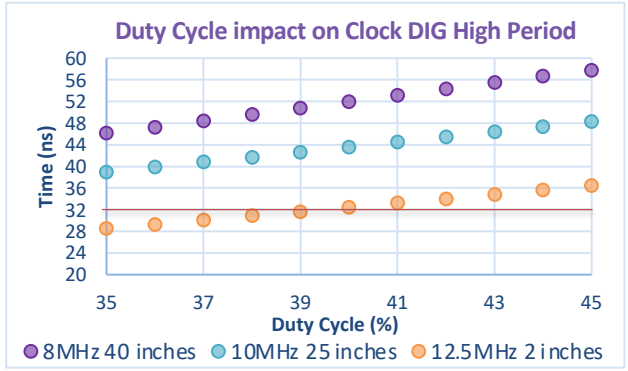


- The longer trace length the biggest flight time
- Inner device propagation delay plays a significant role in defining the operating frequency.
  - The highest the Tpd the bigger the time margin reduction.
- Increasing tLOW provides extra timing margin.

Frequency and AC/DC parameters impact







- Increasing duty cycle reduces tLOW, thus reducing the Time Margin.
- When reducing the Duty Cycle the tHIGH and tDIG_HIGH are affected.
  - Small Duty Cycle can produce a NOT PASS on tHIGH/tDIG_HIGH.

A correct selection of Duty Cycle provides extra time margin to complete the setup transaction, granting higher operating frequency.

From MIPI I3C Spec t_{HIGH} min 24ns, t_{DIG_HIGH} min 32ns

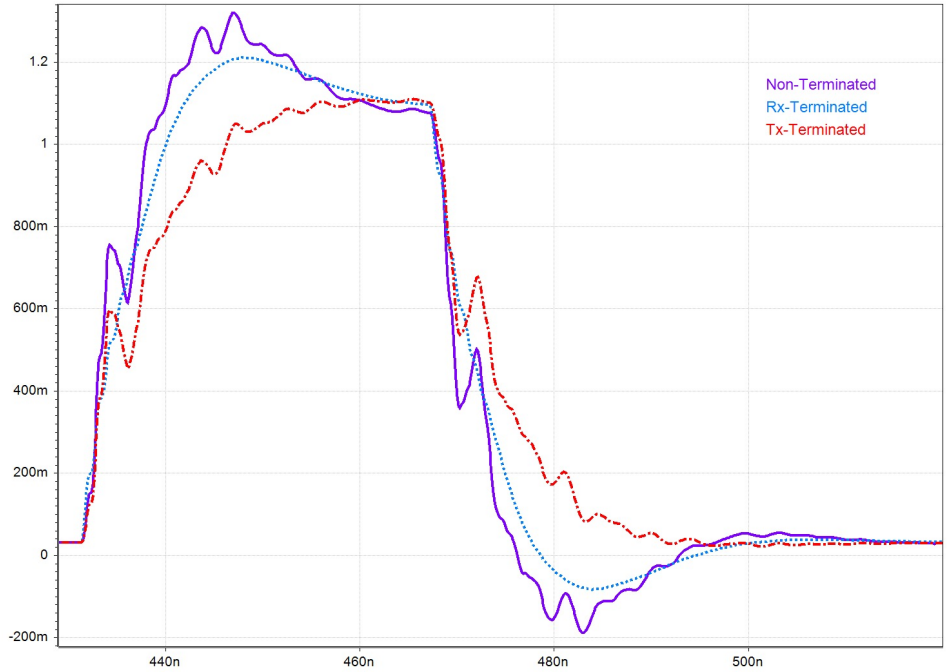
mipi® DEVCON
MIPI ALLIANCE DEVELOPERS CONFERENCE

28-29 SEPTEMBER 2021

Non-monotonic signal behavior

Non-monotonic signal behavior

- Termination effect on transmission lines
  - Non-terminated circuit:
    - Signal bounces back and forth between the driver and the receiver.
  - Tx-terminated circuit:
    - Reduces drive strength
    - Increases propagation delay
    - Limits buffer capabilities
  - Rx-terminated circuit:
    - Reduces bouncing effect
    - Increases propagation delay



mipi DEVCON
MIPI ALLIANCE DEVELOPERS CONFERENCE

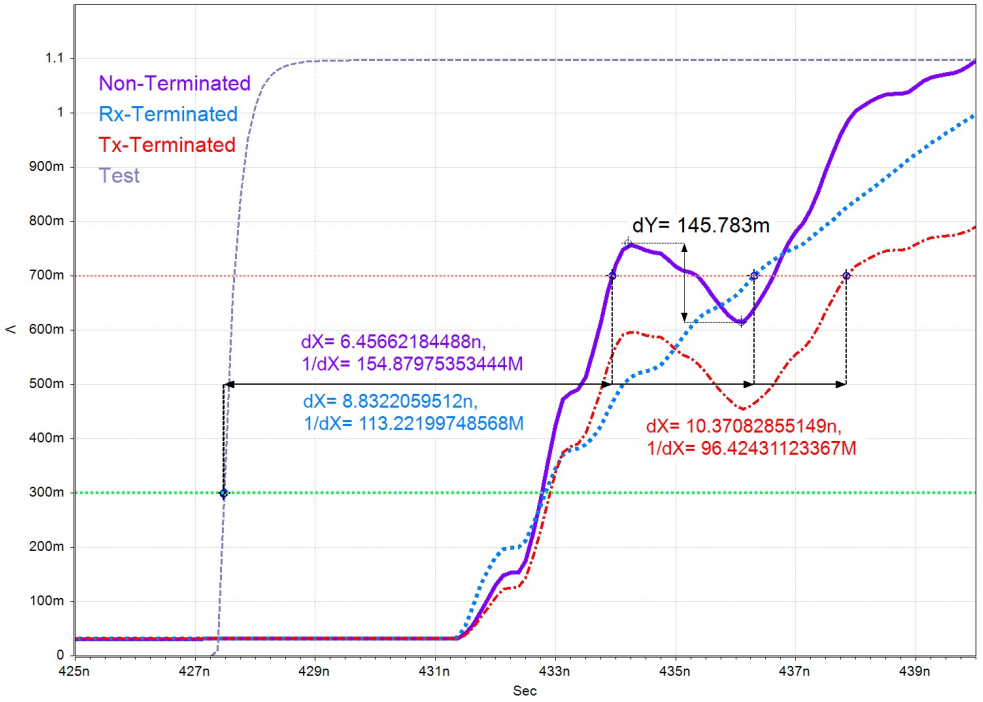
28-29 SEPTEMBER 2021

Slope reversal capability and timing improvement

Slope reversal capability and timing improvement

- With the non-deterministic loading of an unterminated bus, there can be reflections on the bus causing slope reversal on the Rx signal.
- By sampling at the first threshold is possible to filter Non-Monotonicity's; Schmidt triggered inputs
  - Non-terminated VS Rx-Terminated: **Improves 2.3ns**
  - Non-terminated VS Tx-Terminated: **Improves 3.92ns**

Slope reversal capability provides additional time margin that improves operating frequency and prevent false logic states.



mipi® DEVCON
MIPI ALLIANCE DEVELOPERS CONFERENCE

28-29 SEPTEMBER 2021

Summary

Summary

- I3C Applications in Server systems (such as DDR5 SPD) are dealing with higher Bus capacitance than the max limit assumptions in MIPI spec (for 12.5MHz capable buses).
- Higher Bus capacitance applications can be mitigated by using good Buffer Drive strength, strong open-drain class pull-up, and HUB isolation circuits.
- A dynamic pullup operation allows to drive the interoperability challenges between the open-drain and push-pull operating modes; by enabling higher operating frequencies on both modes and limiting critical parameters to meet latest specification.
- Strong buffers tend to increase signal energy reflections, specially in complex topologies resulting with slope reversal conditions at Devices' Inputs.
- Schmitt trigger capable inputs are required in order to mitigate slope reversal conditions when dealing with high bus capacitance and strong buffers

mipi®
DEVCON
MIPI ALLIANCE DEVELOPERS CONFERENCE

28-29
SEPTEMBER
2021

THANK YOU!