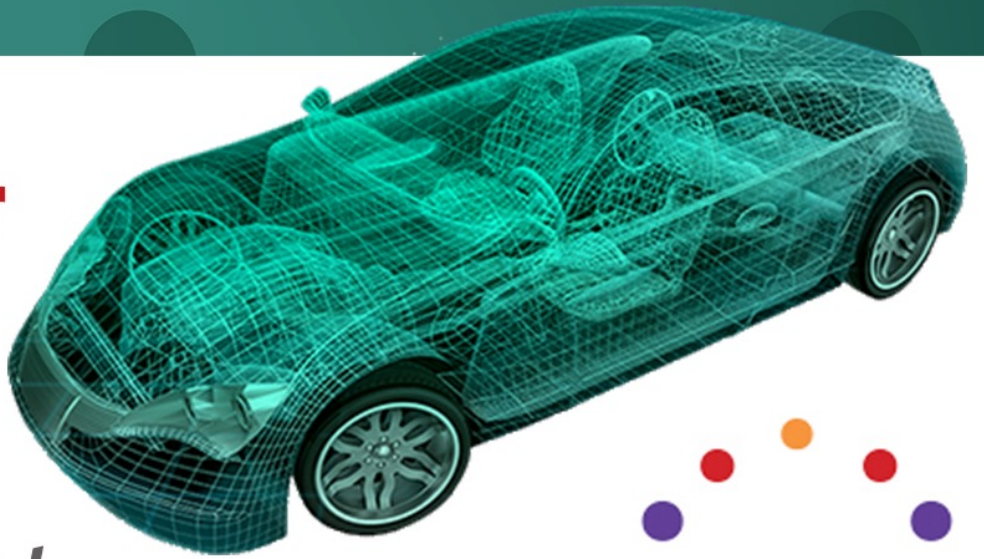
MIPI Automotive Workshop

15 November 2022



Live Virtual Event

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IF IT'S NOT MIPI, IT'S NOT MOBILE

MIPI A-PHY®:

Continuing to Drive Innovation for In-Vehicle Connectivity

Raj Kumar Nagpal / Edo Cohen

MIPI A-PHY® Working Group Co-Chairs

15 November 2022

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Agenda

- A-PHY v1.0 / v1.1
- Power over A-PHY (PoA)
- A-PHY v2.0
- A-PHY in Zonal Architecture
- A-PHY for Modern Automotive Cockpit Display
- A-PHY Compliance Program

A-PHY v1.0 / v1.1

MIPI A-PHY – MASS Cornerstone

First industry-standard asymmetric SerDes physical layer specification targeted for ADAS/ADS and infotainment applications

About A-PHY

(v1.0 released in Sep 2020)

- Direct coupling to native MIPI CSI-2® / MIPI DSI-2℠/ VESA DisplayPort™ and eDP protocols
- High noise immunity, ultra low PER (< 10^{-19})
- Supports bridge-based and endpoint integration
- Support for automotive coax and SDP channels
- Power over cable
- Built-in functional safety according to ISO 26262
- Adopted by IEEE as IEEE 2977-2021

A-PHY v1.1 Enhancements

(released Dec 2021)

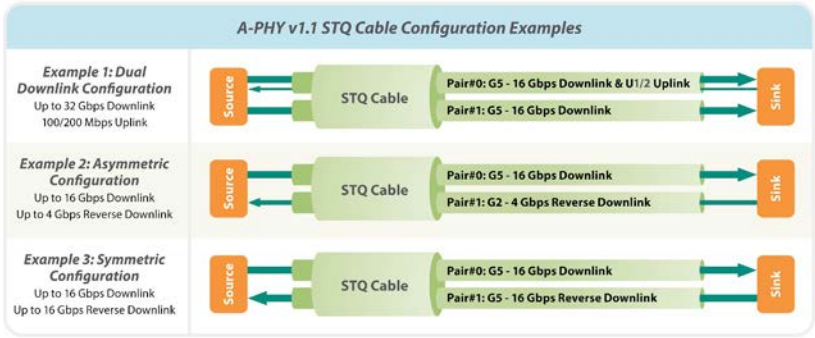
- Increased support for lower cost legacy cables
- Double uplink data rate
- Star quad cable support, enabling lower cost dual lane operation, for up to 32 Gbps data rate

MIPI A-PHY Performance

A-PHY v1.1 enhancements shown in orange

Uplink Gear Data Rate	Modulation	Modulation Bandwidth (MHz)	Max Net App Data Rate (Mbps)
U1 100 Mbps	NRZ-8B/10B	50	55
U2 200 Mbps	PAM4-8B/10B	50	125

Downlink Gear Data Rate	Modulation	Modulation Bandwidth (GHz)	Max Net App Data Rate (Gbps)
G1 2 Gbps	NRZ-8B/10B	1	1.5
	PAM4 (Optional)	0.5	1.8
G2 4 Gbps	NRZ-8B/10B	2	3
	PAM4 (Optional)	1	3.6
G3 8 Gbps	PAM4	2	7.2
G4 12 Gbps	PAM8	2	10.8
G5 16 Gbps	PAM16	2	14.4

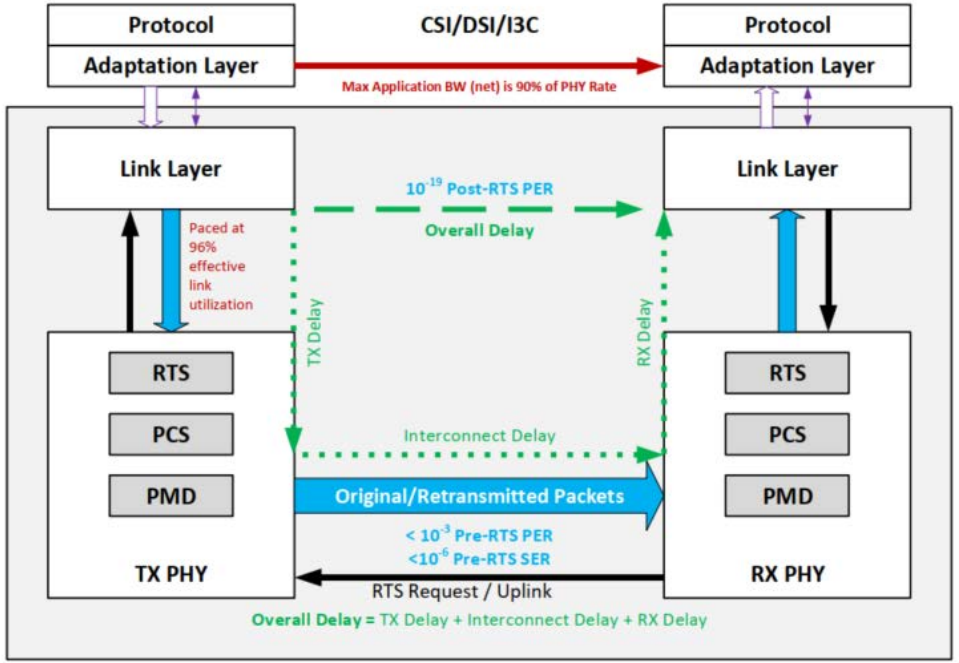


PER: Packet Error Rate

What Makes MIPI A-PHY So Robust and Efficient?

RTS + NBIC

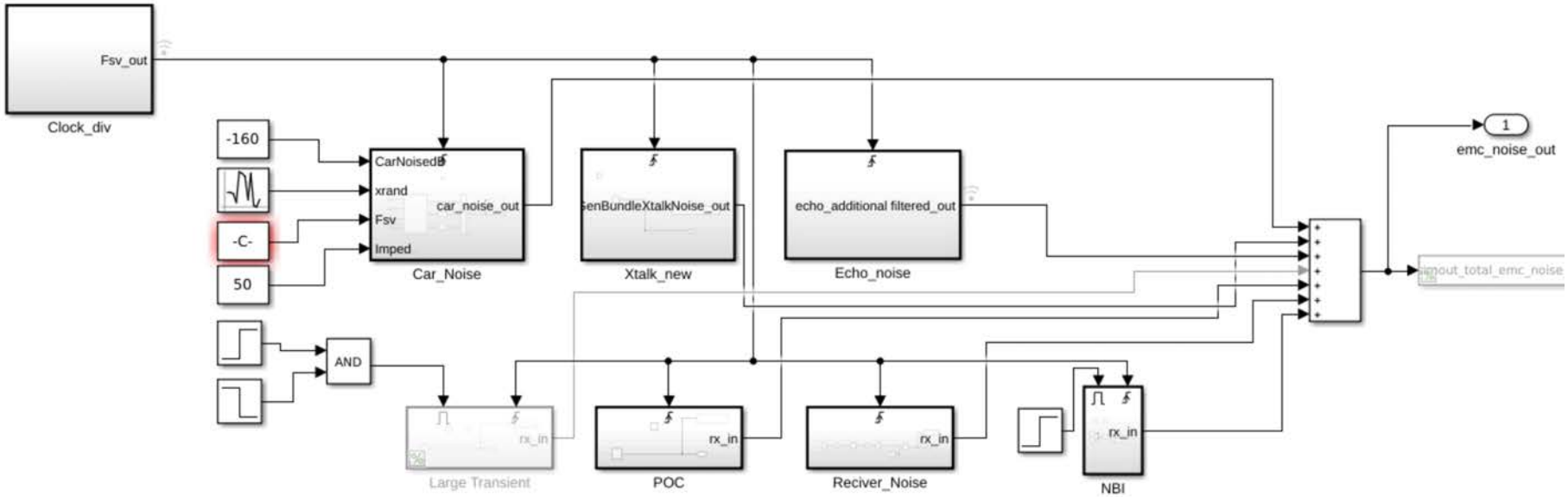
- **Time bounded local PHY-level retransmission**
  - Only within pre-defined “Overall Delay” (~6µs@G5)
  - Local: Transparent to the upper layers
  - Local: Happens within a single A-PHY hop
- **Dynamic modulation for retransmitted packets with better error resistance**
- **Highly resilient**
  - Overcomes large thousands symbols-long error bursts
  - Multiple 10s mV, instantly attacking NBI peaks
- **High reliability → PER < 10^{-19}**
- **Low overhead → 90% net data rate**



High throughput automotive links are EMI-limited — not AWGN limited

NBI: Narrow Band Interferences
NBIC: Narrow Band Interferences Canceller
PCS: Physical Coding Sub-Layer
PMD: Physical Media Dependent
RTS: Re-Transmission Sub-Layer
AWGN: Additive White Gaussian Noise

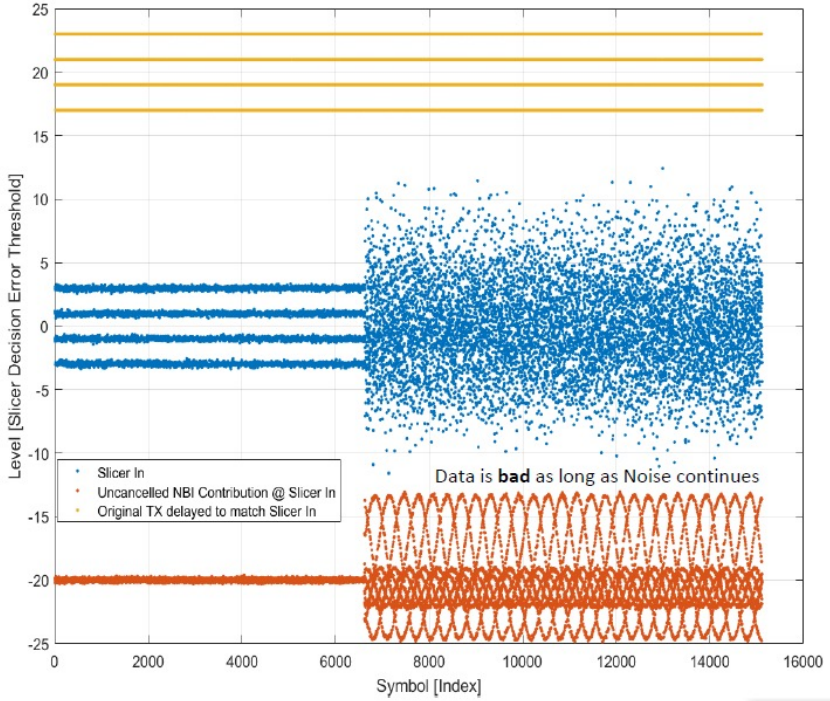
EMC Noises Part of Model as Per Spec



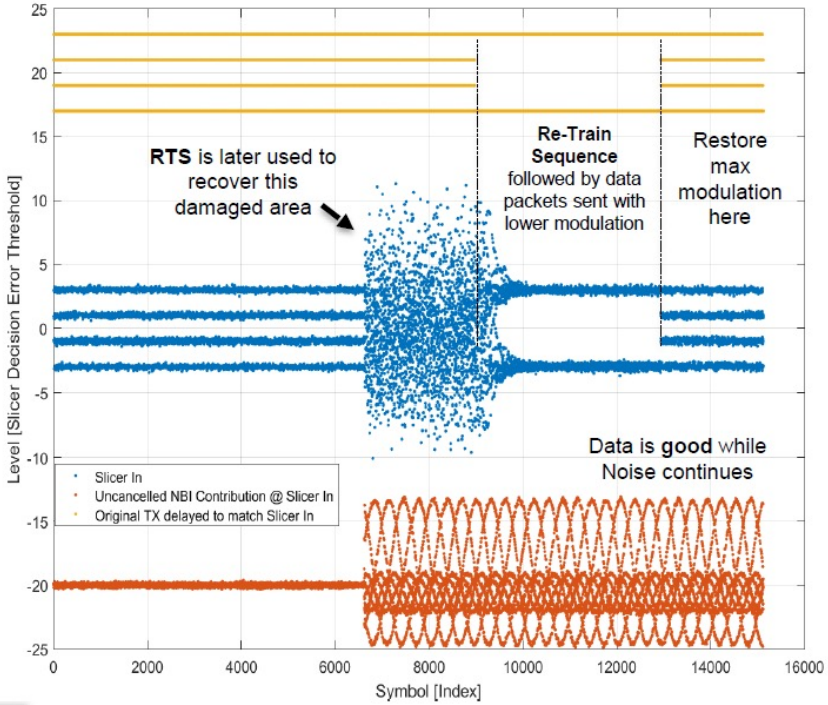
To Speed Up/Ensure JITC Convergence, JITC Re-training Is Used

Example: 4GBaud PAM4, 40mVpeak 3 Tone NBI, instant attack, without re-training

Without Re-training, Canceller cannot Overcome NBI Impact on Slicer

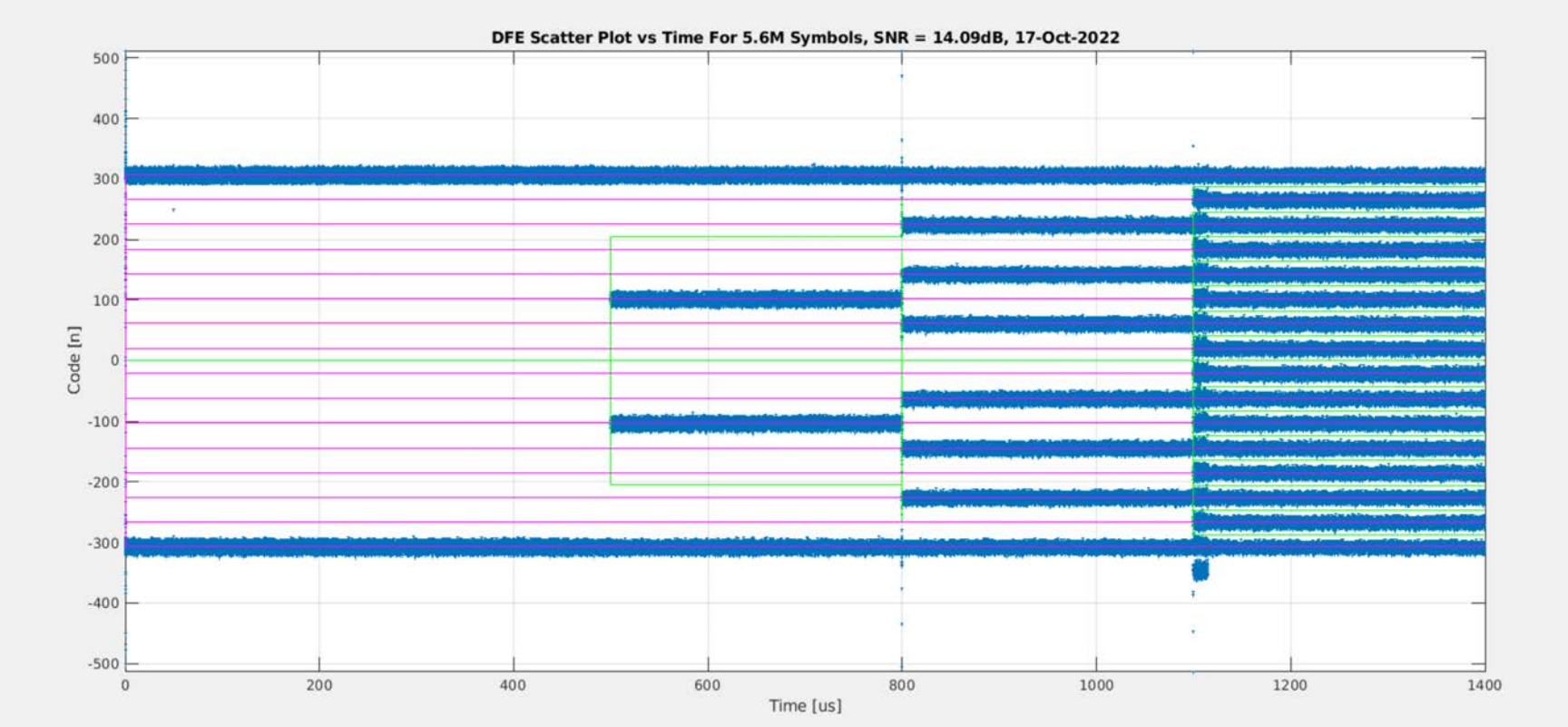


With Re-Training, Usage of "Known Data" Slicing Allows Canceller to Quickly Converge to Remove NBI Impact on Slicer



JITC: Just In Time Canceller

PAM2/4/8/16 Scatter Results A-PHY v1.0 / 1.1

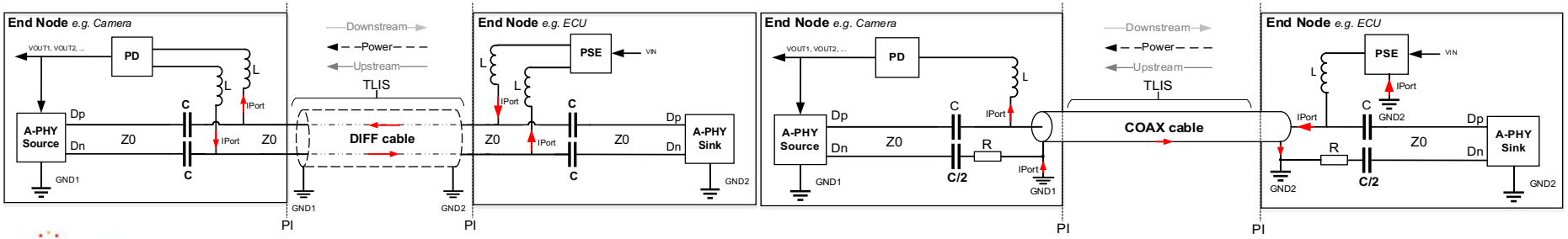


Power over A-PHY

Power over A-PHY – PoA

- A-PHY v1.0 / v1.1 include a section on PoA
- Separate specification is being developed to provide better flexibility and enhanced capabilities without impacting the A-PHY specification
  - This specification will be backward compatible with current definitions
- A-PHY v2.0 will be aligned with the new PoA specification
- The new PoA specification introduces new power types A-PHY link can support to enable power over cable to multiple types of devices and use cases

		PoA System Type					
		Type 1	Type 2	Type 3	Type 4	Type 5	
		12 V	12 V	24 V	24 V	48 V	
		Unregulated	Regulated	Unregulated	Regulated	Regulated	
	Requirement	Class 1 [9]	Class 3 [9]	Class 5 [9]	Class 7 [9]	Class 9 [9]	**Additional Information**
1	$VPSE_{max}$ (V) [1]	18	18	36	36	60	See ***Section 7.2.2***
2	*$VPSE\_OC_{min}$ (V)* [2]	*8.4*	*14.4*	*12*	*26*	*48*	
3	$VPSE_{min}$ (V) [3]	8	14.4	11.7	26	48	
4	$Icont_{max}$ (mA)[4]	293	500	500	500	500	See ***Section 7.2.4*** See Equation 5 for I_{CONT} when Vpse > Vpsemin.
5	$Ppse_{min}$ (W)[5]	2.34	7.2	5.85	13	24	See ***Section 7.2.5*** See Equation 6 for Ppse when Vpse >$Vpse_{min}$.
6	VPD_{min} (V) [6]	6.83	12.4	9.7	24	46	See ***Section 8.3.3***
7	VPD_{max} (V) [7]	18	18	36	36	60	
8	PPD_{max} (W) [8]	2	6.2	4.85	12	23	See ***Section 8.3.1***



A-PHY v2.0

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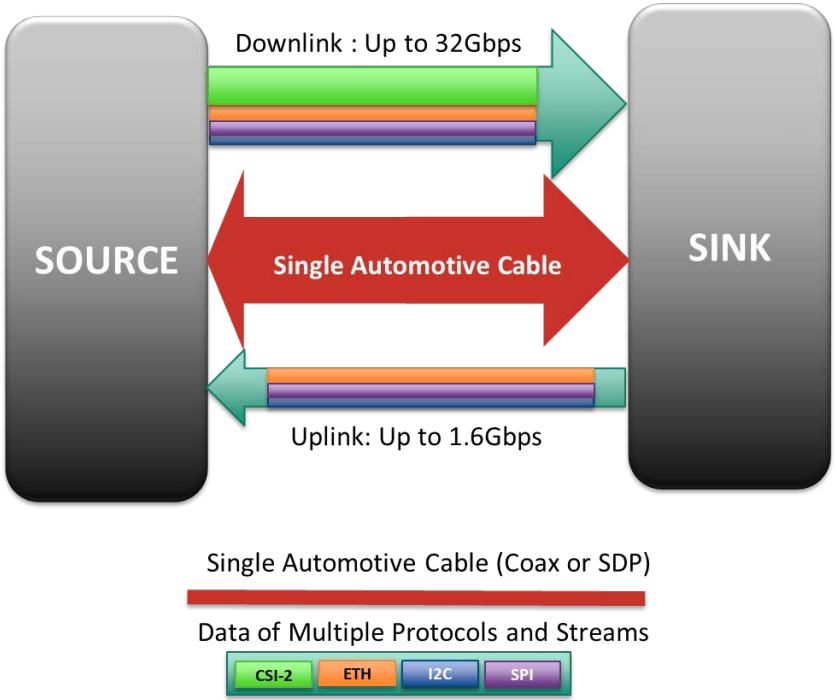
A-PHY v2.0 – Main Goals

- **Specification update focused on emerging architecture and use cases**
  - Zonal architecture and SDV (software-defined vehicle)
  - Modern automotive cockpit environments
- **Maintain backward compatibility to A-PHY v1.0 / v1.1**
  - A-PHY v1.0 / v1.1 will be forward compatible with next A-PHY specification
- **No changes in the upper layers**
  - Easy migration with minimal impact at system level
- **Maintain high EMC resilience and low packet error rate**

A-PHY Next Generation – Main New Features

- **Double downlink throughput**
  - Up to **32Gbps** (28.8Gbps net data rate) per single lane
- **Uplink throughput increase**
- **Up to 1.6Gbps** (1.166Gbps net data rate)
- **Enhance interface support**
  - Add 1Gb Ethernet support (based on the new uplink BW)
  - Other interfaces may be added based on market demand
- **Expand A-PHY secure control**
  - Enable support of a secure A-PHY network



Downlink Gear Table (A-PHY v1.1)

Downlink Gear	Modulation	Modulation Bandwidth [GHz]	Data Rate [Gbps]	Max Net App Data Rate [Gbps]
G1	NRZ-8B/10B	1	2	1.5
	PAM4	0.5		1.8
G2	NRZ-8B/10B	2	4	3
	PAM4	1		3.6
G3	PAM4	2	8	7.2
	NRZ-8B/10B	4		6
G4	PAM8	2	12	10.8
G5	PAM16	2	16	14.4

Downlink Gear Table (A-PHY v2.0)

Downlink Gear	Modulation	Modulation Bandwidth [GHz]	Data Rate [Gbps]	Max Net App Data Rate [Gbps]
G1	NRZ-8B/10B	1	2	1.5
	PAM4	0.5		1.8
G2	NRZ-8B/10B	2	4	3
	PAM4	1		3.6
G3	PAM4	2	8	7.2
	NRZ-8B/10B	4		6
G4	PAM8	2	12	10.8
G5	PAM16	2	16	14.4
G6	PAM8	4	24	21.6
G7	PAM16	4	32	28.8

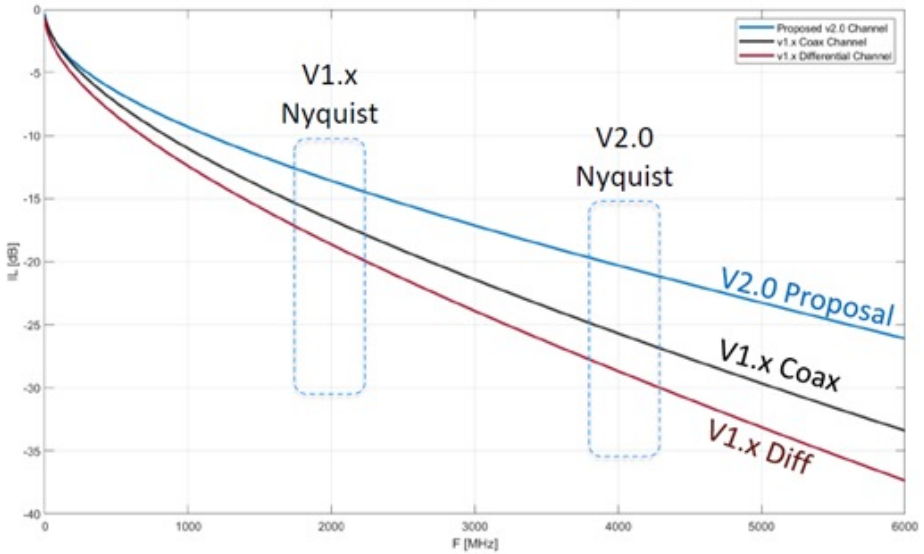
Uplink Gear Table (Initial Proposal)

Uplink Gear	Modulation	Modulation Bandwidth [MHz]	Data Rate [Mbps]	Max Net App Data Rate [Mbps]
U1	NRZ-8B/10B	50	100	53
U2	PAM4-8B/10B	50	200	125
U3	PAM4-8B/10B	400	1600	1166

A-PHY v1.x and v2.0 Channels

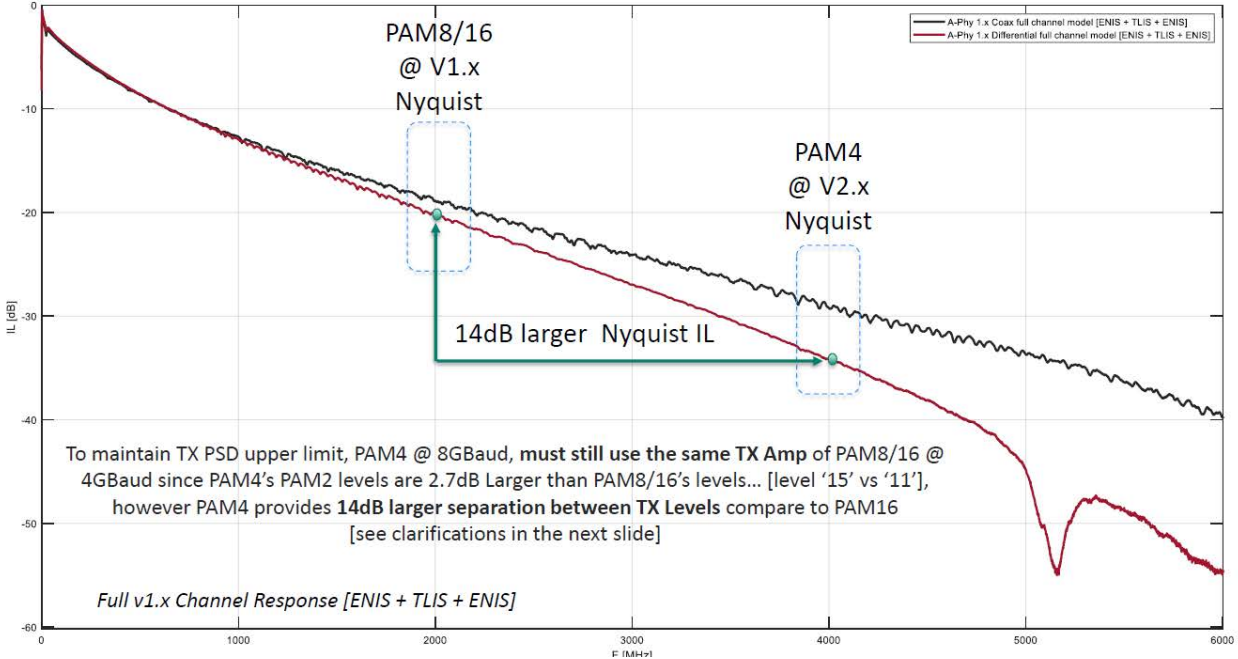
Proposed Link Segment (TLIS) For G6 & G7

- Single IL limit , reuse IEEE 802.3cy channel $\quad Insertion\ loss(f) \le 0.00135(f_{MHz}) + 0.3564(f_{MHz})^{0.45} + 0.495\left(\frac{f_{MHz}}{7500}\right)^{6}$ (dB)
- New channel IL @ 4GHz is only slightly higher than V1.x channel at 2GHz
- To maintain TX PSD upper limit of -92dBm/Hz, G6/7, which operate at 8GBaud, will use **TX Amp which is 3dB larger** than in G4/5 @ 4GBaud



Optional G4/G5 with PAM4 @8GBaud

Optional G4/5 Using PAM4 @ 8GBaud over v1.x Channels

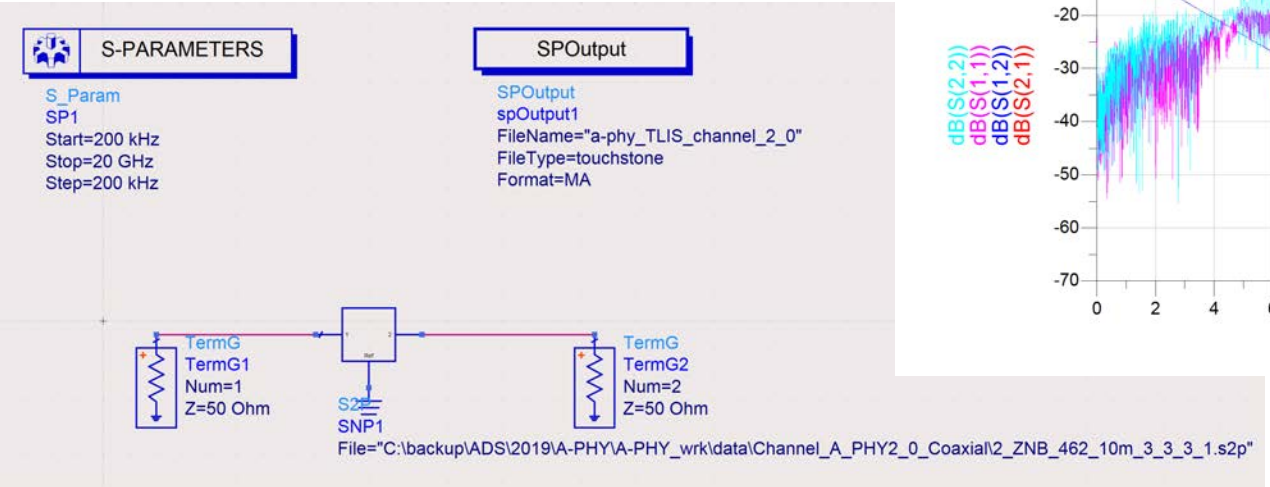


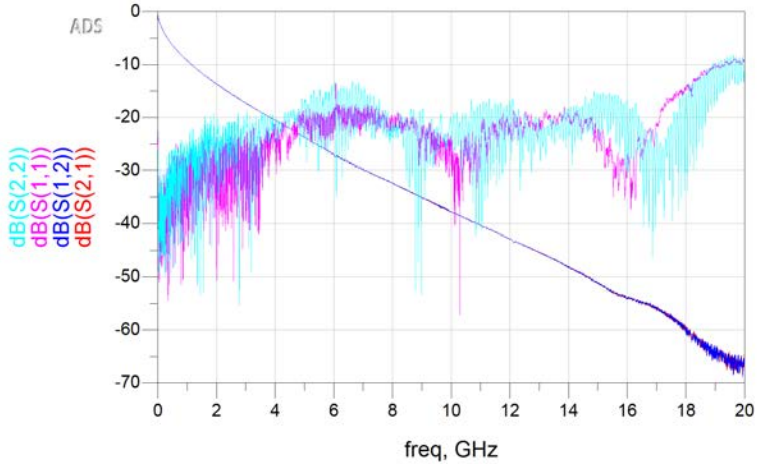
A-PHY V2.0 – Downlink Gear Table

Downlink Gear	Modulation	Nyquist Frequency [GHz]	Data Rate [Gbps]	Max Net App Data Rate [Gbps]
G1	NRZ-8B/10B	1	2	1.5
	PAM4 [Opt]	0.5		1.8
G2	NRZ-8B/10B	2	4	3
	PAM4 [Opt]	1		3.6
G3	PAM4	2	8	7.2
G4	PAM8	2	12	10.8
G5	PAM16	2	16	14.4
	PAM4 [*Opt]	4		
G6	PAM8	4	24	21.6
G7	PAM16	4	32	28.8

A-PHY v2.0 Channel Model

- Lab measured S-parameters





A-PHY in Zonal Architecture

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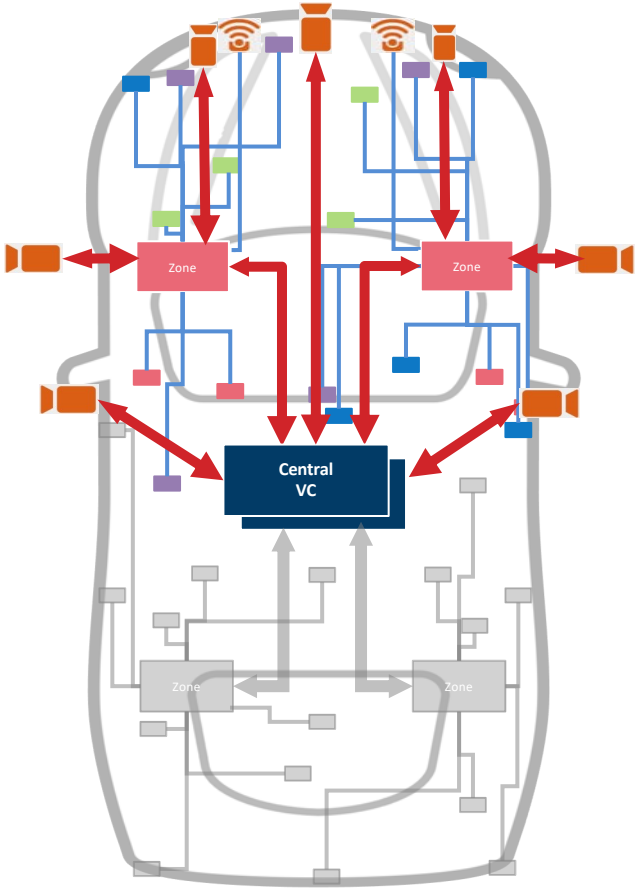
Zonal Architecture

- **Drivers**
  - Reducing wiring harness complexity and weight
  - Centralized and scalable compute unit
  - Reduced number of ECU and simpler hardware abstraction
  - Simplified OTA updates and upgrades for Software Defined Vehicle (SDV)
  - Software compatibility and Interface flexibility

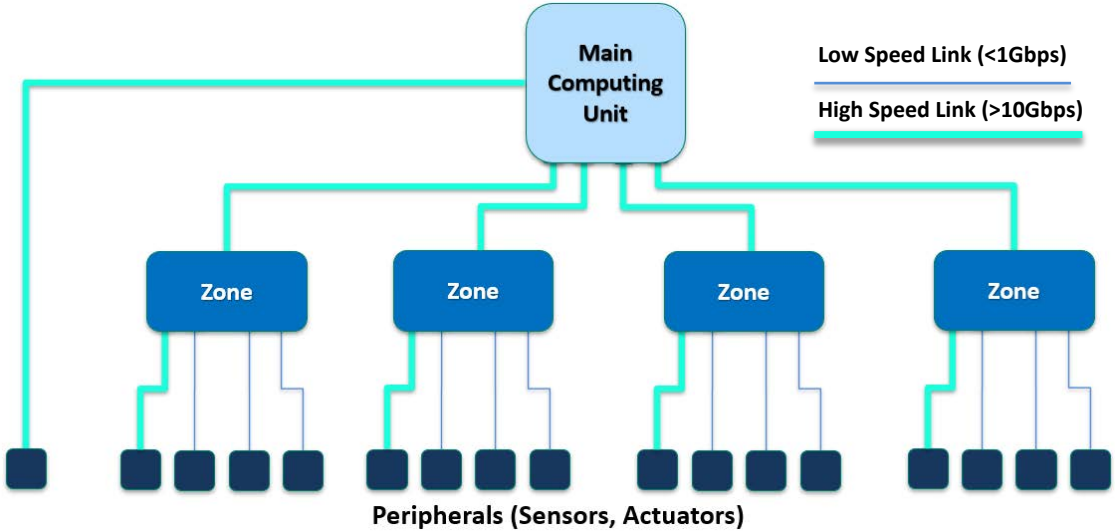
- **Guidelines**
  - Aggregation of nodes in spatial proximity by Zone ECUs
  - Central vehicle computer (VC)
  - High-rate backbone
  - Shared infrastructure across functional domains

- **Challenges**
  - Heterogeneous technologies
  - Interoperability
  - Topology depth
  - Bandwidth
  - Latency
  - Efficiency



Zonal Architecture – High-Level Structure

- Strong demand for reductions of harness complexity and weight
- Data aggregation in zone with no change of data format(s) desired
- Hybrid connectivity – direct or via zone
- **Data processing centralized**
  - Improved perception performance
  - Easier update and SW maintenance
  - Improved flexibility/scalability



Architecture Optimization

- **Future looking -** Majority of high-speed links in the vehicle connect **asymmetric** edge devices
- **Flexible -** Central VC should be able to connect natively, both to aggregators or directly to edge devices
- **Optimized -** Standardized communication technology (PHY and protocol) should be integrated into the high-speed edge devices
- **Backward compatible -** legacy interface gateways and low-bandwidth located in the spatial area of the zonal aggregators, may use a 100Mbps/1Gbps Ethernet backbone.

A-PHY is the perfect fit Zonal Architecture optimization

- Resilient asymmetric high-speed link (up to 32Gbps per lane) with clear forward roadmap
- Only PHY natively integrated to edge devices and aggregators (e.g., MIPI CSI-2)
- Multiplex both the high-speed asymmetric communication and the 1Gbps Ethernet backbone over the same cable.

A-PHY for Modern Automotive Cockpit Displays

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Modern Automotive Cockpit Displays

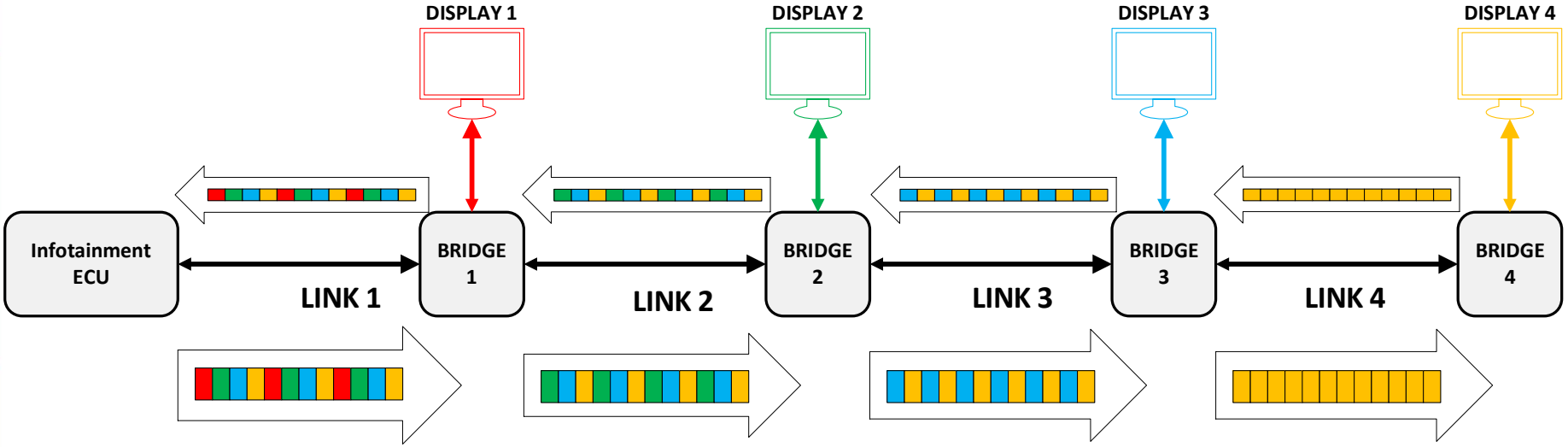
Display Type	Example Size (Inches)	Example Resolution
Left and Right-Side Mirror Displays	7”	1280x800
Driver Instrument Display	12.3”	3840x1440
Center Information Display	12.3”	3840x2160
Extended Co-Driver display	12.3”	3840x2160
Lower Control Display	12.4”	3840x2160

Modern Automotive Cockpit Displays

- Multiple connectivity schemes including daisy chain
- Up to **64Gbps** non-compressed data in single port
  - Up to **192Gbps with VESA DSC compression** with no additional overhead in single port
- Flexible uplink up to 1.6Gbps
  - Enable internal DMS[2] camera
- Ultra low PER[1] for the entire vehicle lifespan (zero errors)
- End-to-end functional safety
- End-to-end advanced layered security
- Multiple protocol support (e.g., MIPI DSI®, VESA DisplayPort)

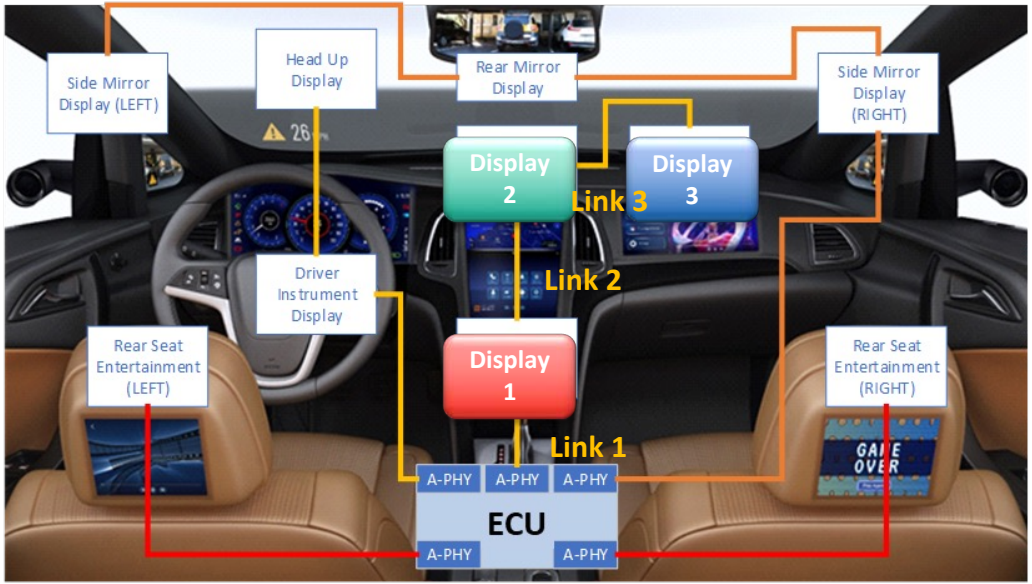
(1) PER – Packet Error Rate
(2) DMS – Driver Monitoring System

Daisy Chain – General Structure Example



Daisy Chain Example

Config	Display 1 (LCD)	Display 2 (CID)	Display 3 (CDD)	Total BW Gbps
1	3840x2160	3840x2160	3840x2160	37.6
2	3840x2160	5120x2160	5120x2160	45.8
3	7680x2800	7680x2800	7680x2800	96.5



Config	DSC	Actual BW Gbps	Link 1	Link 2	Link 3
1	-	37.6	DL-G6	G7	G5
	+	12.5	G5	G4	G3
2	-	45.8	DL-G7	DL-G6	G6
	+	15.3	G6	G5	G3
3	-	96.5	Requires compression		
	+	32.2	DL-G6	G6	G4

Gear	Single Lane BW (Gbps)	Dual Lane BW (Gbps)
G1	2	4
G2	4	8
G3	8	16
G4	12	24
G5	16	32
G6	24	48
G7	32	64

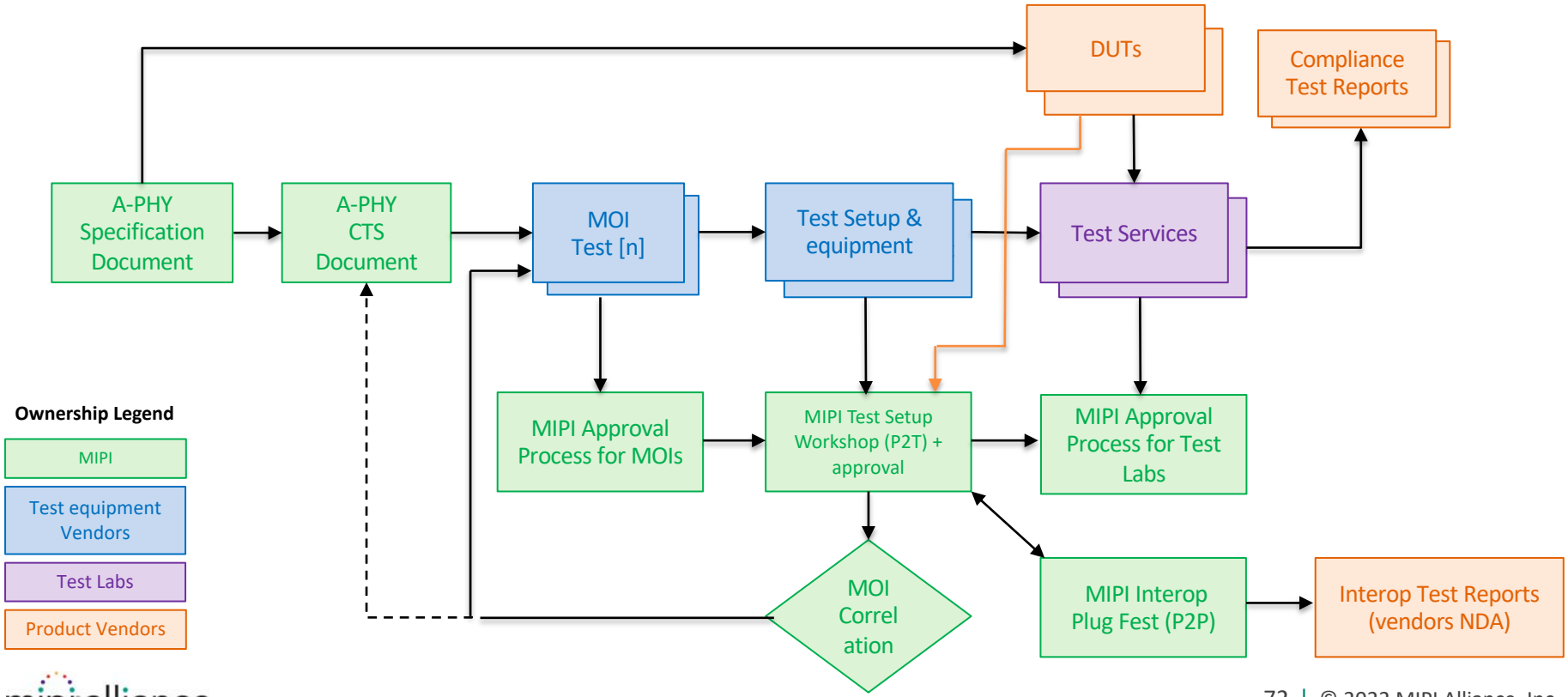
Assumptions: Uncompressed 24-bit/pixel or DSC 8bpp, 60fps, CVT-2 Blanking overhead
DSC: VESA Display Stream Compression

A-PHY Compliance Program

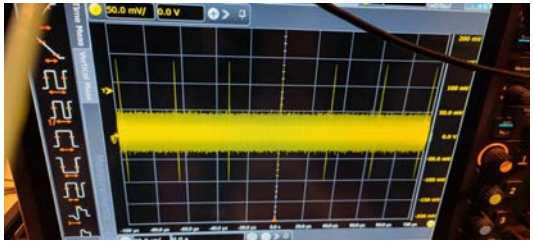
A-PHY Compliance Program

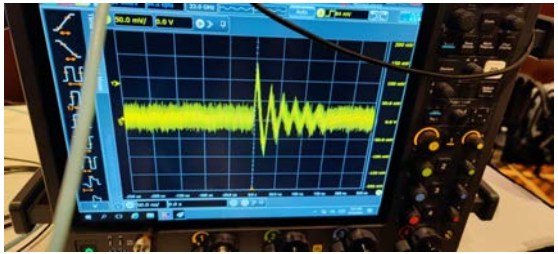
- MIPI Alliance is evaluating a compliance plan for A-PHY and MIPI Automotive SerDes Solutions (MASS℠) framework
  - Pilot activity **successfully completed phase I** and now in plan for next phase
  - Pilot program supervised by a test lab including two test vendors
  - All aspects of this activity will be reviewed for approval by MIPI Board of Directors
- All A-PHY tests are defined at box level (connector) and not at component level (i.e., chip)
- Currently, there is no impact on the membership requirements or any indication that this activity will increase product prices

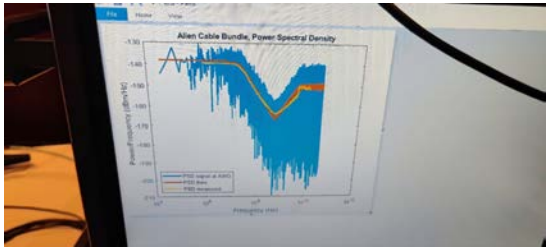
Compliance Process – WIP

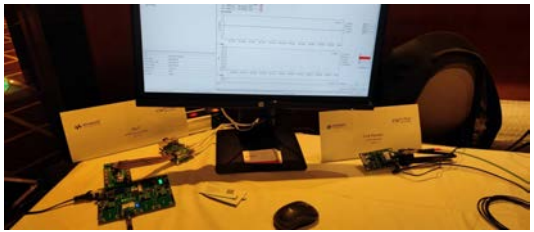


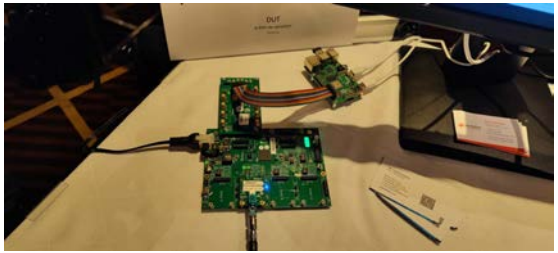
Test Demo Updates at Munich F2F

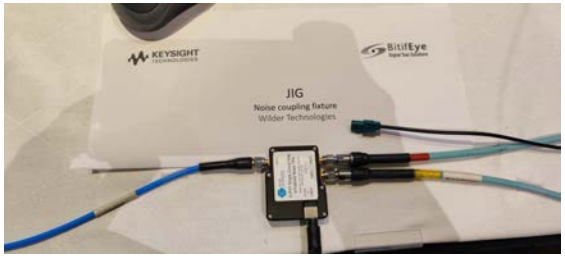


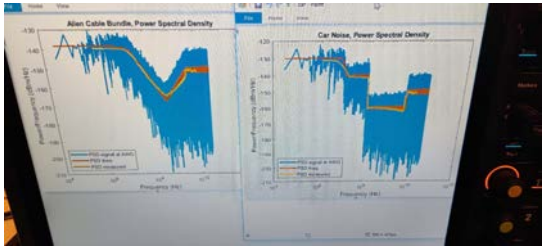












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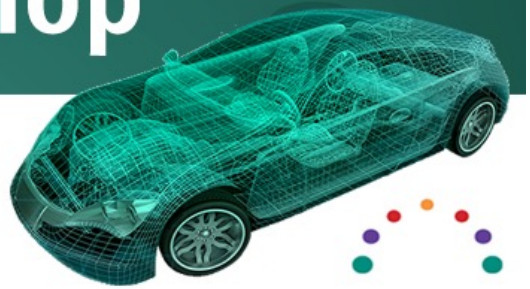

Q&A

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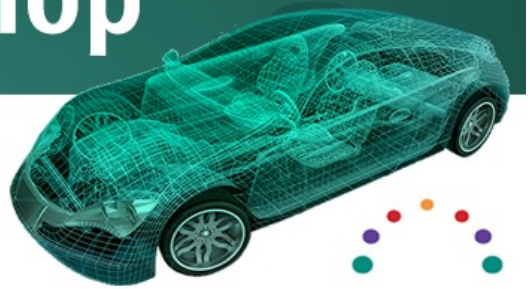

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to view recordings of any sessions you missed