MIPI Automotive Workshop

15 November 2022

Live Virtual Event
MIPI A-PHY®: Continuing to Drive Innovation for In-Vehicle Connectivity

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MIPI A-PHY® Working Group Co-Chairs
15 November 2022
Agenda

• A-PHY v1.0 / v1.1
• Power over A-PHY (PoA)
• A-PHY v2.0
• A-PHY in Zonal Architecture
• A-PHY for Modern Automotive Cockpit Display
• A-PHY Compliance Program
A-PHY v1.0 / v1.1
MIPI A-PHY – MASS Cornerstone

First industry-standard asymmetric SerDes physical layer specification targeted for ADAS/ADS and infotainment applications

About A-PHY
(v1.0 released in Sep 2020)

• Direct coupling to native MIPI CSI-2® / MIPI DSI-2℠/ VESA DisplayPort™ and eDP protocols
• High noise immunity, ultra low PER (< 10^{-19})
• Supports bridge-based and endpoint integration
• Support for automotive coax and SDP channels
• Power over cable
• Built-in functional safety according to ISO 26262
• Adopted by IEEE as IEEE 2977-2021

A-PHY v1.1 Enhancements
(released Dec 2021)

• Increased support for lower cost legacy cables
• Double uplink data rate
• Star quad cable support, enabling lower cost dual lane operation, for up to 32 Gbps data rate

PER: Packet Error Rate
What Makes MIPI A-PHY So Robust and Efficient?

**RTS + NBIC**

- **Time bounded local PHY-level retransmission**
  - Only within pre-defined “Overall Delay” (~6µs@G5)
  - Local: Transparent to the upper layers
  - Local: Happens within a single A-PHY hop

- **Dynamic modulation for retransmitted packets with better error resistance**

- **Highly resilient**
  - Overcomes large thousands symbols-long error bursts
  - Multiple 10s mV, instantly attacking NBI peaks

- **High reliability → PER < 10^{-19}**

- **Low overhead → 90% net data rate**

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**High throughput automotive links are EMI-limited — not AWGN limited**

NBI: Narrow Band Interferences  
NBIC: Narrow Band Interferences Canceller  
PMD: Physical Media Dependent  
PCS: Physical Coding Sub-Layer  
RTS: Re-Transmission Sub-Layer  
AWGN: Additive White Gaussian Noise
EMC Noises Part of Model as Per Spec
To Speed Up/Ensure JITC Convergence, JITC Re-training Is Used

Example: 4GBaud PAM4, 40mVpeak 3 Tone NBI, instant attack, without re-training
PAM2/4/8/16 Scatter Results A-PHY v1.0 / 1.1
Power over A-PHY – PoA

- A-PHY v1.0 / v1.1 include a section on PoA
- Separate specification is being developed to provide better flexibility and enhanced capabilities without impacting the A-PHY specification
  - This specification will be backward compatible with current definitions
- A-PHY v2.0 will be aligned with the new PoA specification
- The new PoA specification introduces new power types A-PHY link can support to enable power over cable to multiple types of devices and use cases

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### PoA System Type

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Type 1</th>
<th>Type 2</th>
<th>Type 3</th>
<th>Type 4</th>
<th>Type 5</th>
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<tbody>
<tr>
<td>VPSE&lt;sub&gt;max&lt;/sub&gt; (V)</td>
<td>12</td>
<td>12</td>
<td>24</td>
<td>24</td>
<td>48</td>
</tr>
<tr>
<td>VPSE&lt;sub&gt;OCmin&lt;/sub&gt; (V)</td>
<td>Unregulated</td>
<td>Regulated</td>
<td>Unregulated</td>
<td>Regulated</td>
<td>Unregulated</td>
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<tr>
<td>VPSE&lt;sub&gt;min&lt;/sub&gt; (V)</td>
<td>8</td>
<td>14.4</td>
<td>11.7</td>
<td>26</td>
<td>48</td>
</tr>
<tr>
<td>I&lt;sub&gt;in&lt;/sub&gt;max (mA)</td>
<td>293</td>
<td>500</td>
<td>600</td>
<td>500</td>
<td>500</td>
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<tr>
<td>PPSE&lt;sub&gt;min&lt;/sub&gt; (W)</td>
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<td>7.2</td>
<td>5.85</td>
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<td>24</td>
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<tr>
<td>VPD&lt;sub&gt;min&lt;/sub&gt; (V)</td>
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<td>9.7</td>
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<td>46</td>
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<tr>
<td>VPD&lt;sub&gt;max&lt;/sub&gt; (V)</td>
<td>18</td>
<td>18</td>
<td>36</td>
<td>36</td>
<td>60</td>
</tr>
<tr>
<td>PPD&lt;sub&gt;max&lt;/sub&gt; (W)</td>
<td>2</td>
<td>6.2</td>
<td>4.85</td>
<td>12</td>
<td>23</td>
</tr>
</tbody>
</table>

Additional Information:
- See Section 7.2.2
- See Section 7.2.4
- See Equation 5 for I<sub>Cont</sub> when VPSE < VPSE<sub>min</sub>.
- See Section 7.2.5
- See Equation 6 for PPSE when VPSE > VPSE<sub>min</sub>.
- See Section 8.3.3
- See Section 8.3.1
A-PHY v2.0 – Main Goals

• **Specification update focused on emerging architecture and use cases**
  – Zonal architecture and SDV (software-defined vehicle)
  – Modern automotive cockpit environments

• **Maintain backward compatibility to A-PHY v1.0 / v1.1**
  – A-PHY v1.0 / v1.1 will be forward compatible with next A-PHY specification

• **No changes in the upper layers**
  – Easy migration with minimal impact at system level

• **Maintain high EMC resilience and low packet error rate**
A-PHY Next Generation – Main New Features

- Double downlink throughput
  - Up to **32Gbps** (28.8Gbps net data rate) per single lane
- Uplink throughput increase
- Up to **1.6Gbps** (1.166Gbps net data rate)
- Enhance interface support
  - Add 1Gb Ethernet support (based on the new uplink BW)
  - Other interfaces may be added based on market demand
- Expand A-PHY secure control
  - Enable support of a secure A-PHY network
## Downlink Gear Table (A-PHY v1.1)

<table>
<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td>G1</td>
<td>NRZ-8B/10B</td>
<td>1</td>
<td>2</td>
<td>1.5</td>
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<tr>
<td></td>
<td>PAM4</td>
<td>0.5</td>
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<td>1.8</td>
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<td>NRZ-8B/10B</td>
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<td>4</td>
<td>3</td>
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<tr>
<td></td>
<td>PAM4</td>
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<td></td>
<td>3.6</td>
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<td>G3</td>
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<td>8</td>
<td>7.2</td>
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<tr>
<td></td>
<td>NRZ-8B/10B</td>
<td>4</td>
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<td>6</td>
</tr>
<tr>
<td>G4</td>
<td>PAM8</td>
<td>2</td>
<td>12</td>
<td>10.8</td>
</tr>
<tr>
<td>G5</td>
<td>PAM16</td>
<td>2</td>
<td>16</td>
<td>14.4</td>
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## Downlink Gear Table (A-PHY v2.0)

<table>
<thead>
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<th></th>
</tr>
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<tbody>
<tr>
<td>G1</td>
<td>NRZ-8B/10B</td>
<td>1</td>
<td>2</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td>PAM4</td>
<td>0.5</td>
<td>2</td>
<td>1.8</td>
</tr>
<tr>
<td>G2</td>
<td>NRZ-8B/10B</td>
<td>2</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>PAM4</td>
<td>1</td>
<td>4</td>
<td>3.6</td>
</tr>
<tr>
<td>G3</td>
<td>PAM4</td>
<td>2</td>
<td>8</td>
<td>7.2</td>
</tr>
<tr>
<td></td>
<td>NRZ-8B/10B</td>
<td>4</td>
<td>8</td>
<td>6</td>
</tr>
<tr>
<td>G4</td>
<td>PAM8</td>
<td>2</td>
<td>12</td>
<td>10.8</td>
</tr>
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<td>G5</td>
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<td>21.6</td>
</tr>
<tr>
<td>G7</td>
<td>PAM16</td>
<td>4</td>
<td>32</td>
<td>28.8</td>
</tr>
</tbody>
</table>
# Uplink Gear Table (Initial Proposal)

<table>
<thead>
<tr>
<th>Uplink Gear</th>
<th>Modulation</th>
<th>Modulation Bandwidth [MHz]</th>
<th>Data Rate [Mbps]</th>
<th>Max Net App Data Rate [Mbps]</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1</td>
<td>NRZ-8B/10B</td>
<td>50</td>
<td>100</td>
<td>53</td>
</tr>
<tr>
<td>U2</td>
<td>PAM4-8B/10B</td>
<td>50</td>
<td>200</td>
<td>125</td>
</tr>
<tr>
<td>U3</td>
<td>PAM4-8B/10B</td>
<td>400</td>
<td>1600</td>
<td>1166</td>
</tr>
</tbody>
</table>
A-PHY v1.x and v2.0 Channels

Proposed Link Segment (TLIS) For G6 & G7

- Single IL limit, reuse IEEE 802.3cy channel
- New channel IL @ 4GHz is only slightly higher than V1.x channel at 2GHz
- To maintain TX PSD upper limit of -92dBm/Hz, G6/7, which operate at 8GBaud, will use TX Amp which is 3dB larger than in G4/5 @ 4GBaud
Optional G4/G5 with PAM4 @ 8GBaud

Optional G4/5 Using PAM4 @ 8GBaud over v1.x Channels

To maintain TX PSD upper limit, PAM4 @ 8GBaud, must still use the same TX Amp of PAM8/16 @ 4GBaud since PAM4's PAM2 levels are 2.7dB Larger than PAM8/16's levels... [level ‘15’ vs ‘11’], however PAM4 provides 14dB larger separation between TX Levels compare to PAM16 [see clarifications in the next slide]

Full v1.x Channel Response [ENIS + TLIS + ENIS]
A-PHY v2.0 Channel Model

- Lab measured S-parameters

```plaintext
S_Param
SP1
Start=200 kHz
Stop=20 GHz
Step=200 kHz

SPOutput
SPoUtput
spOutput1
FileName="a-phy_TLIS_channel_2_0"
FileType=touchstone
Format=MA
```

File="C:\backup\ADS\2019\A-PHY\A-PHY_wrk\data\Channel_A_PHY2_0_Coaxial12_ZNB_462_10m_3_3_3_1.s2p"
A-PHY in Zonal Architecture
Zonal Architecture

• Drivers
  – Reducing wiring harness complexity and weight
  – Centralized and scalable compute unit
  – Reduced number of ECU and simpler hardware abstraction
  – Simplified OTA updates and upgrades for Software Defined Vehicle (SDV)
  – Software compatibility and Interface flexibility

• Guidelines
  – Aggregation of nodes in spatial proximity by Zone ECUs
  – Central vehicle computer (VC)
  – High-rate backbone
  – Shared infrastructure across functional domains

• Challenges
  – Heterogeneous technologies
  – Interoperability
  – Topology depth
  – Bandwidth
  – Latency
  – Efficiency

OTA – Over The Air

High Speed (>1Gbps)
Low Speed (<1Gbps)
Zonal Architecture – High-Level Structure

- Strong demand for reductions of harness complexity and weight
- Data aggregation in zone with no change of data format(s) desired
- Hybrid connectivity – direct or via zone
- **Data processing centralized**
  - Improved perception performance
  - Easier update and SW maintenance
  - Improved flexibility/scalability
Architecture Optimization

- **Future looking** - Majority of high-speed links in the vehicle connect asymmetric edge devices
- **Flexible** - Central VC should be able to connect natively, both to aggregators or directly to edge devices
- **Optimized** - Standardized communication technology (PHY and protocol) should be integrated into the high-speed edge devices
- **Backward compatible** - legacy interface gateways and low-bandwidth located in the spatial area of the zonal aggregators, may use a 100Mbps/1Gbps Ethernet backbone.

**A-PHY is the perfect fit Zonal Architecture optimization**
- Resilient asymmetric high-speed link (up to 32Gbps per lane) with clear forward roadmap
- Only PHY natively integrated to edge devices and aggregators (e.g., MIPI CSI-2)
- Multiplex both the high-speed asymmetric communication and the 1Gbps Ethernet backbone over the same cable.
A-PHY for Modern Automotive Cockpit Displays
## Modern Automotive Cockpit Displays

<table>
<thead>
<tr>
<th>Display Type</th>
<th>Example Size (Inches)</th>
<th>Example Resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Left and Right-Side Mirror Displays</td>
<td>7”</td>
<td>1280x800</td>
</tr>
<tr>
<td>Driver Instrument Display</td>
<td>12.3”</td>
<td>3840x1440</td>
</tr>
<tr>
<td>Center Information Display</td>
<td>12.3”</td>
<td>3840x2160</td>
</tr>
<tr>
<td>Extended Co-Driver display</td>
<td>12.3”</td>
<td>3840x2160</td>
</tr>
<tr>
<td>Lower Control Display</td>
<td>12.4”</td>
<td>3840x2160</td>
</tr>
</tbody>
</table>

![Automotive Cockpit Displays](image.png)
Modern Automotive Cockpit Displays

- Multiple connectivity schemes including daisy chain
- Up to **64Gbps** non-compressed data in single port
  - Up to **192Gbps with VESA DSC compression** with no additional overhead in single port
- Flexible uplink up to 1.6Gbps
  - Enable internal DMS² camera
- Ultra low PER¹ for the entire vehicle lifespan (zero errors)
- End-to-end functional safety
- End-to-end advanced layered security
- Multiple protocol support (e.g., MIPI DSI®, VESA DisplayPort)

¹PER – Packet Error Rate
²DMS – Driver Monitoring System
Daisy Chain – General Structure Example

Infotainment ECU

BRIDGE 1

DISPLAY 1

LINK 1

BRIDGE 2

DISPLAY 2

LINK 2

BRIDGE 3

DISPLAY 3

LINK 3

BRIDGE 4

DISPLAY 4

LINK 4
**Daisy Chain Example**

<table>
<thead>
<tr>
<th>Config</th>
<th>Display 1 (LCD)</th>
<th>Display 2 (CID)</th>
<th>Display 3 (CDD)</th>
<th>Total BW Gbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3840x2160</td>
<td>3840x2160</td>
<td>3840x2160</td>
<td>37.6</td>
</tr>
<tr>
<td>2</td>
<td>3840x2160</td>
<td>5120x2160</td>
<td>5120x2160</td>
<td>45.8</td>
</tr>
<tr>
<td>3</td>
<td>7680x2800</td>
<td>7680x2800</td>
<td>7680x2800</td>
<td>96.5</td>
</tr>
</tbody>
</table>

**Assumptions:**
- Uncompressed 24-bit/pixel or DSC 8bpp, 60fps, CVT-2 Blanking overhead
- DSC: VESA Display Stream Compression

**Gear Single Lane BW (Gbps) | Dual Lane BW (Gbps)**

<table>
<thead>
<tr>
<th>Gear</th>
<th>Single Lane BW (Gbps)</th>
<th>Dual Lane BW (Gbps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>G1</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>G2</td>
<td>4</td>
<td>8</td>
</tr>
<tr>
<td>G3</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>G4</td>
<td>12</td>
<td>24</td>
</tr>
<tr>
<td>G5</td>
<td>16</td>
<td>32</td>
</tr>
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<td>G6</td>
<td>24</td>
<td>48</td>
</tr>
<tr>
<td>G7</td>
<td>32</td>
<td>64</td>
</tr>
</tbody>
</table>

**Notes:**
- Link 1
  - DL-G6
  - DL-G7
  - DL-G6
  - DL-G6
- Link 2
  - G7
  - G5
  - G6
- Link 3
  - G5
  - G3
  - G6
  - G4
A-PHY Compliance Program
A-PHY Compliance Program

• MIPI Alliance is evaluating a compliance plan for A-PHY and MIPI Automotive SerDes Solutions (MASS\textsuperscript{SM}) framework
  – Pilot activity \textit{successfully completed phase I} and now in plan for next phase
  – Pilot program supervised by a test lab including two test vendors
  – All aspects of this activity will be reviewed for approval by MIPI Board of Directors
• All A-PHY tests are defined at box level (connector) and not at component level (i.e., chip)
• Currently, there is no impact on the membership requirements or any indication that this activity will increase product prices
Compliance Process – WIP


MIPI Approval Process for MOIs → MIPI Test Setup Workshop (P2T) + approval → MOI Correlation

MIPI Approval Process for Test Labs → MIPI Interop Plug Fest (P2P) → Interop Test Reports (vendors NDA)

DUTs → Compliance Test Reports

Ownership Legend:
- MIPI
- Test equipment Vendors
- Test Labs
- Product Vendors
Test Demo Updates at Munich F2F
Q&A
THANK YOU

Check back at http://www.mipi.org/2022-automotive-workshop to view recordings of any sessions you missed