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**MIPI VGISM for Sideband GPIO and Messaging
Consolidation on Mobile System**

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MIPI ALLIANCE
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CONFERENCE

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MIPI.ORG/DEVCON

Agenda

- The Problem Statement
- Virtual GPIO Interface (MIPI VGISM) : Concept
- MIPI VGISM Architecture
- Application Scenarios
- Summary
- Q&A

Mobile Connectivity Expansion Trends

Cellular

- 2G/3G/4G → LTE-Advanced → 5G

WiFi

- 802.11a/b/g/n/ac → ax
802.11ad/WiGig

Video

- VGA/SD/HD → 4K → 8K

Docking

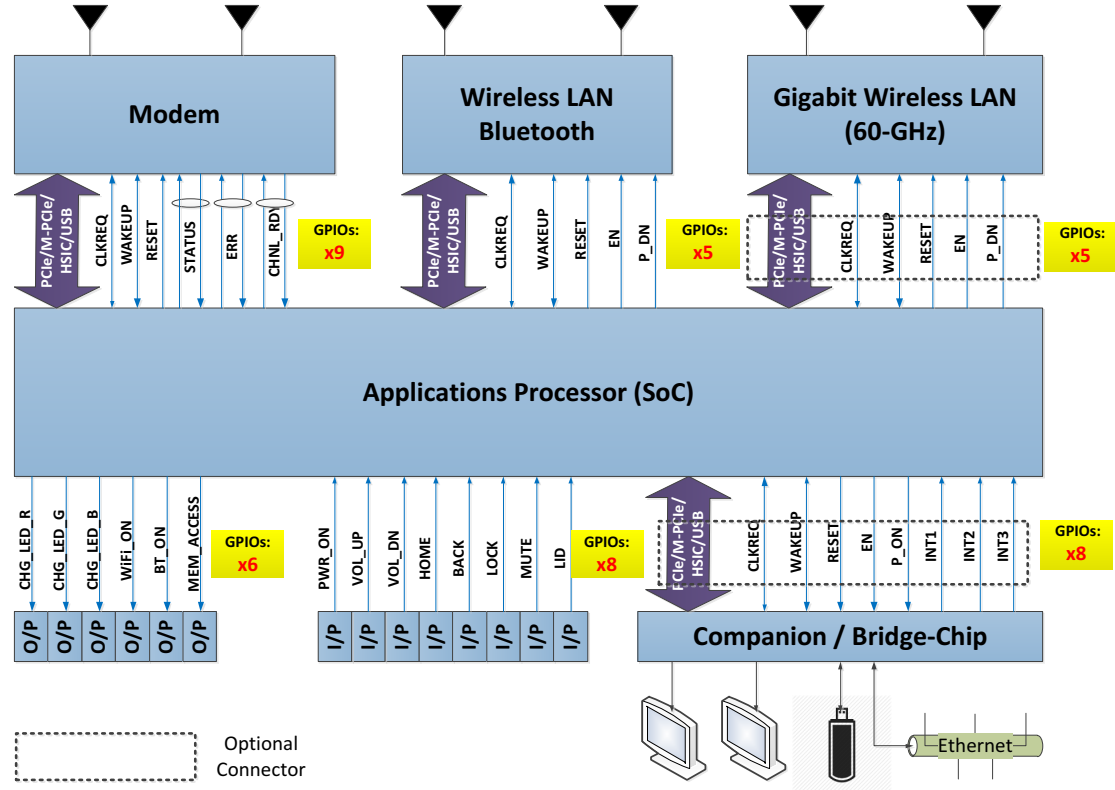
- Charging/audio/video →
Productivity, Games and External
Storage

Mobile Influenced

- Drones, IoT, Automotive,
- CAT-1 to CAT-3 Low-Power LTE
Modem Support



The Problem of Sideband Proliferation

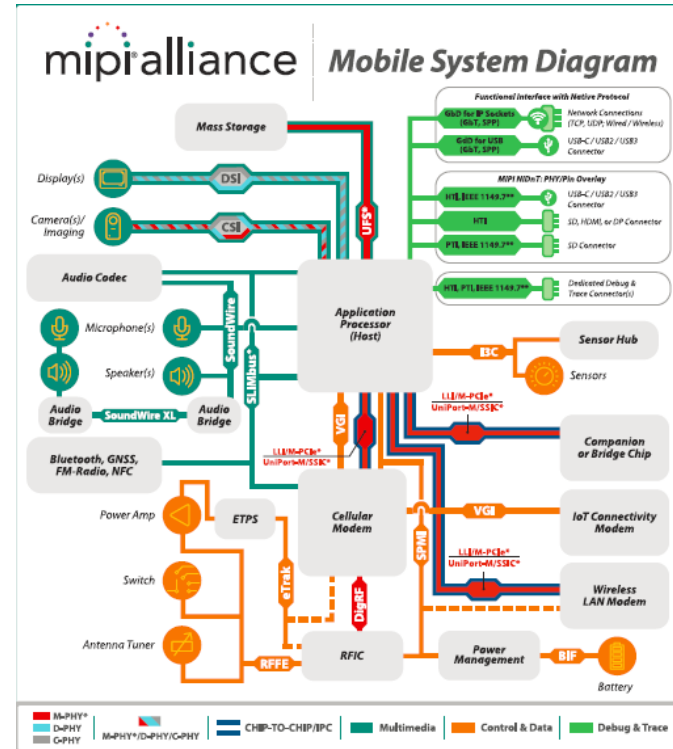


The Problem of Sideband Proliferation

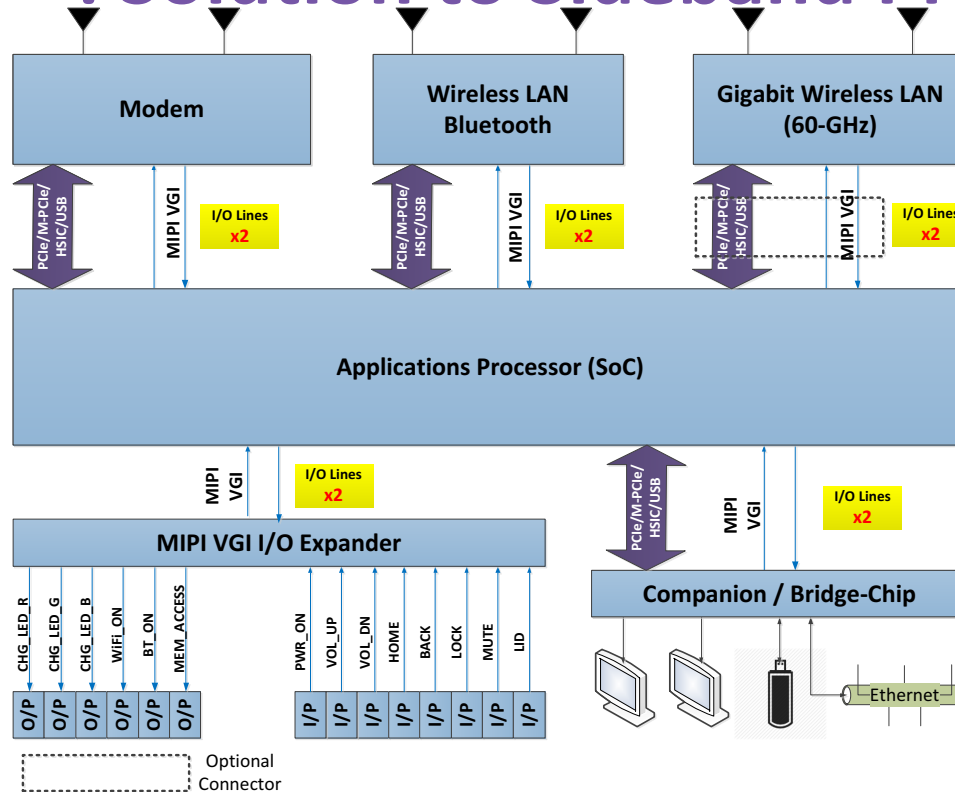
Typical Sideband Utilization

Domain	Number of Sideband I/O
Camera/Imaging	6 to 12
Audio CODEC	4 to 7
Cellular Modem	3 to 10
Wireless LAN Modem	3 to 10
Bridge Chip	3 to 8
Sensor Hub	4 to 18

Typical Sideband GPIOs: 23 to 65

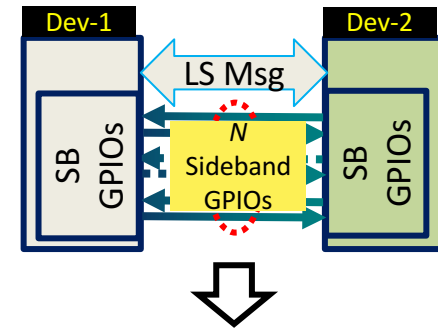


MIPI VGISM: Solution to Sideband Proliferation

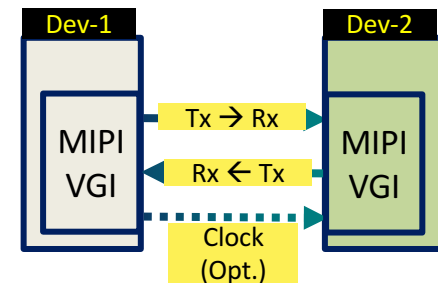


MIPI VGISM: The Concept

- **MIPI VGI** consolidates **N**-sideband GPIOs and sub-100 MHz serial messaging over **2** or **3** wire interface in a Point-to-Point configuration
- **2-wire MIPI VGI** : Asynchronous, Full-Duplex (4-Mbps max.)
- **3-wire MIPI VGI** : Synchronous, Full-Duplex
- **MIPI VGI Rev-1 (3-wire) Max Speed:** 76.8 MHz

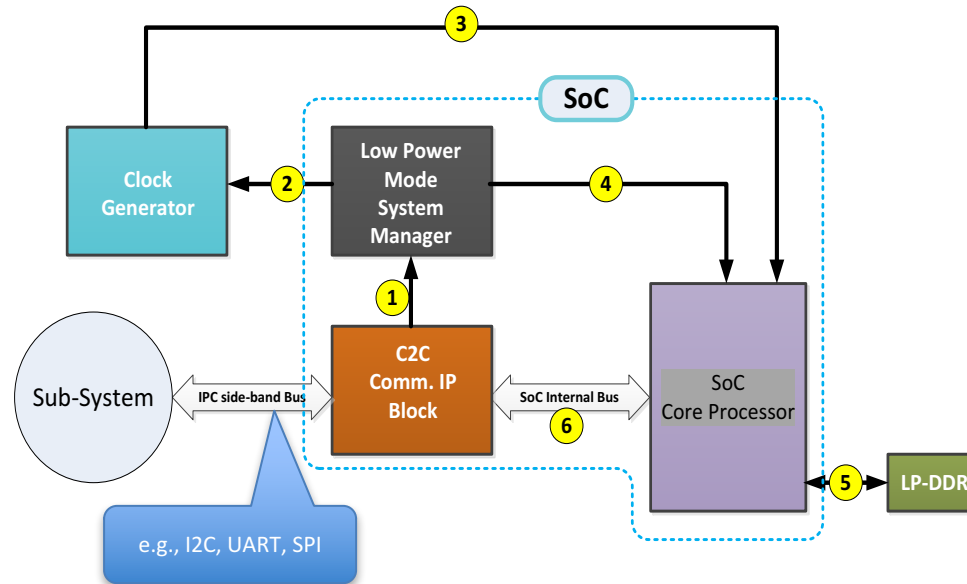


Virtual GPIO Interface(MIPI **VGI**)



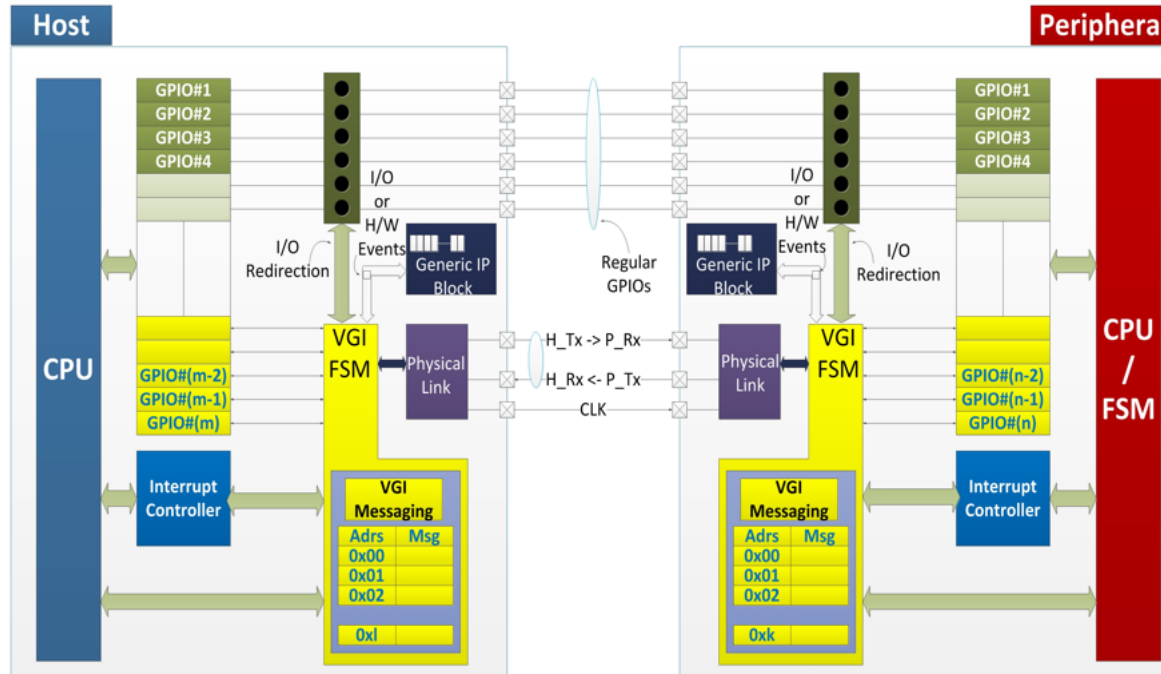
- ✓ Consolidates Low Speed Messaging Interface and Sideband GPIOs (**N-pins to 2/3-pins reduction**)

Limitation of Conventional Techniques

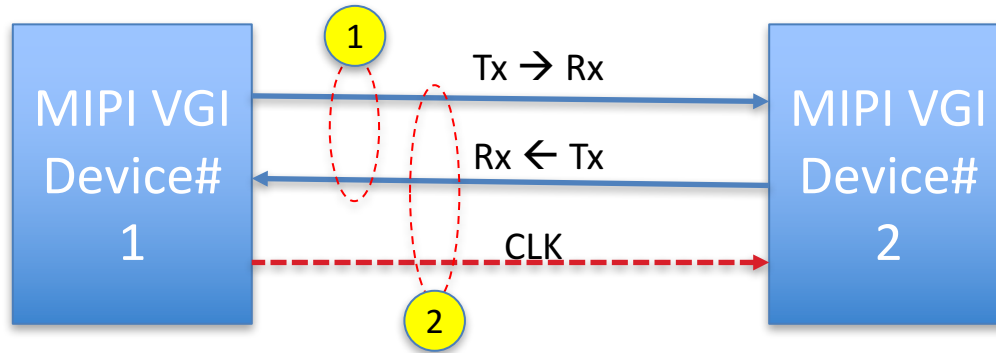


- ✓ HLOS processing latency varies widely
- ✓ Deep-sleep to active-state typical latency : Typically → 30 to 100-mS
- ✓ Timing uncertainty not suitable for the key IPC side-band signaling

MIPI VGISM Architectural Block-Diagram

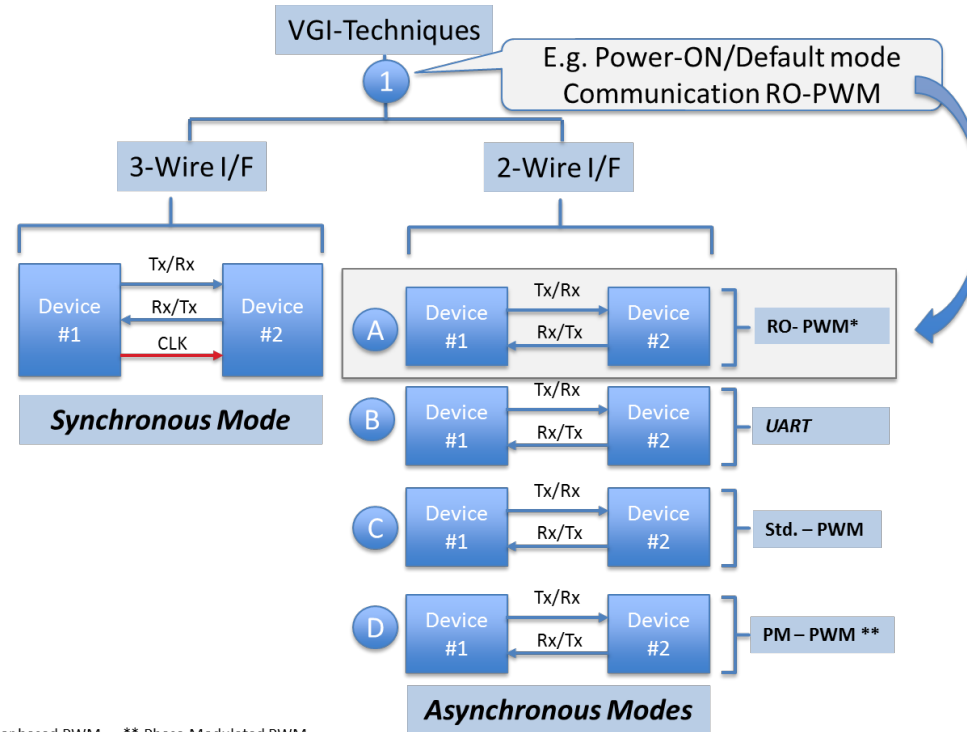


MIPI VGISM Physical Interface: 2-wire or 3-wire



- 1 Asynchronous MIPI VGI
 - ▣ Initial and Power State Transition mode communication over 2-wire, 4-Mbps max.
- 2 Synchronous MIPI VGI
 - ▣ Common clock (Up to 76.8 MHz in VGI Rev-1)
 - ▣ Sleep clock based operation supported in Low Power Modes

MIPI VGISM Techniques At-a-Glance

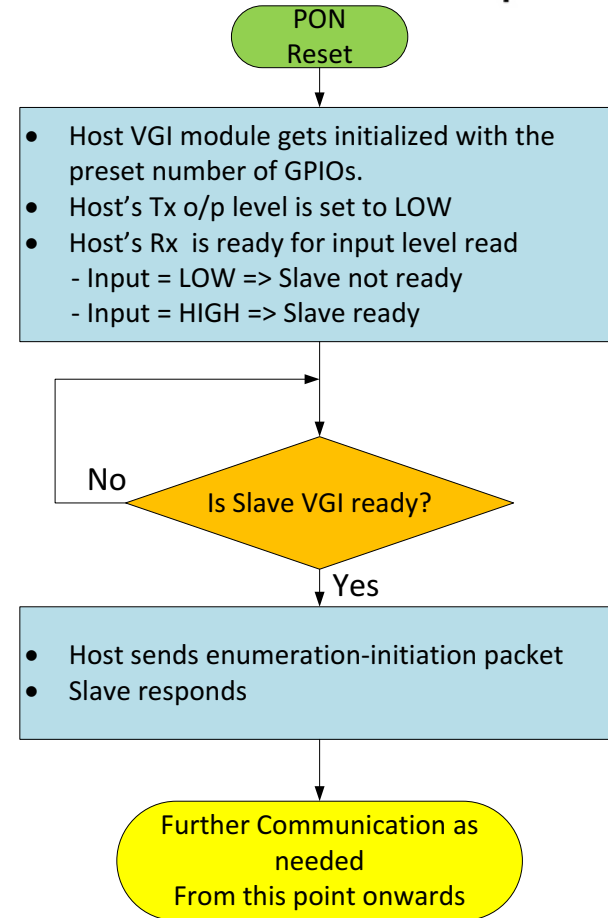


* Ring-Oscillator based PWM, ** Phase-Modulated PWM

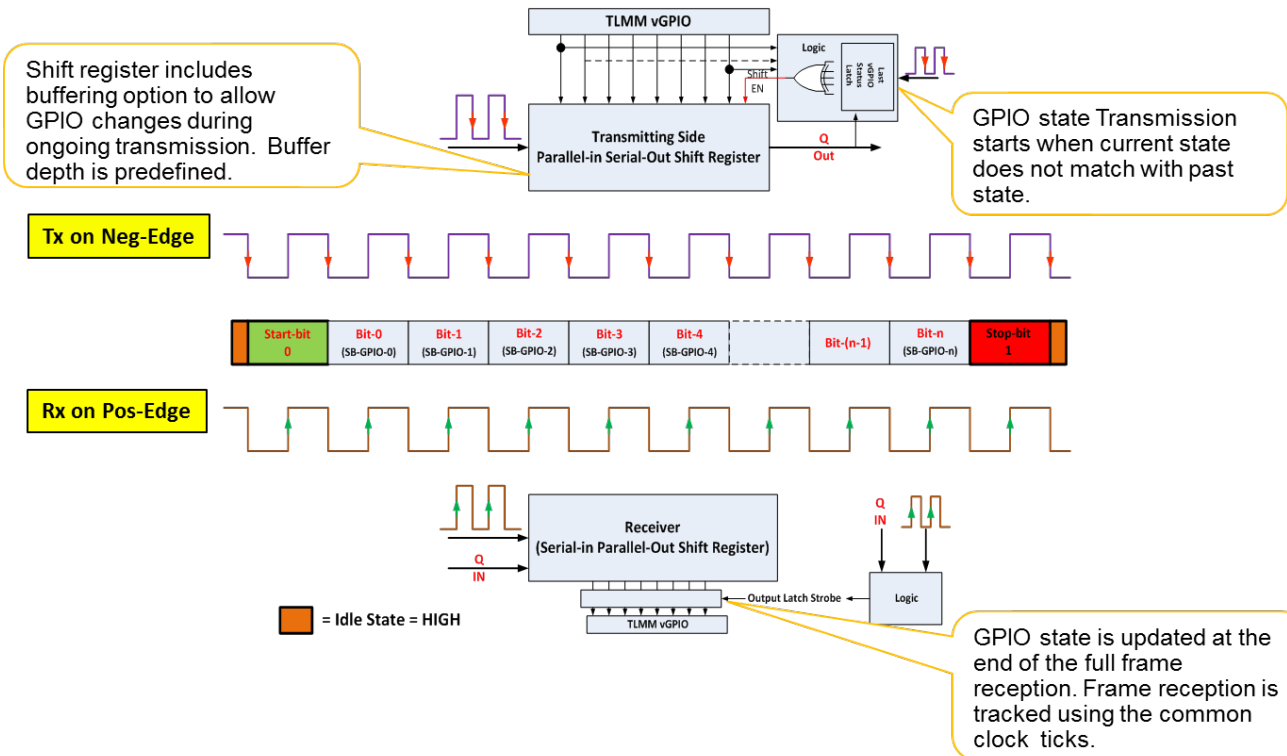
MIPI VGISM Roadmap

#	VGI Features	VGI v1.0	VGI Next
1	2-wire and 3-wire I/F support	✓	✓
2	Default PWM encoding	✓	✓
3	UART Encoding	✓	✓
4	PM-PWM Encoding (Phase-Modulated PWM)	-	✓
5	2-wire mode max throughput	4 Mbps	8 Mbps (PM-PWM)
6	3-wire mode max throughput	76.8 Mbps	153.6 Mbps
7	1.2V, 1.8V Operation support	✓	✓
8	1-wire mode support	-	✓

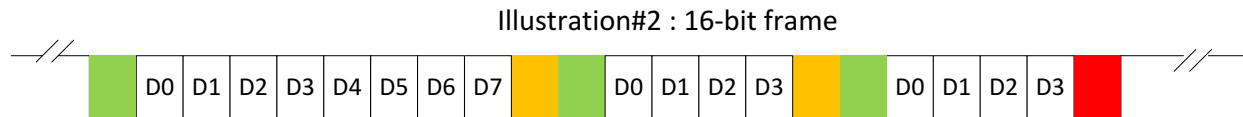
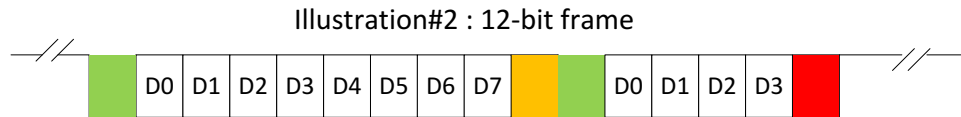
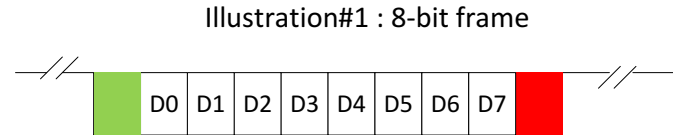
MIPI VGISM Init Sequence



Synchronous 3-Wire MIPI VGISM

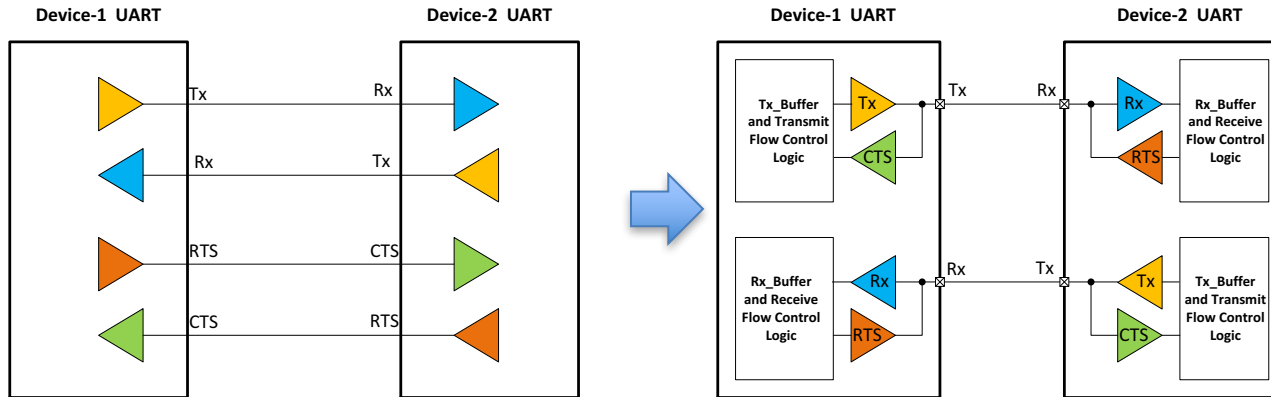


Asynchronous 2-wire MIPI VGISM: UART Mode

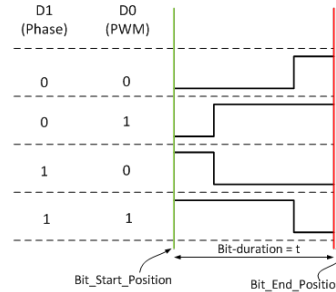


Asynchronous 2-wire MIPI VGISM: UART Mode

H/W Flow Control over Tx/Rx eliminates RTS/CTS physical pins



Asynchronous MIPI VGISM: Phase-Modulated PWM

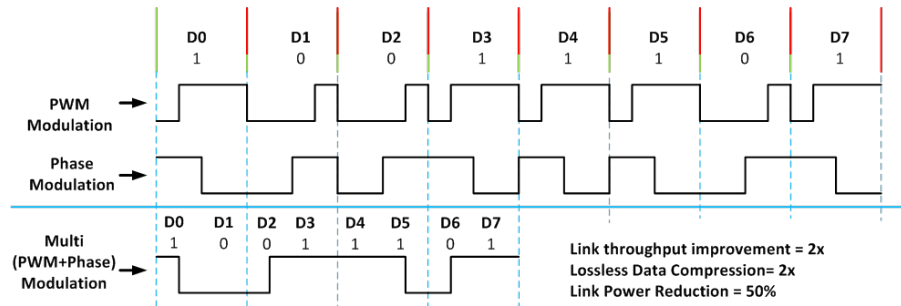


Highlights:

- All Digital Solution
- 2x Throughput
- Time-domain data compression
- Link power Reduction by 50%

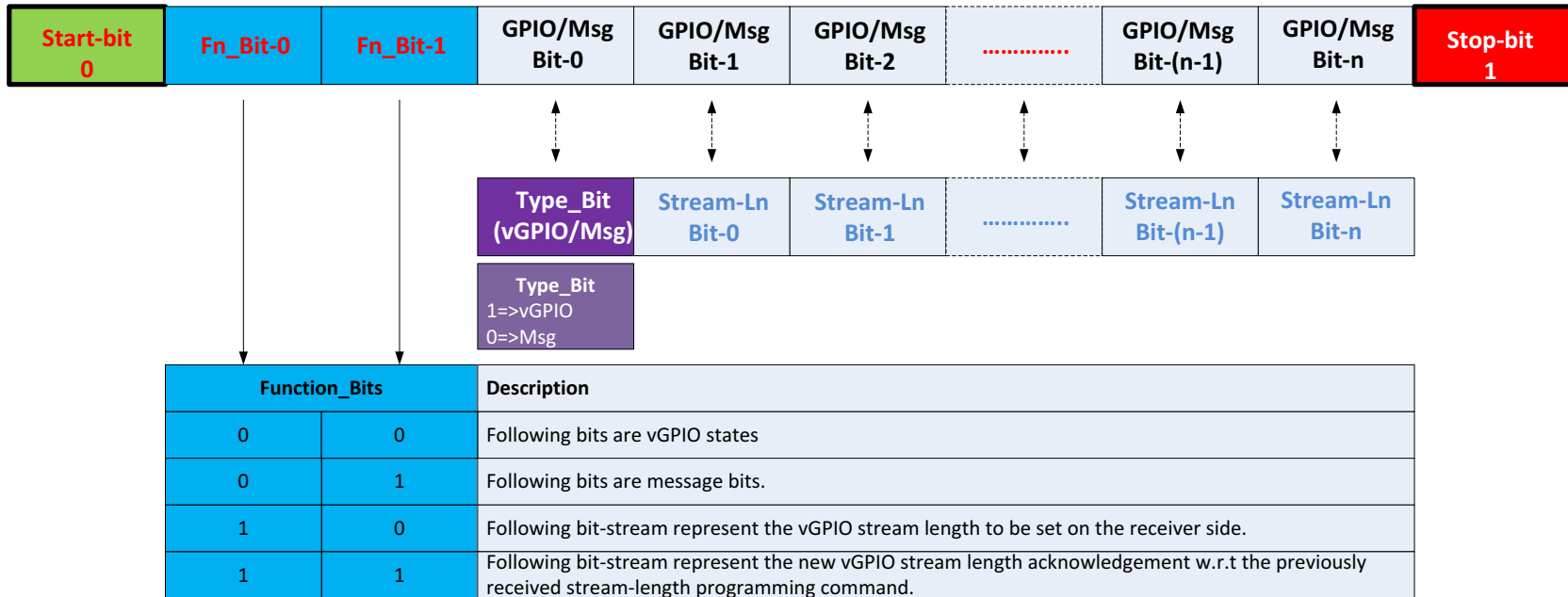
[Symbol to signal mapping for a joint \(PWM+Phase\) modulation scheme](#)

Example Representation of an arbitrary data-sequence "10011101"



[Link throughput and power :: A comparative look](#)

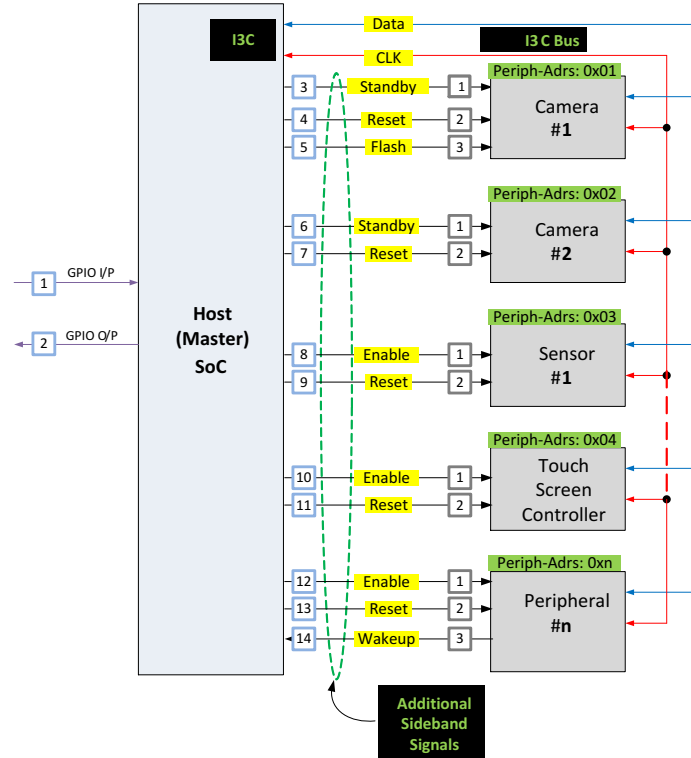
MIPI VGISM Protocol



NOTE: The mechanism has a fixed overhead of two-bits over the base-line vGPIO implementation.

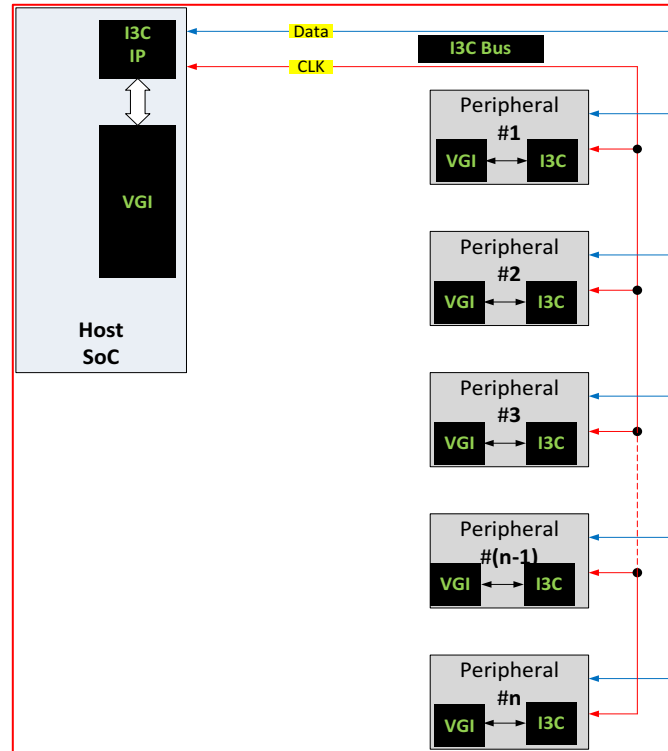
MIPI VGISM FSM Integration with MIPI I3CSM

- VGI FSM could be integrated with a serial interface of choice, such as MIPI I3CSM
- I3CSM supports MIPI VGI integration through dedicated Common Command codes (CCC) support in I3CSM v1.0
- Helps reduce Hardware event pins at system level



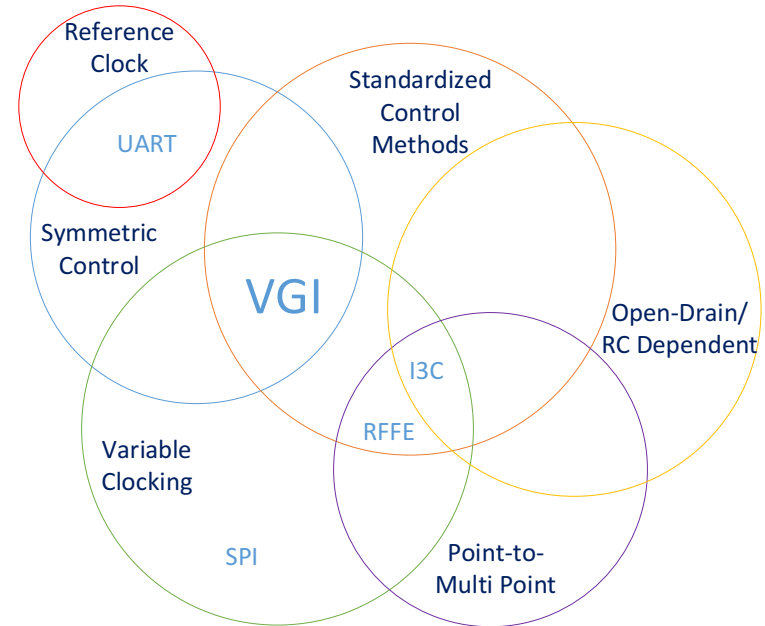
MIPI VGISM FSM Integration with MIPI I3CSM

- HW Event sideband signals are eliminated
- VGI-FSM (Finite State Machine) performs I3CSM message encoding/decoding for HW events and thus frees up the associated CPU on the host-SoC for these tasks.
- Impact is reduced Latency and Power consumption.



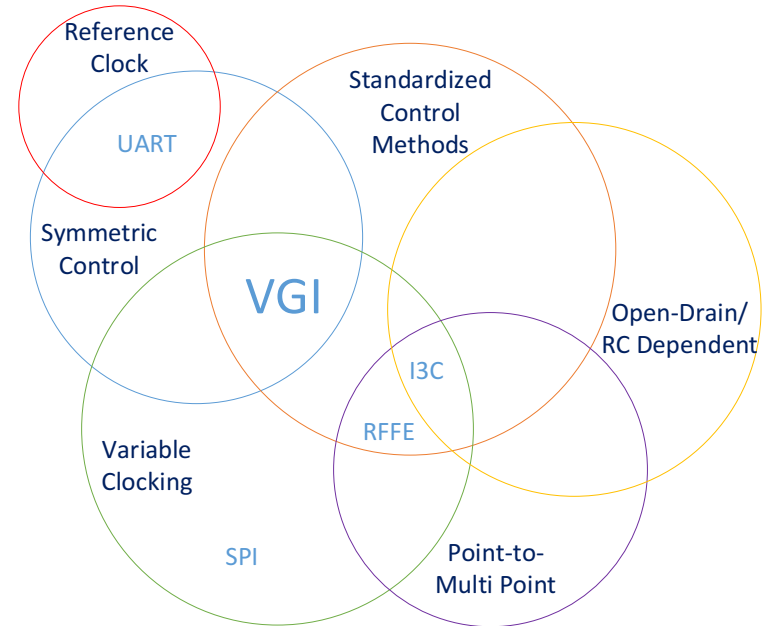
Comparing MIPI VGISM

- **SPI**
 - Master-Slave approach
 - Custom implementations, no common methods
- **MIPI I3CSM**
 - Multi-Master Multi-Slave, Open-Drain approach
 - In-band interrupts
- **MIPI RFFESM**
 - Master-Multi Multi-Slave approach
- **UART**
 - Custom implementations, requires reference clocks
- **MIPI VGISM**
 - Symmetric control approach (No Master No Slave)
 - Initialization from either side

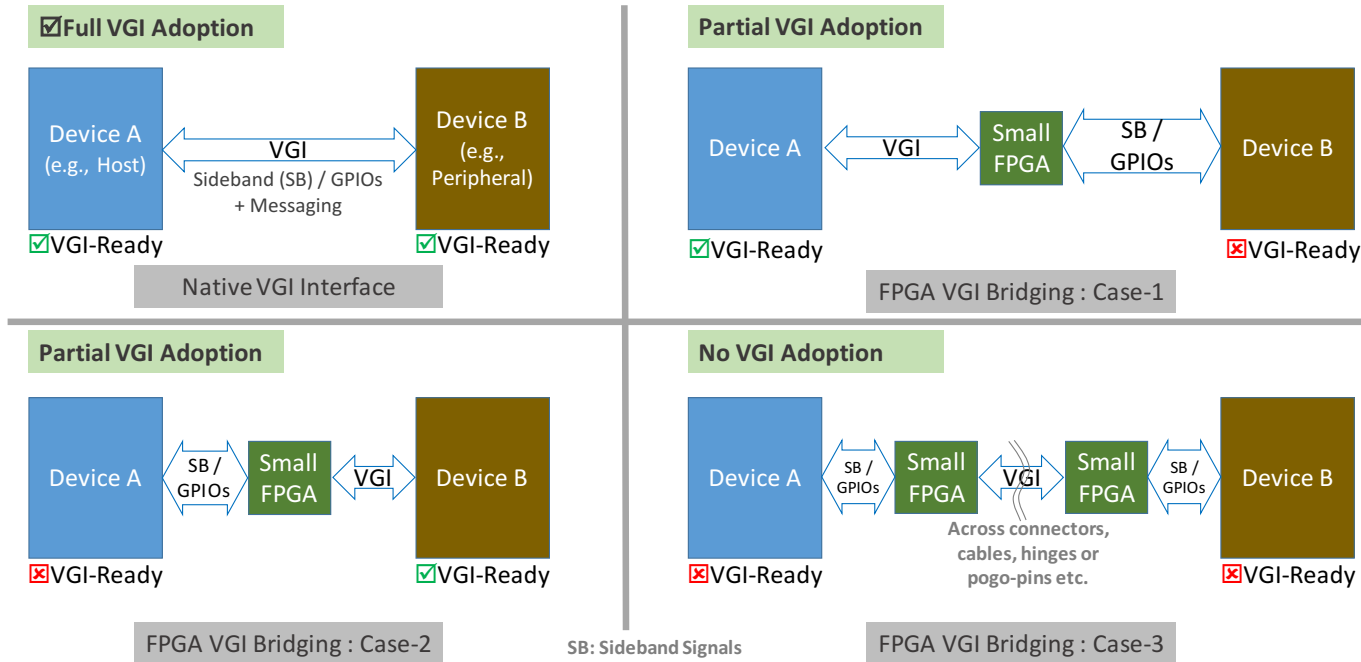


Comparing MIPI VGISM - Clocking

- **UART**
 - Requires Reference Clock with Agreed rates
- **SPI, MIPI I3C^(SM), MIPI RFFE^(SM)**
 - Clock is forwarded from Master to Slave
- **MIPI VGI^(SM)**
 - Using RO-PWM PHY option, the clocking is forwarded with data
 - Only Transmitter requires clock to create telegrams
 - Receiver captures telegrams without internal clock
 - Useful for devices which power down
 - Useful for very simple write-only devices (LED bank)



Phased MIPI VGISM Adoption – Leveraging Smaller FPGAs



Summary

- ❑ Sideband GPIOs add to SoC and PCB level cost and complexity
- ❑ MIPI VGI consolidates sideband GPIOs and Low-Speed serial messaging interface in P2P configuration to reduce I/O pins
- ❑ Both 2 and 3-wire interface options are available
- ❑ Common PWM start-up mode ensures interoperability
- ❑ The VGI FSM can be combined with any other interface bus of choice, e.g. I3C^(SM) VGI
- ❑ The MIPI VGI Specification is to be released in 2018



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