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MIPI-SPMI℠ 1.0 Multi-master Verification

2017
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BANGALORE, INDIA
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Agenda

- MIPI-SPMI – An Introduction
- MIPI-SPMI Multi-master Verification Architecture
- Verification Challenges and their Solutions
- Conclusions and References

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MIPI-SPMI – An Introduction

- SPMI (System Power Management Interface):
  - 2-wire serial interface
  - Supports up-to 4 masters and 16 slaves
  - Connects the integrated Power Controller (PC) of a System-on-Chip (SoC) processor system with one or more Power Management Integrated Circuits (PMIC) voltage regulation systems
- Within PC, SPMI-related functions are referred to as “Master”.
- Within PMIC, SPMI related functions are referred to as “Slave”.

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MIPI-SPMI – An Introduction

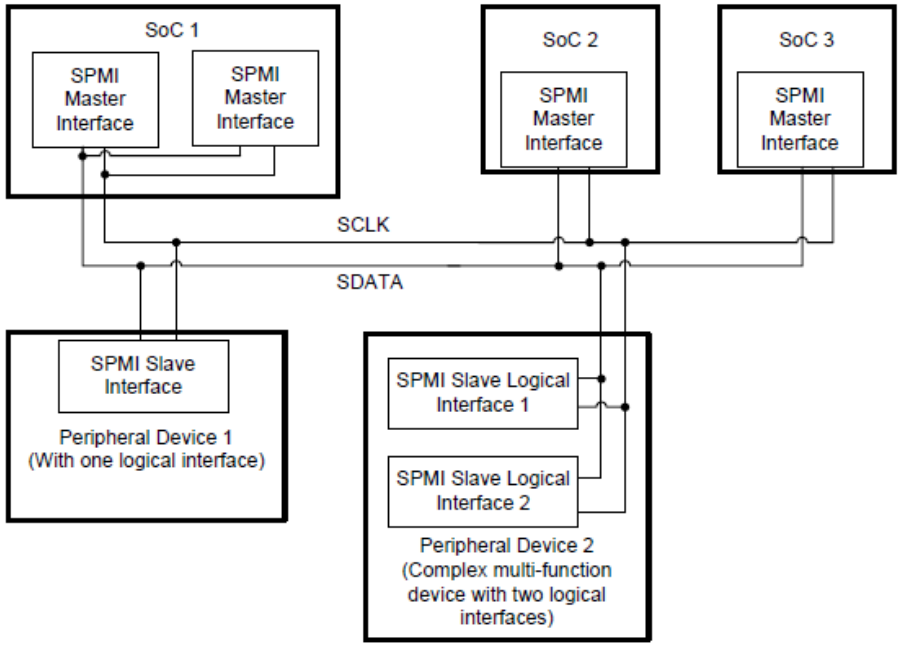

Figure 1 SPMI System Example

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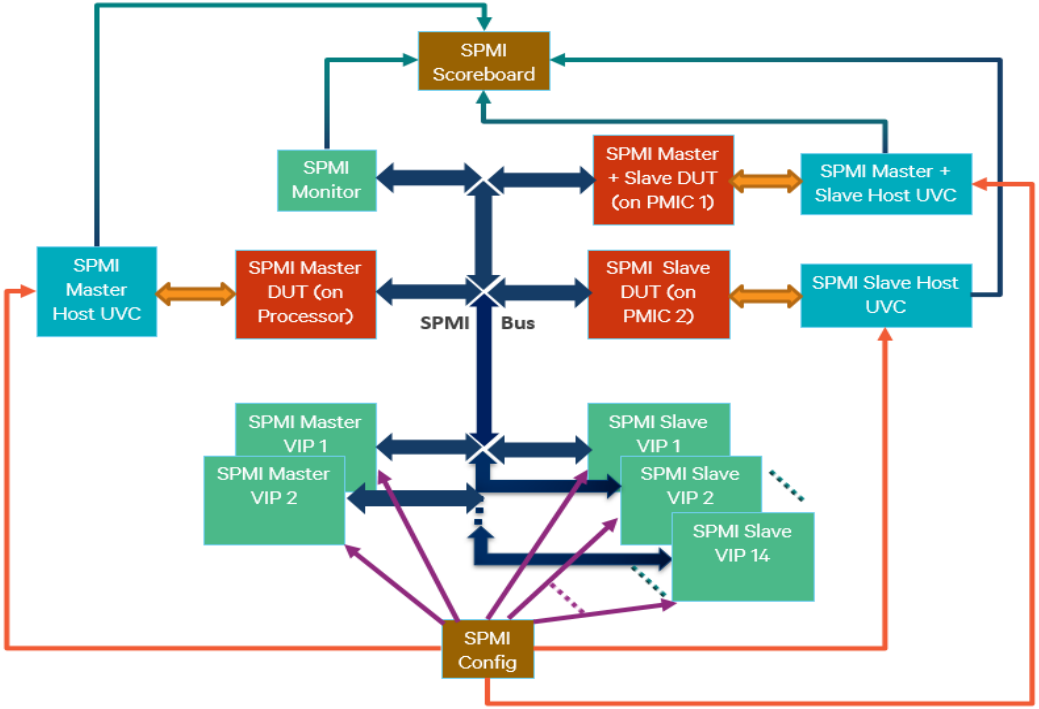
MIPI-SPMI Multi-master Verification Architecture



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Verification Challenges and their Solutions

- Multiple masters waking up at the same time and trying to connect
  - No RCS request
  - Pending RCS request
- Second master trying to connect when one master is already present
  - SSC Detection
  - Bus Idle
  - Bus Arbitration
- Multiple masters and slaves arbitrating with different priority levels
  - A-bit and SR-bit for slaves; priority and secondary MPLs for masters

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Verification Challenges and their Solutions

- BOM (Bus Owner Master) transfer, i.e. SCLK Handover
- Disconnection of a master
  - Using TBO command
  - During command parity error
- Noise during
  - Bus Idle
  - Master Arbitration
  - Slave Arbitration

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Multiple masters waking up at the same time and trying to connect

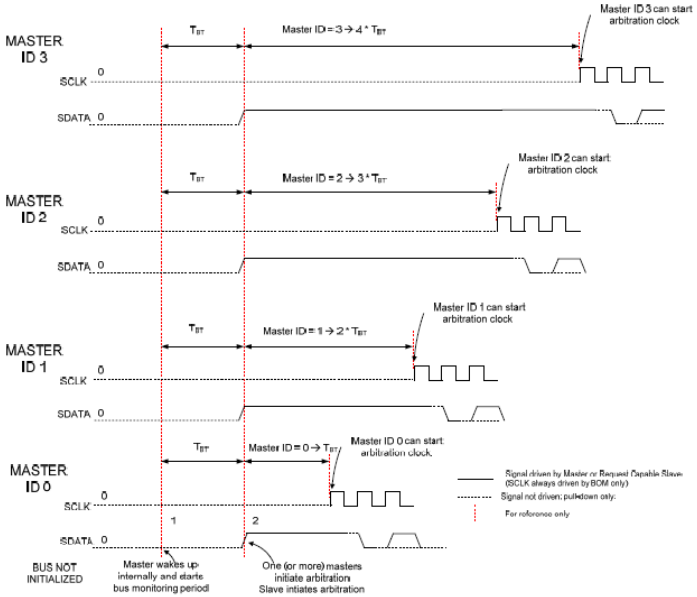

Figure 33 Bus Initialization

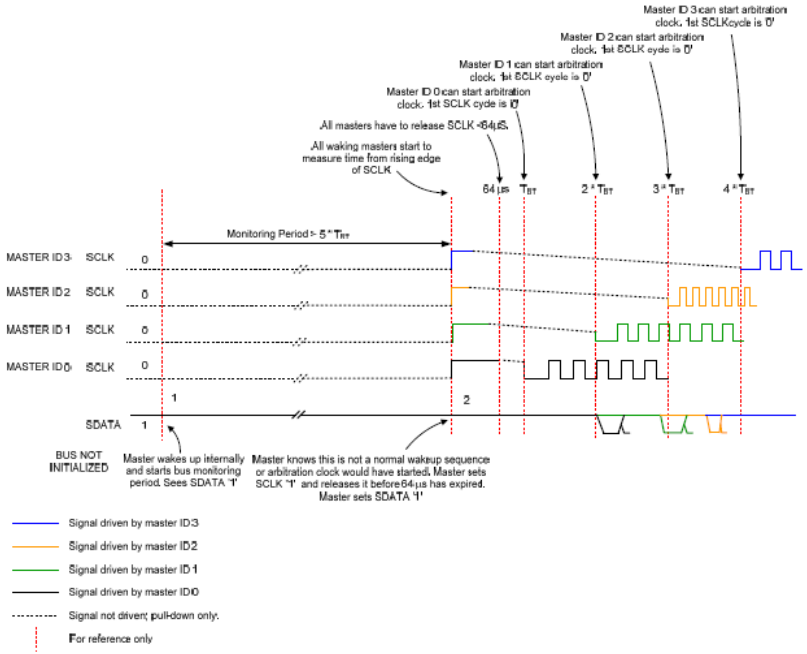

Figure 34 Bus Initialization with Pending Bus Arbitration Request by RCS

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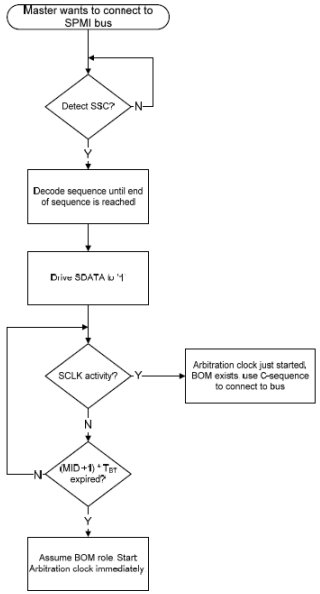
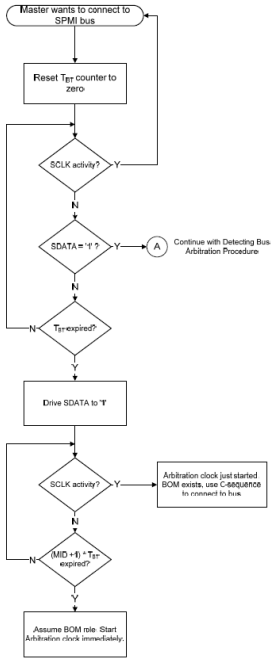
Second master trying to connect when one master is already present



Note: This procedure runs simultaneously with the Detecting Bus Idle procedure

Figure 30 Detecting SSC to Connect to Bus Flow Diagram



Note: This procedure runs simultaneously with the Detecting SSC procedure

Figure 31 Detecting Bus Idle to Connect to Bus Flow Diagram

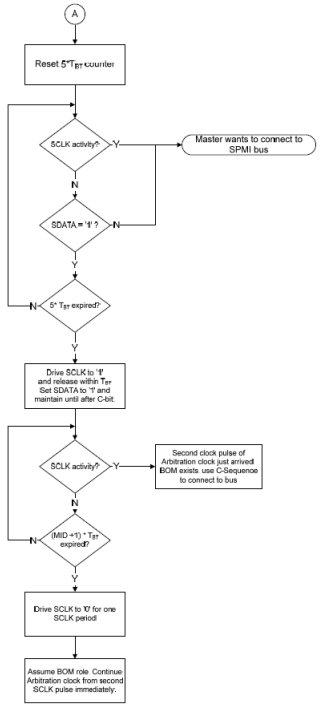


Figure 32 Detecting Bus Arbitration to Connect to Bus Flow Diagram

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Multiple masters and slaves arbitrating with different priority levels and BOM (Bus Owner Master) transfer

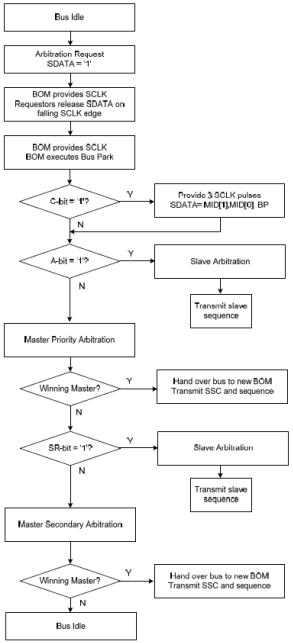

Figure 18 Bus Arbitration Flow Diagram

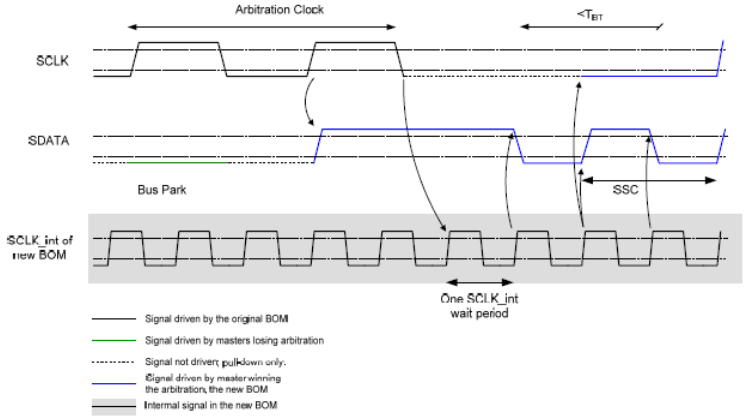

Figure 25 SCLK Handover Sequence

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Disconnection of a master

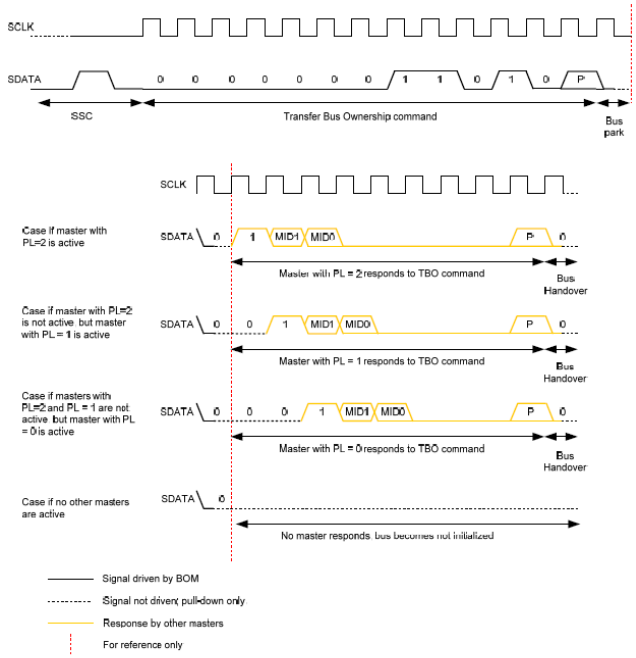
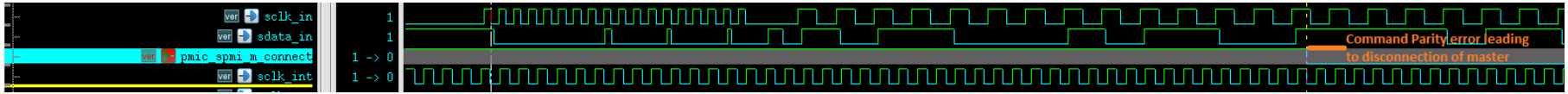


Figure 46 Transfer Bus Ownership Command Sequence



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Noise on SDATA bus

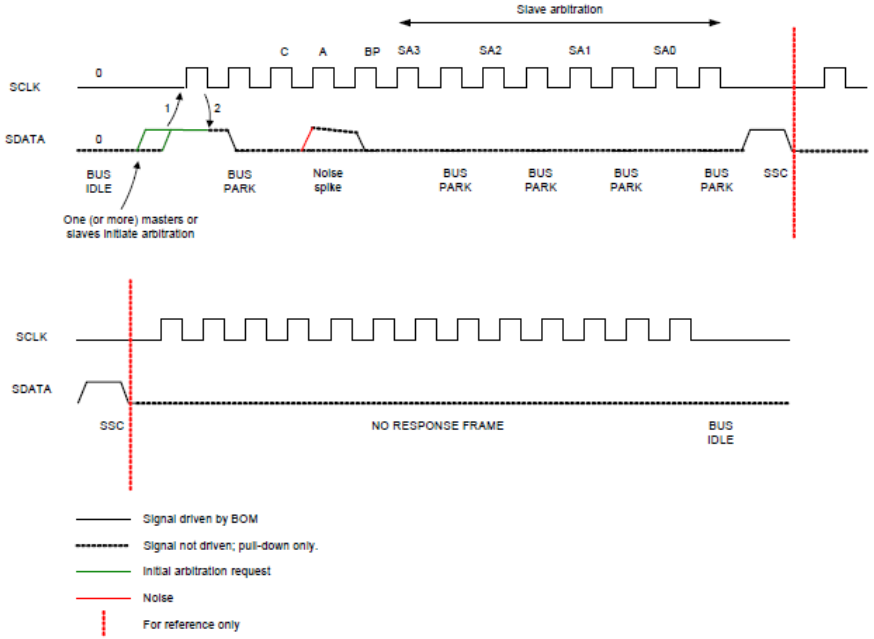

Figure 28 False Slave Arbitration due to Noise

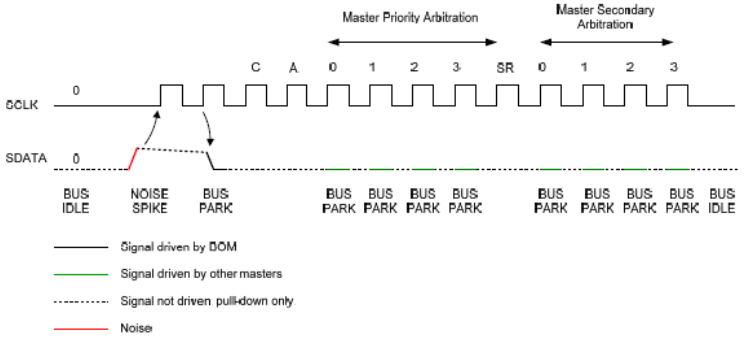

Figure 26 False Bus Request Detection

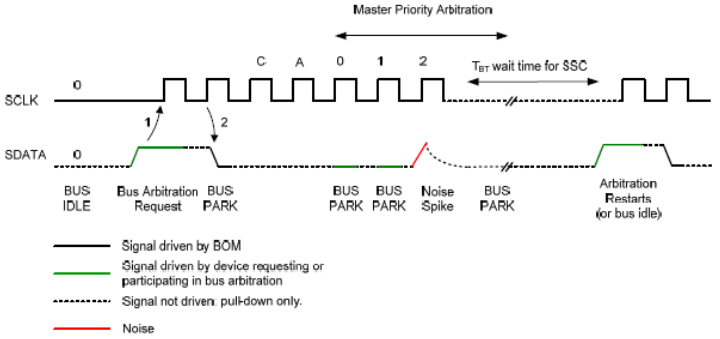

Figure 27 Noise During Priority Slots of the Bus Arbitration

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Conclusions and References

- MIPI-SPMI protocol plays a vital role in reducing the number of pin connections in a chipset as it support multi-master and multi-slave systems and various types of data path commands.
- There are certain areas which needs some improvement. Some of them has been addressed in MIPI-SPMI spec ver. 2.0. Some more are yet to be taken care as suggested by us in this presentation.
- **Reference**: MIPI® Alliance Specification for System Power Management Interface (SPMI) - Version 1.0 – 27 October 2008

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