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MIPI High Speed Serial Technologies: Debug & Conformance Testing Challenges and Solutions

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Tektronix

2017
MIPI ALLIANCE
DEVELOPERS
CONFERENCE

BANGALORE, INDIA
MIPI.ORG/DEVCON

Speakers

Ramesh P.E

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Tektronix

Agenda

- MIPI D-PHY℠ Overview of signal characteristics
- Measurement/Probing Challenges
- MIPI C-PHY℠ Overview of signal characteristics
- MIPI C-PHY℠ Clock recovery & Switching Jitter
- Stress signal generation for Receiver Testing
- Q/A

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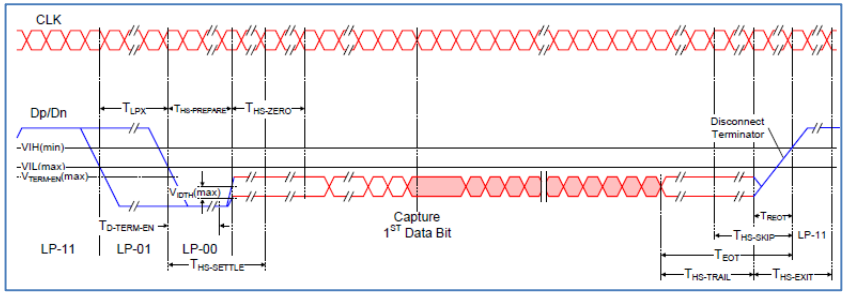
MIPI D-PHY : Signal Characteristics Overview

- Detection of LP-HS transition and timing measurements on that transition



- Dynamic switching of terminations between LP and HS mode
- Measurements on clock and data lanes verify voltage and timing parameters, separate LP from HS bits
- D-PHY v2.0 onwards included eye diagram and jitter measurements

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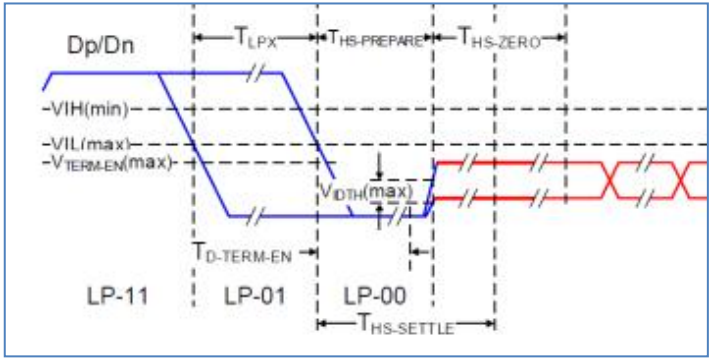
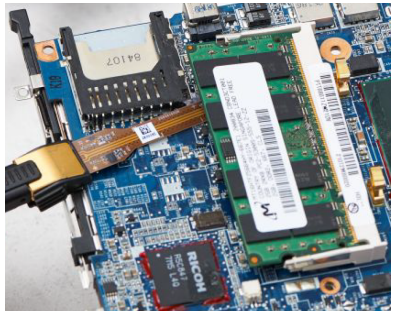
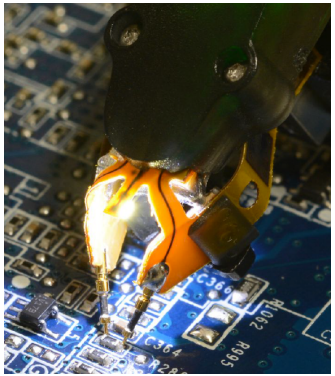
Probing without losing signal fidelity

- High speed mode, Low power mode
  - High impedance to 50ohm bus
- Access to tight test locations







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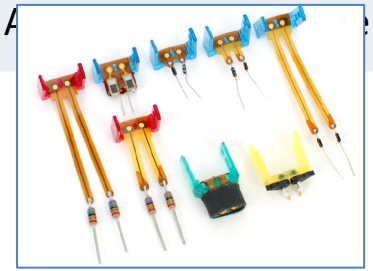
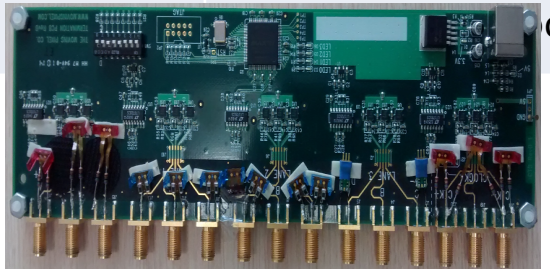
Probe lead length effects

Length of the lead	Rise time
Adapter with full length wire	227ps 46% Overshoot
Adapter with half length wire	126ps 48% Overshoot
Adapter with quarter length wire	59ps 43% Overshoot
A…	…ot





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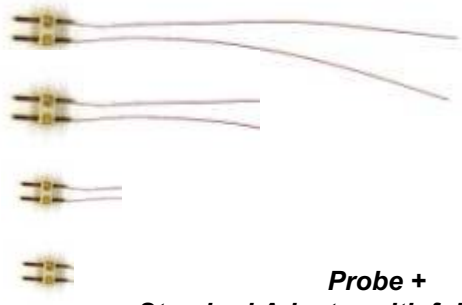
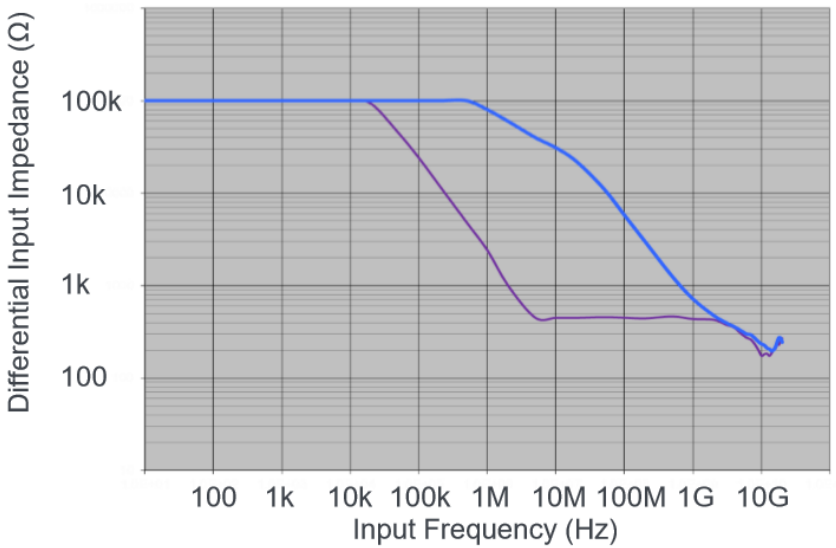
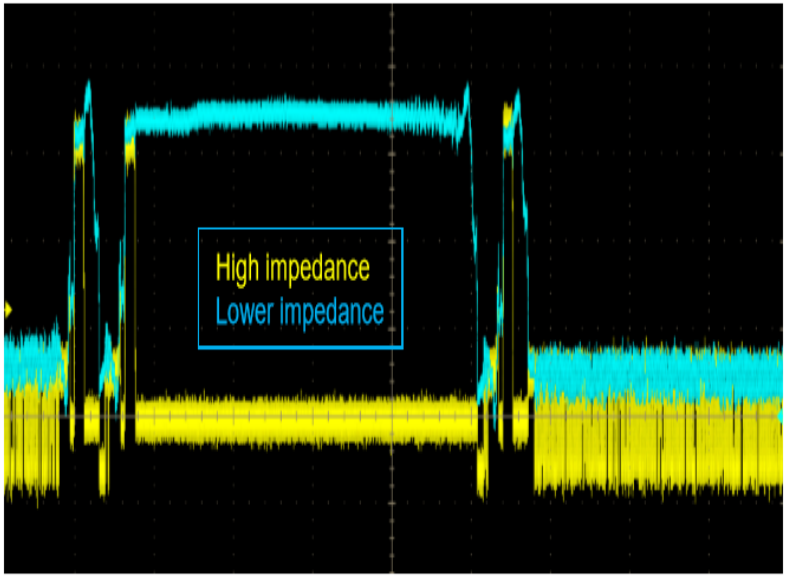


Probe +
Standard Adapter with full length wire

Probe impedance





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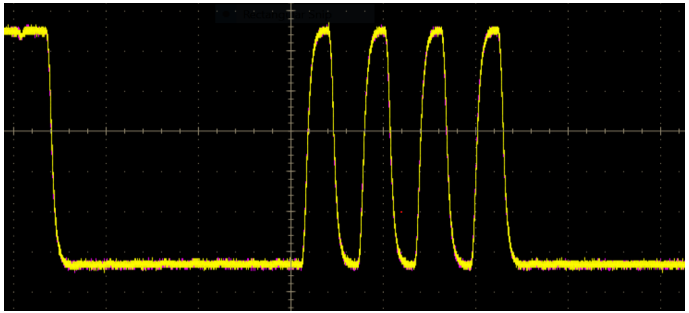
Measurement to be immune to instrument noise

- MIPI D-PHY: LP Slew rate measurement limit of 150 mV/ns
  - 50mV sliding vertical window, and average of all the edges
- A LPF filter to limit the high frequency noise



Note that this slew rate measurement is very sensitive to high-frequency noise (contributed primarily by the DSO), which can translate to high-frequency deviations in the slew rate curve data. Because it is not desirable to include these deviations in the measurement, it is advantageous to filter the source waveform prior to performing the slew rate measurement, which will remove the high-frequency deviations. To reduce the measurement noise, a 400-MHz, 4th-order Butterworth lowpass filter will be applied to the source waveform prior to performing the measurement. (Note that for simplicity, the test filter will be used for all tests 1.1.x and 1.2.x, however the benefit

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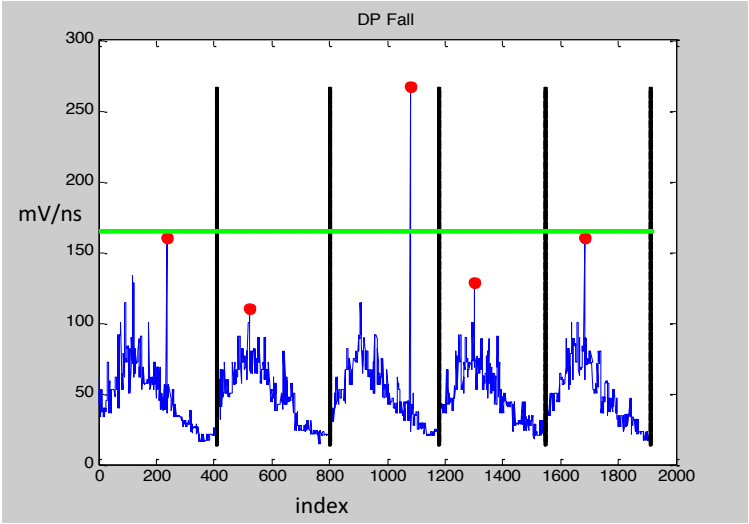
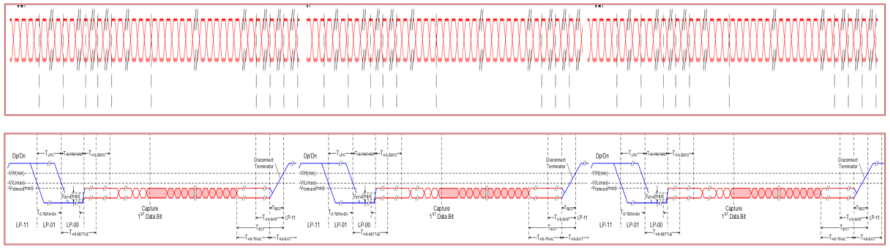
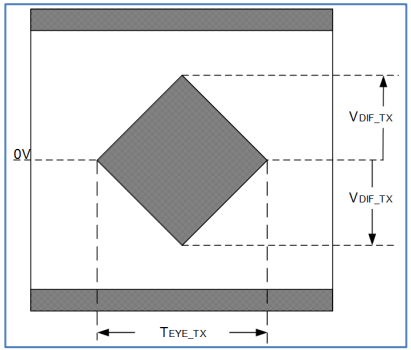
Instantaneous Slew Rate



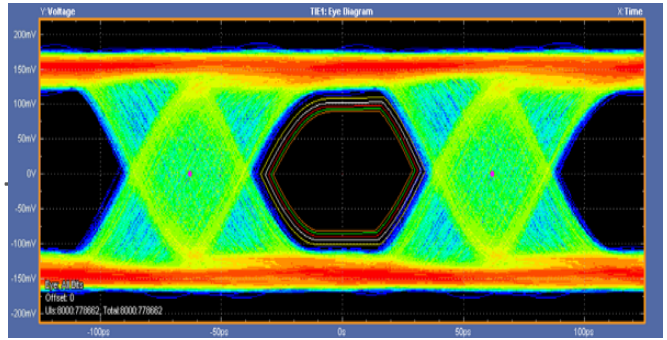
Debugging using Jitter extrapolation

- MIPI D-PHY Tx HS Eye Diagram
- Analysis of Continuous(Recommended) or Burst Data





- Analysis duration
  - (1) Sufficient to analysis at BER 1E-6 (Prorated Mask)
  - (2) Desirable to analysis at BER 1E-12
    - Sophisticated extrapolation software



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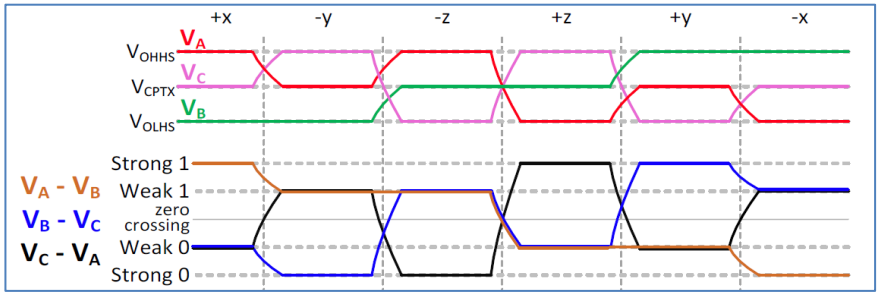
MIPI C-PHY : Signal Characteristics Overview

- 1st triggered edge recovered from A, B, and C wires
- Eye mask placement for optimal eye opening
- Rise/fall times are different for different transitions
- Derive three differential signal from 3 wire signal
- All the three eye diagram to be tested (V_{AB},V_{BC},V_{CA})



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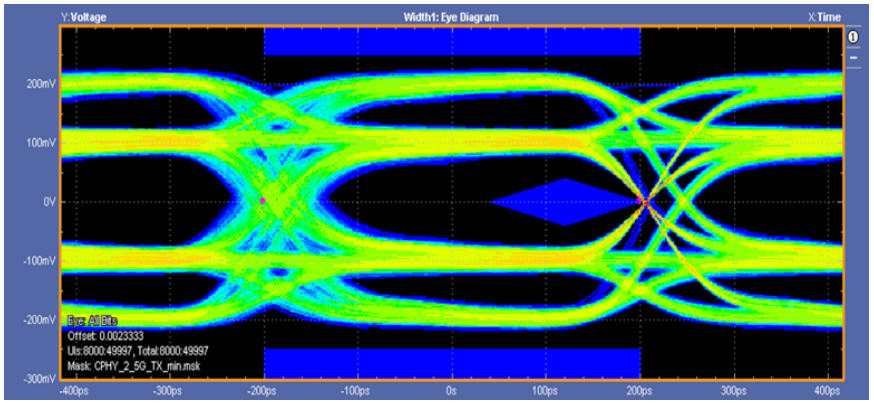
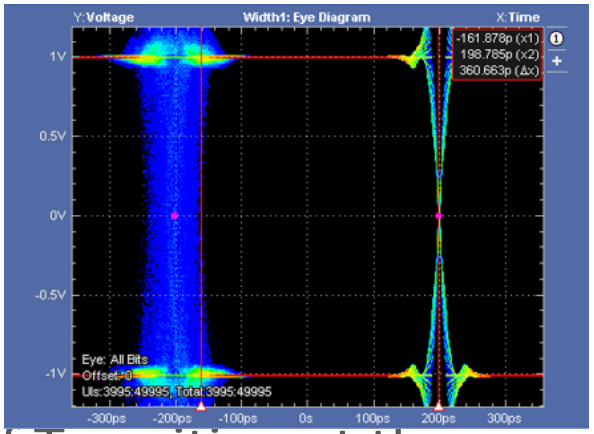
Switching Jitter and RT/FT



Clock Jitter



- Switching Jitter varies with number of Transition at the cross over.
- Data Jitter is 92psec, clock jitter is 61psec. Increment in clock jitter is not the same reflected in data, but increased by 3 folds (means 15 psec on clock increases data jitter by about 40 psec)

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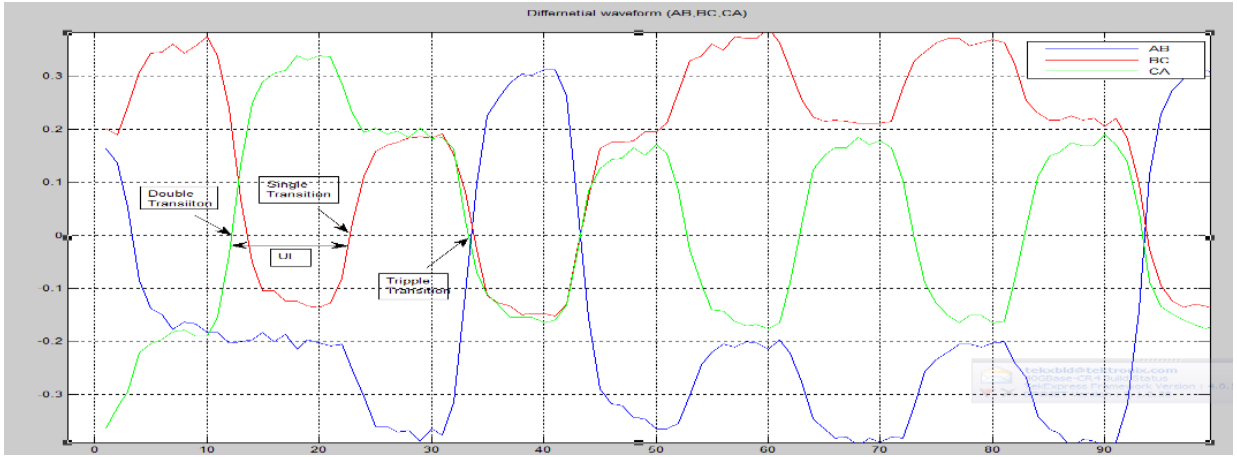
Switching Jitter based on Transition Type



Transition Type	Min UI(ps)	MAX UI(ps)	Mean
Single	340.6	436.95	389.83
Double	368.4	469.4	409.9
Triple	359.27	457.1	401.6

Transition Type	Min Time	Max time	Mean
Double	20	71	45
Triple	0.97	61	29

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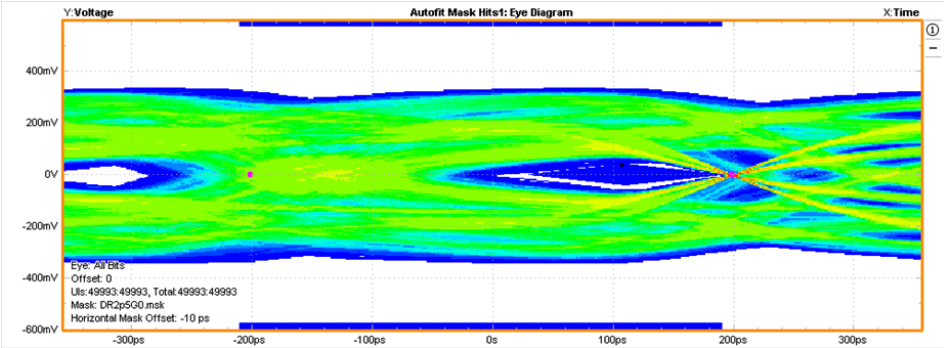
Unit Interval Analysis of stressed signal



Transition Type	Min(psec)	Max(psec)	Mean(psec)
Single	266.74	507.7	383.84
Double	323.23	559.83	418.29
Triple	302.4	508.41	393.99

Time difference of transition Δt

Transition Type	Min(psec)	Max(psec)	Mean(psec)
Double	55.95	178.48	111.9
Triple	5.193	158.2	55.6

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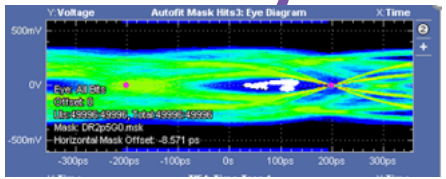
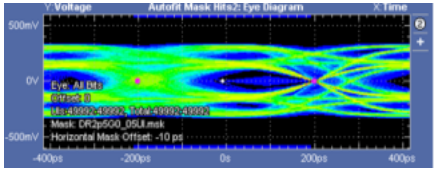
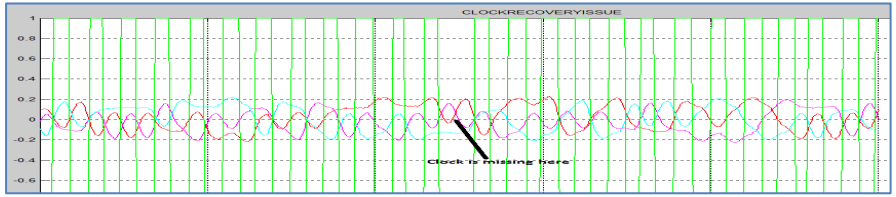
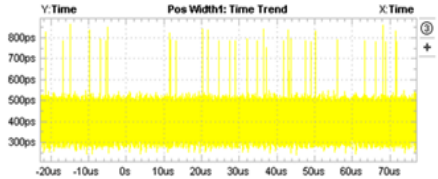
Switching Jitter with stress signal can affect the clock recovery

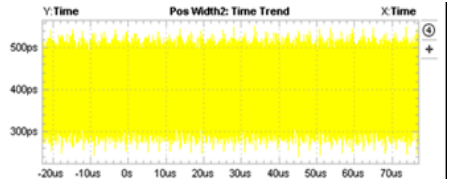








Recovered Clock before recovery improvement



Recovered Clock after recovery improvement

Clock Recovery works fine as long as unit interval variance due to switching jitter less than 0.5UI, If not then clock recovery will lock the data either early or late arrival data and results in Mask violation.
Clock transition is missed because of an ISI coupled with switching jitter

How the clock is missed?

We assume that jitter is less than 0.5UI. The difference between early occurrence and late occurrence of the transition of the differential signal can be less than 0.5UI.

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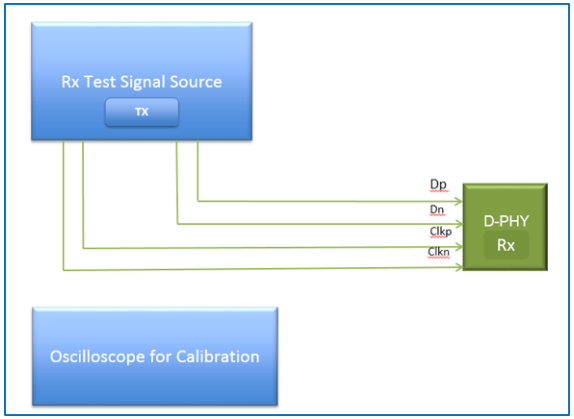
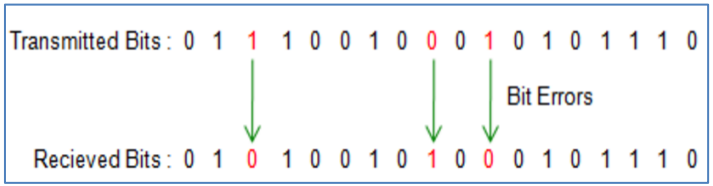
Receiver Testing

- Philosophy
  - Stimulus calibration based on parameter
  - Stimulus fed to the Rx
  - Check for error free reception
- Equipment
  - Waveform Generator
    - Data and clock lanes
  - Oscilloscope for Calibration
  - Choice based on MIPI D-PHY/C-PHY spec versions
- Observables
  - Bit errors detected





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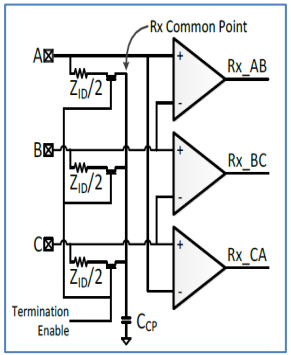
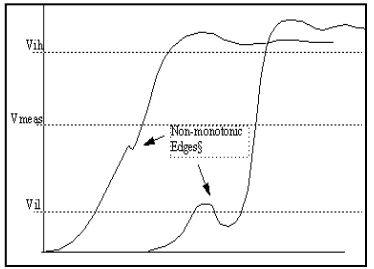
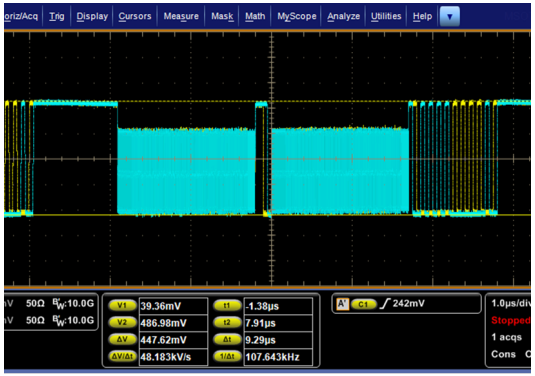
MIPI C-PHY Receiver Test : Signal Generation

- Monotonic signal generation
- C-PHY Encoding – bits, symbols, wire states
- Pseudo Random test patterns PRBS9/11/18
- Stressors
  - rise/fall time, duty cycle distortion (DCD), ISI,
- Differential and Common mode voltage control
- RX Test scenarios
  - Sequencing different waveforms created using LP, HS and LP-HS Mode
  - Defining various start up sequences by varying different parameters like jitter , length of sequences and looping these sequences
  - Fine granularity and control of various parameters like pre-amble, sync, post-amble
  - Ability to create waveforms for LP Only, HS only and LP-HS transition







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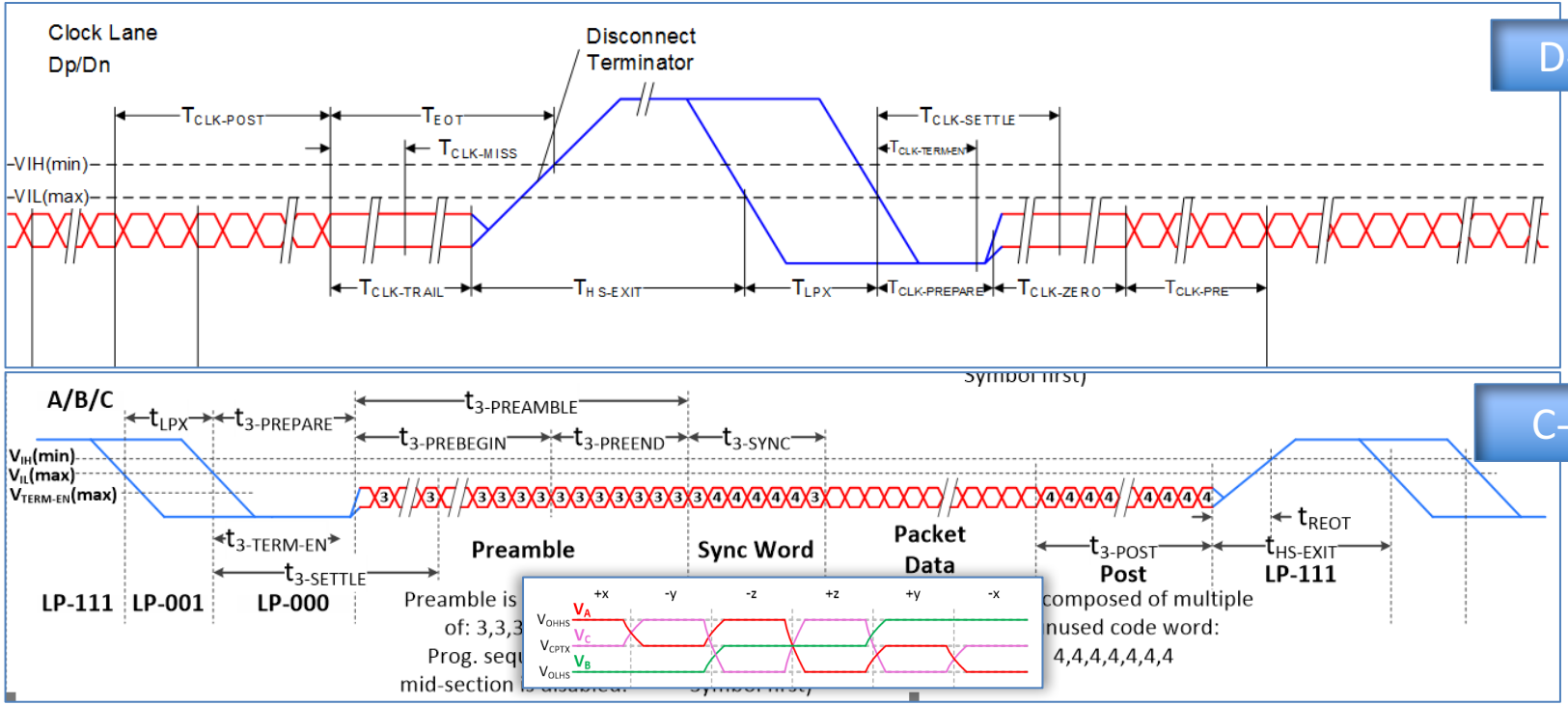
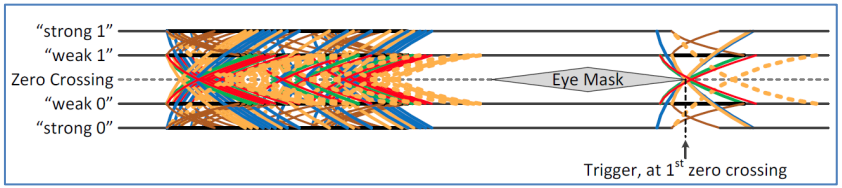
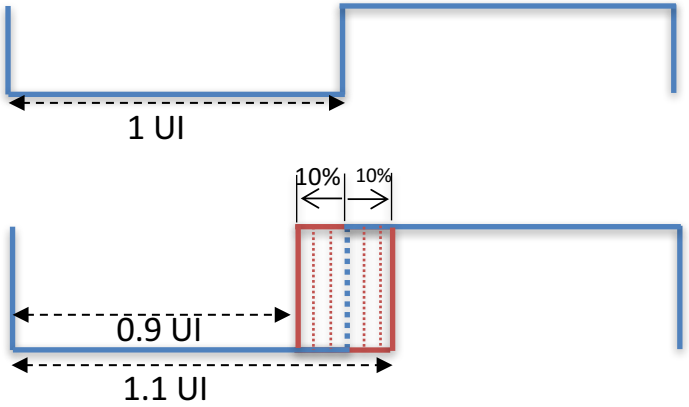
Rx test parameter precision, flexibility & range



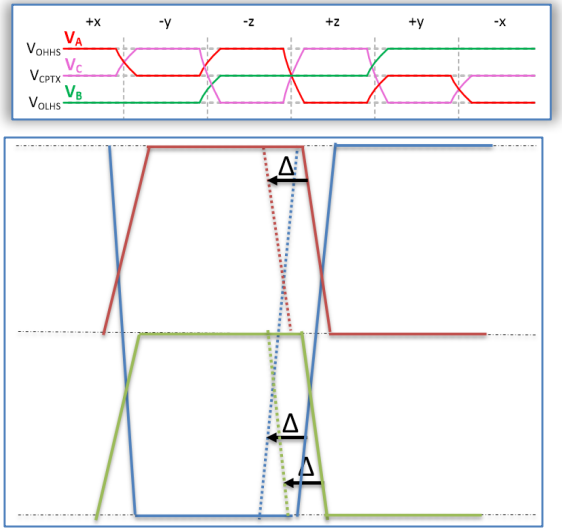
Multilevel Signal: Duty Cycle Distortion

- C-PHY receiver stress with Duty Cycle Distortion





- A symbol interval, all the lines would have the same DCD(Δ), but this would change with every symbol



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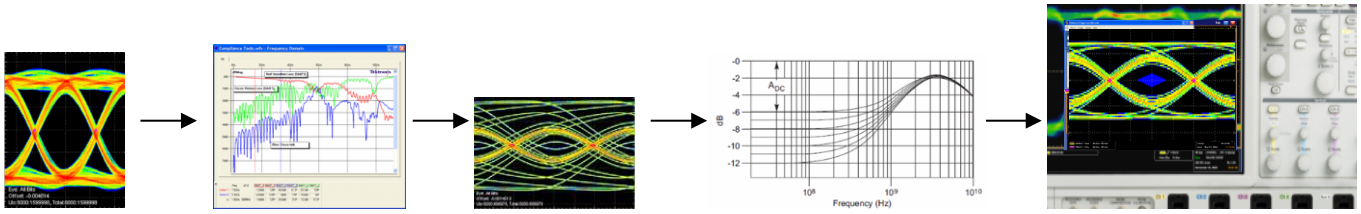
Link Analysis



- Maximize Margins - Compensate for margin loss due to test fixtures
- Remove Reflections
- Open Closed Eyes - Apply receiver equalization to compensate for channel loss before analysis
- Compliance Test - require de-embedding, channel embedding, and equalization

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Backup

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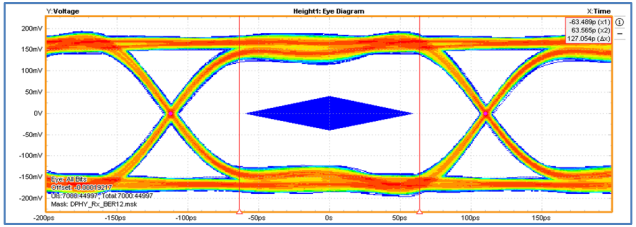
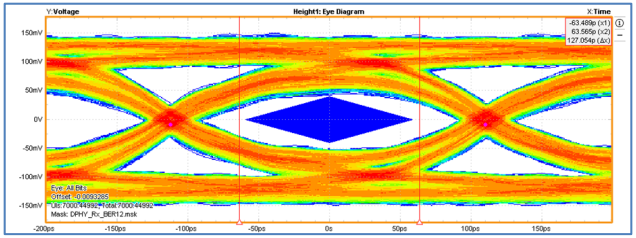
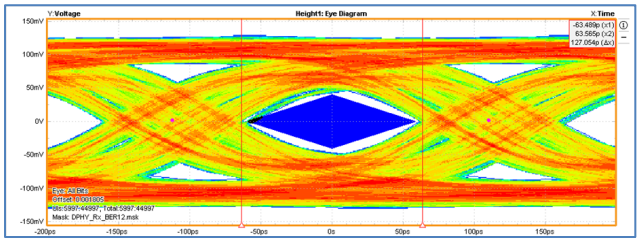
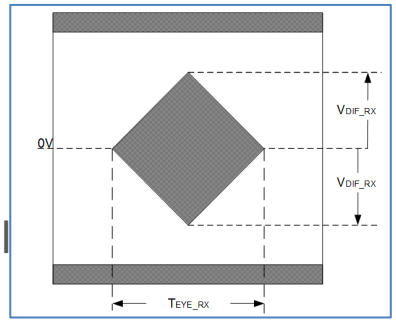
D-PHY Rx Jitter Tolerance

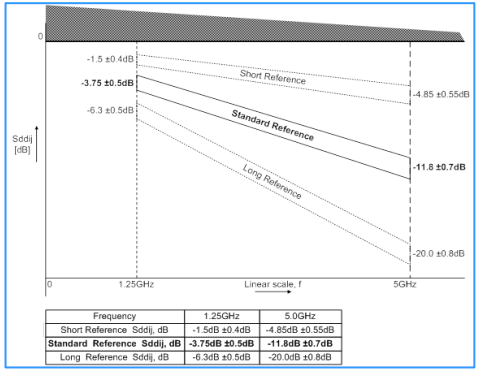






- RT/FT Control
- Insertion Loss
- De-Emphasis
- Periodic Jitter & VOD Control
- Static Skew
- DC common Mode
- SSC





Frequency	1.25GHz	5.0GHz
Short Reference Sddj, dB	-1.5dB ±0.4dB	-4.85dB ±0.55dB
Standard Reference Sddj, dB	**-3.75dB ±0.5dB**	**-11.8dB ±0.7dB**
Long Reference Sddj, dB	-6.3dB ±0.5dB	-20.0dB ±0.8dB

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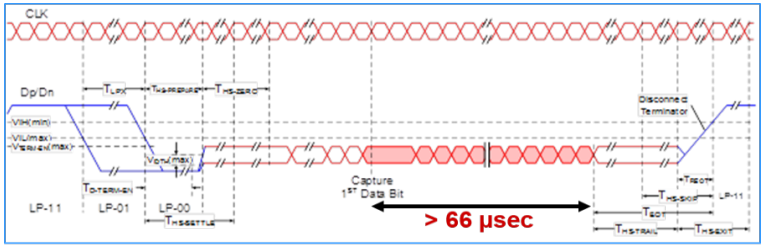
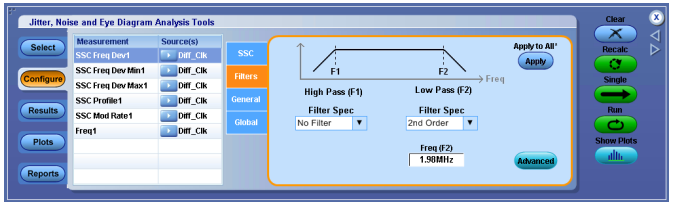
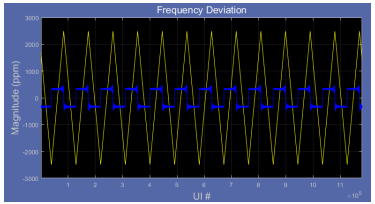
D-PHY Tx Test: Spread Spectrum clocking

- SSC Testing
  - Modulation Rate = 30KHz (min)
  - Measure over =>2 SSC cycles
  - Device Test Modes/options
    - HS data length > 66 µsec
    - HS data '101010…'



Jitter, Noise and Eye Diagram Analysis





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