mipi® DEVCON

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Emulation of DUT using UniPro℠ RMMI as a Standard Interface

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CONTENTS

I. INTRODUCTION

- Increased Complexity of System-on-Chip (SoC) has made verification an extremely difficult task.
- The effective speeds of simulators used during functional verification make it difficult to run many system level tests.
- Testing hardware and software together on the actual chip is difficult, time consuming and expensive.
- Co-verification of hardware and software at an early stage with the aid of an emulation system and before silicon availability is a viable and increasingly popular strategy.
- These solutions allow software teams to develop many applications before first silicon arrived and thus greatly reduce development time.

Features of Hardware Emulation Platform

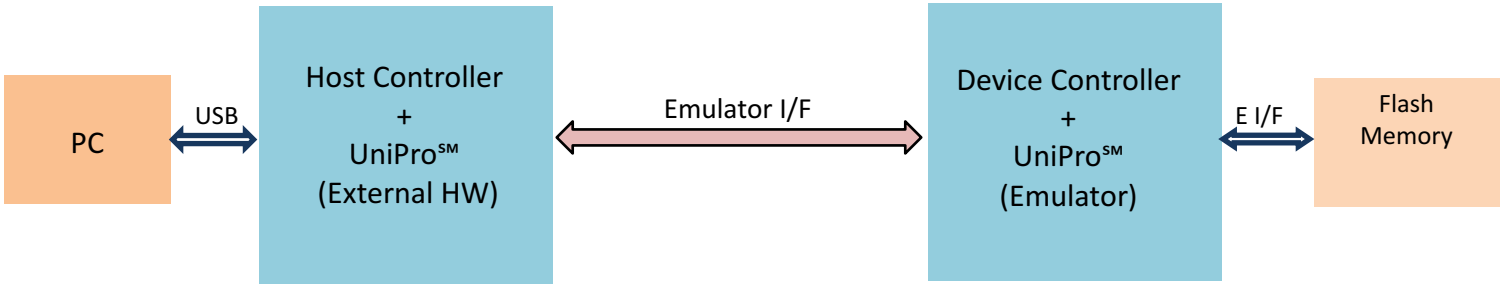
- Enables to run and Debug full end to end system level verification in a complete Emulation environment that applies real world operating conditions to the DUT.
- Full Emulation system, from OS level to BIOS level, which enables us to directly emulate devices upon hardware in real environment enhances the confidence of System on Chip (SoC) design.
- Facilitates the development of firmware/ROM code before Silicon Availability, resulting in significant savings in time to market and improved product quality.
- Enables faster Debug and Development of Hardware as well as Software by providing rich debug environment that lets users look at all signals throughout an entire session .
- The platform can also be used for dynamic power analysis in a realistic system-level environment to enable more optimal tradeoffs between power and performance.

Comparison of FPGA Prototyping and Emulation

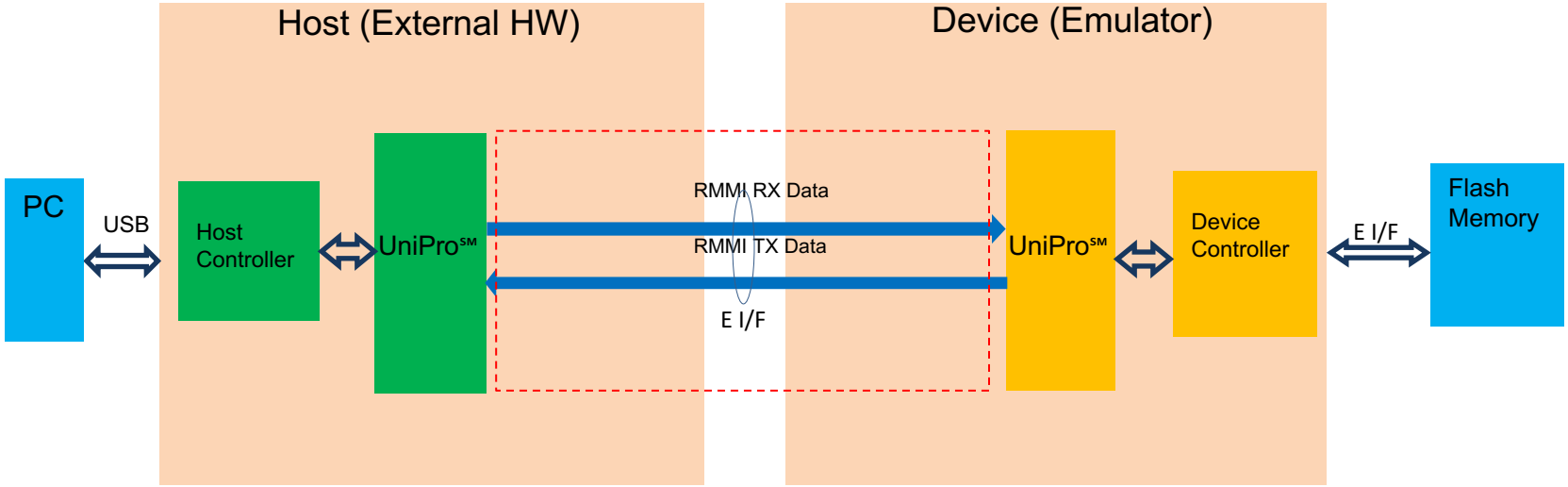
	FPGA Prototyping	Emulation
Pros	✓ RTL Accurate ✓ High Frequency ✓ Relatively cheap	✓ Accurate Clock control ✓ Accurate Power Control ✓ High visibility ✓ Performance analysis ✓ Less Bring up Time
Cons	× No Clock control × No Power control × Poor visibility	× Expensive × Low frequency

UniPro℠ RMMI based Emulation Platform

- The Platform has been developed for a UniPro℠ RMMI based flash device controller
- The hardware includes an FPGA based host platform connected to the device emulator
- The host is also connected to a PC via USB port and provides user interface
- Flash memory protocol is implemented with real flash memories connected using Emulator Interface Cable

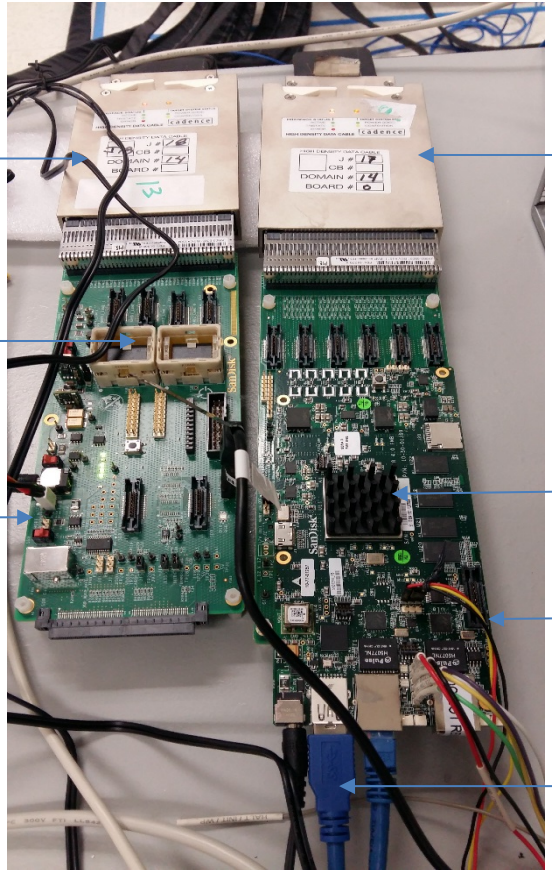


II. EMULATION SYSTEM OVERVIEW



WD's custom Host based on UniPro℠ RMMI Interface

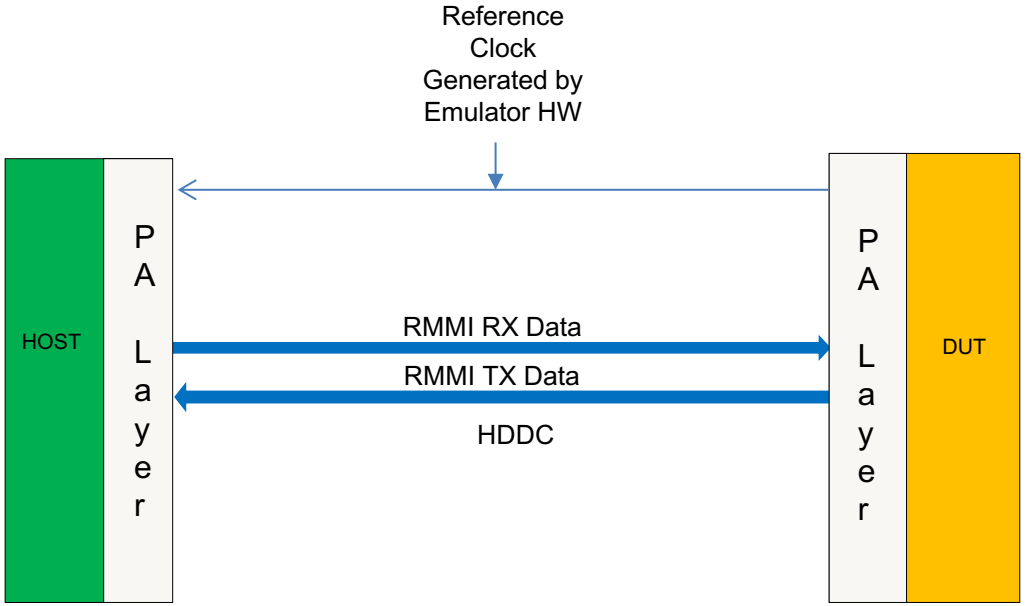
SYSTEM OVERVIEW:



Implementation Overview

- UniPro℠ RMMI Interface based flash device controller is mapped onto Emulator and a FPGA based Host platform connected together through SanDisk's custom made UniPro℠ RMMI based Solution.
- Since off-the-shelf RMMI adapter is not available, it was a challenge to develop and prove.
- The Host controller is responsible for managing the data transfer between Host SW and device.
- MAC layer is responsible for transporting any kind of data between applications like the camera, display and memory devices on the same physical link.
- The MAC layer can be implemented using any of the standard MIPI protocols like MIPI UniPro℠, MIPI CSI-3℠, MIPI LLI℠, MIPI DSI-2℠ and M-PCIe.
- Flash memory protocol is implemented with real flash memories connected to device controller using HDDC cable.

UniPro℠ RMMI Solution



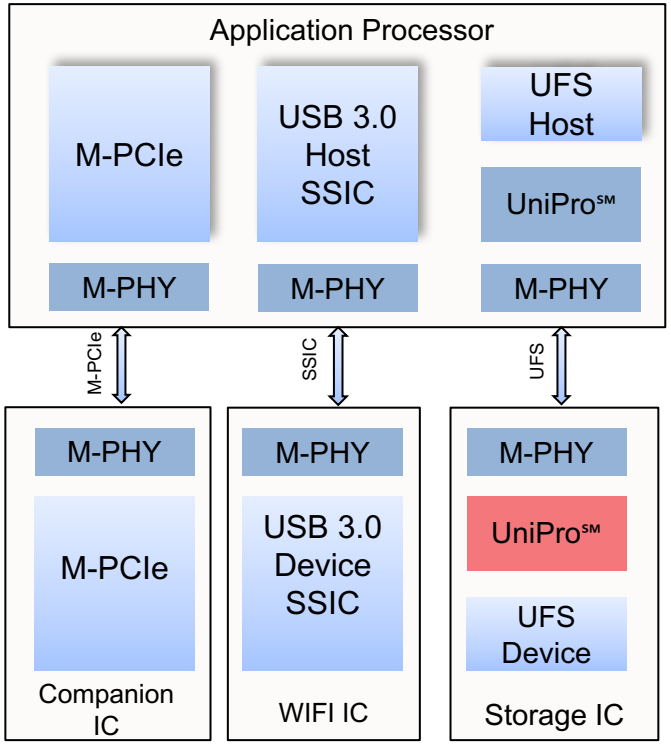
Implementation Overview of RMMI based solution

- UniPro℠ PHY Adapter layer is responsible for abstracting the details of the PHY technology. Higher protocol layers are agnostic as to which physical lanes are being used.
- The UniPro℠ RMMI adaptor is built around the standard digital Reference M-PHY Module Interface (RMMI). The RMMI interface adheres to MIPI UniPro℠ and MIPI M-PHY Specification.
- The UniPro℠ RMMI data bus is a dual simplex, parallel interface which is directly connected to the Device.
- Due to the flexibility provided in UniPro℠ RMMI standard, width of the data buses conveying data to and from the PA layer can be increased.

Features of this Solution

- The UniPro℠ RMMI solution enables seamless integration of MIPI MPHY protocol based Devices with wide range of high-speed interfaces for mobile applications including JEDEC Universal Flash Storage (UFS), USB SuperSpeed InterChip (SSIC), PCI-SIG M-PCIe™, MIPI UniPro℠, MIPI DigRF v4, MIPI Low Latency Interface (LLI℠) and future MIPI CSI-3℠ and MIPI DSI-2℠.
- It provides wide bandwidth and sufficient flexibility to be attractive for multiple applications, but which can also be covered with one physical layer technology.
- The interface to the link protocol-specific controller (host or device) is compliant to the MIPI M-PHY specification version 3.0, which allows seamless integration of the two IPs, namely the controller and the MIPI M-PHY, into the chip design.
- Enables rapid creation of system-level environments using the same hardware and software that the real silicon will use.
- Symbol clock is generated by Emulator and shared between the transmitter and receiver.
- Supports transfer of data up to 2 TX and 2 RX lanes.

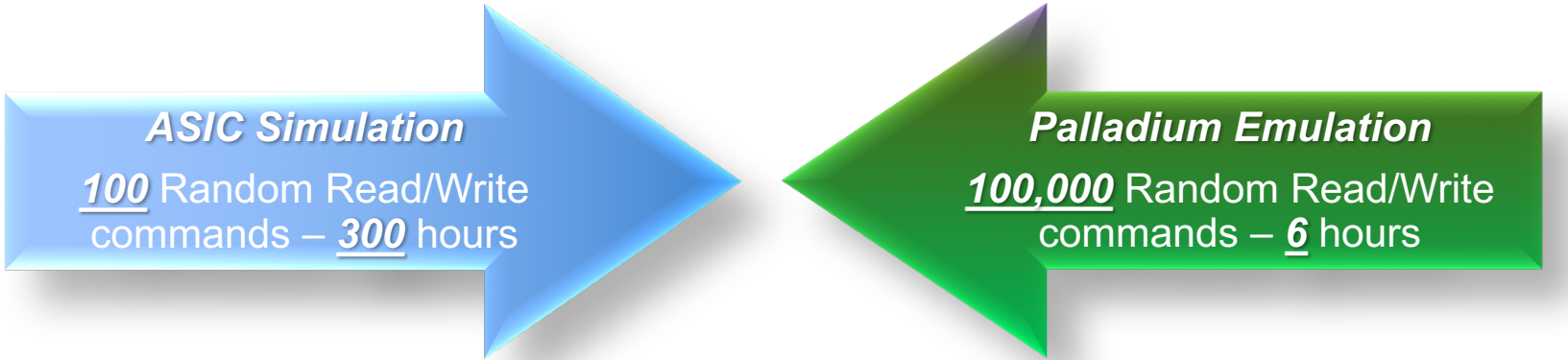
Uniport based Applications in Mobile Platform



- The UniPro℠ RMMI Adopter solution can be used as standard Interface in the Hardware emulation platform to connect Wide range of IP's or SoC's which implement MIPI M-PHY as their Physical layer.

III. Results and Discussions

- Datapath Random test for ASIC SOC Verification



Results and Discussions

- Transfer of large user data up to 100MB via multiple packets from Host to flash memory completed successfully in about 30 min.
- The functional hardware emulation is 20000 times more faster than software simulations.
- Achieved emulation throughput of 16 Mbps on Tx and Rx
- Early debug and development of FW code accelerated the silicon validation cycle as the code reached a high level of confidence with the testing on the emulator. These can be run on silicon with no changes.
- Emulation approach is suitable to detect functional misbehavior caused by power control
- Performance analysis of the system
- To enable optimal tradeoffs between power and performance, Dynamic power analysis in a realistic system-level environment can be done to analyze issues like peak power consumption and supply voltage drops which can compromise a hardware's functionality.
- Estimated saving in Time-To-Market by 4-6 weeks.

IV. CONCLUSION

- Emulation Platform offers highest verification performance over all other methods without abstracting out critical portions of a real system.
- RMMI Adopter solution is built around standards compliant interfaces and can be reused between projects eliminating re-implementation of custom verification environments.
- This system level approach to verification helps us find issues that escape from the traditional verification techniques.
- Provides advanced debug environment for Hardware/Software co-validation
- Improved product quality, reduced Time-To-Market and Plug and Play feature of Emulation platform along with RMMI solution makes it an essential tool in the SoC development cycle despite an additional cost overhead.

Q&A

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THANK YOU

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