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MIPI ALLIANCE DEVELOPERS CONFERENCE

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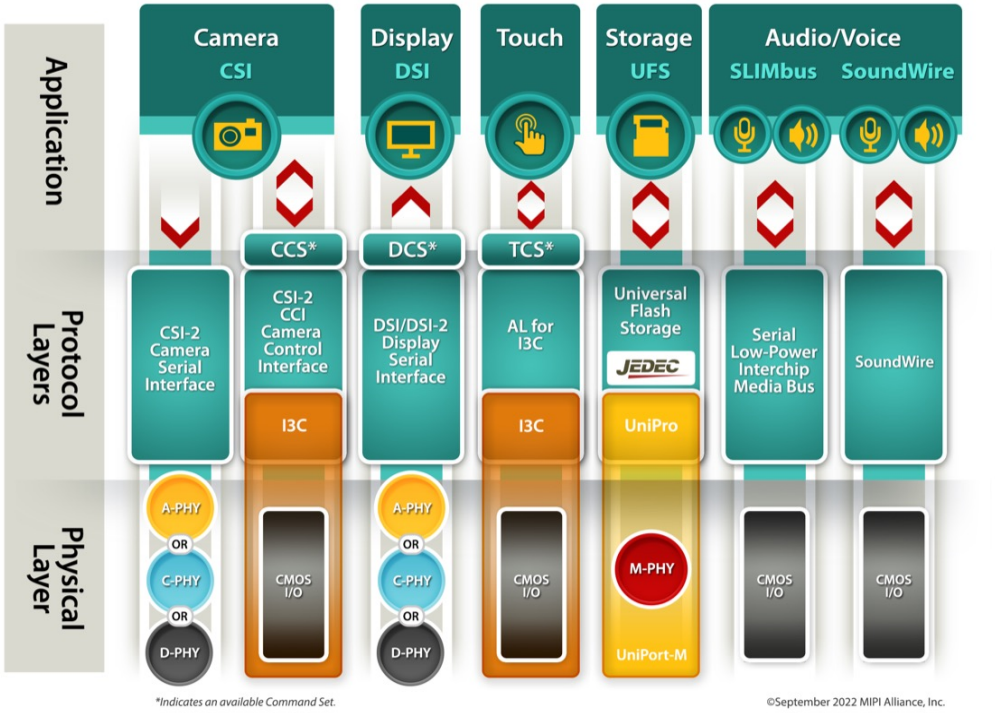
Leveraging MIPI DSI-2℠ & MIPI CSI-2® in Low-Power Display & Camera FPGA-based Subsystems

Agenda

- Overview of MIPI in Display and Sensor Applications
- System Development Trade-offs in ASIC and FPGA
- MIPI FPGA in China
- Examples using Hercules Microelectronics HME H1D03
- Mixel MIPI D-PHY℠ Overview
- Conclusion

MIPI for Mobile & Mobile-Influenced Devices

- MIPI specifications designed from the ground up for applications targeting:
  - Low power
  - High bandwidth
  - Low EMI
- Target expanded from mobile to “beyond mobile” applications:
  - Automotive
  - IoT
  - Wearables
  - Industrial applications



MIPI in Display

- MIPI DSI-2 is used in many displays with low power requirement
  - In addition to mobile, tablets, wearables, VR/AR/MR, and other consumer products use MIPI DSI-2

Synaptics uses MIPI DSI in VR chipset (VXR7200)

Compound Photonics uses MIPI DSI in AR micro-displays

NXP uses MIPI DSI in i.MX7ULP for wearables, which is used in Garmin Edge GPS

MIPI in Sensor Applications

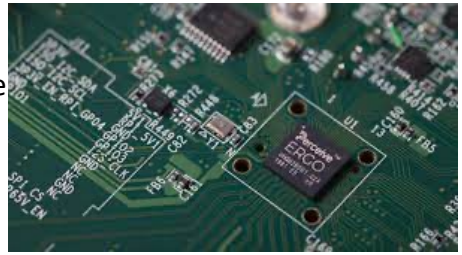
- MIPI CSI-2 is de facto standard for camera and sensors, especially those targeting low power applications

Microsoft HoloLens 2 uses MIPI CSI-2 in depth camera

Teledyne e2v uses MIPI CSI-2 in Snappy CMOS Image Sensor

ams OSRAM uses MIPI CSI-2 in Mira image sensor family

Perceive uses MIPI CSI-2 in Ergo AI edge processor



GEO uses MIPI CSI-2 for multiple generations of automotive geometric processor

MIPI Bridging Solutions

- The increasing number of MIPI devices in different applications, is driving the need for MIPI bridging devices to:
  - Aggregate, split, and post process MIPI CSI-2 and MIPI DSI-2 Signals
  - Enable application processors with different capabilities (high end, low end) to interact with high resolution/low resolution displays and sensors

System Development Trade-offs in ASIC and FPGA

Considerations	ASIC	FPGA
Prototyping Cost	High	Low
Unit Cost (Production Volume)	Low	High
Development Time	High	Low
Process Nodes Availability	High	Low
Foundry Availability Impact	High	Low
Design Customization/Flexibility	High	Low
Post-fabrication Customization	Low	High
End-Product Bring-up Time	Low	High
Power Efficiency	High	Medium

Key	Advantage	Disadvantage

FPGA in Sensor and Display Markets

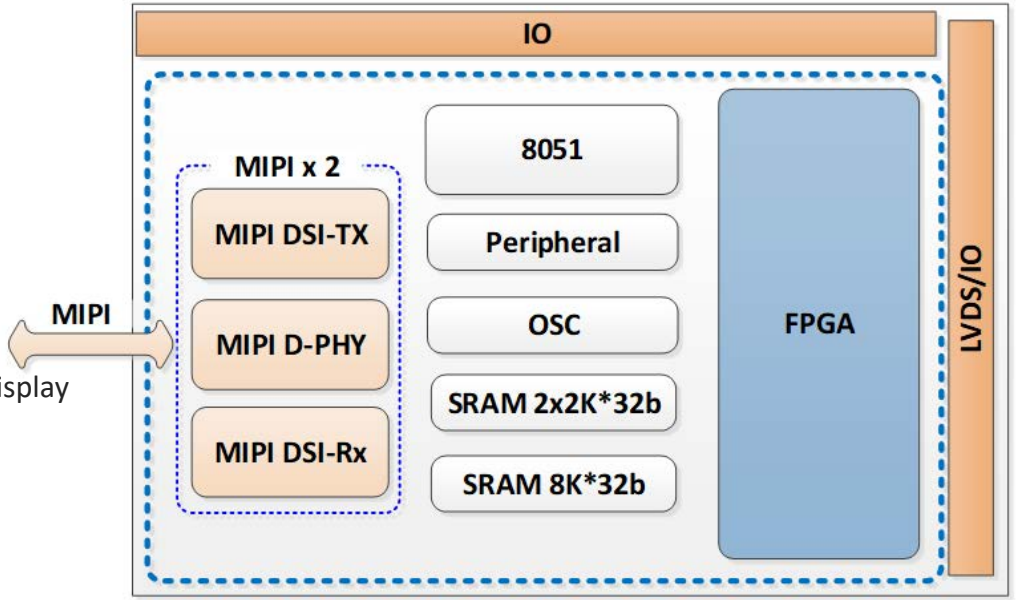
- FPGA in general is useful to prototype and provide proof of concept.
- FPGA deployment in end products is growing:
  - Faster FPGA speeds, decrease in power consumption and cost
  - Customized functions and requirements to target different application and use cases
- Productization challenges:
  - Power consumption
    - » FPGA core power ➔ Compromise between customizable and hardened functions
    - » Limited Process Nodes ➔ Target newer technology nodes to minimize power consumption
  - FPGA end-product realization time
    - » Provide a full reference design to the end customers

MIPI FPGA in China

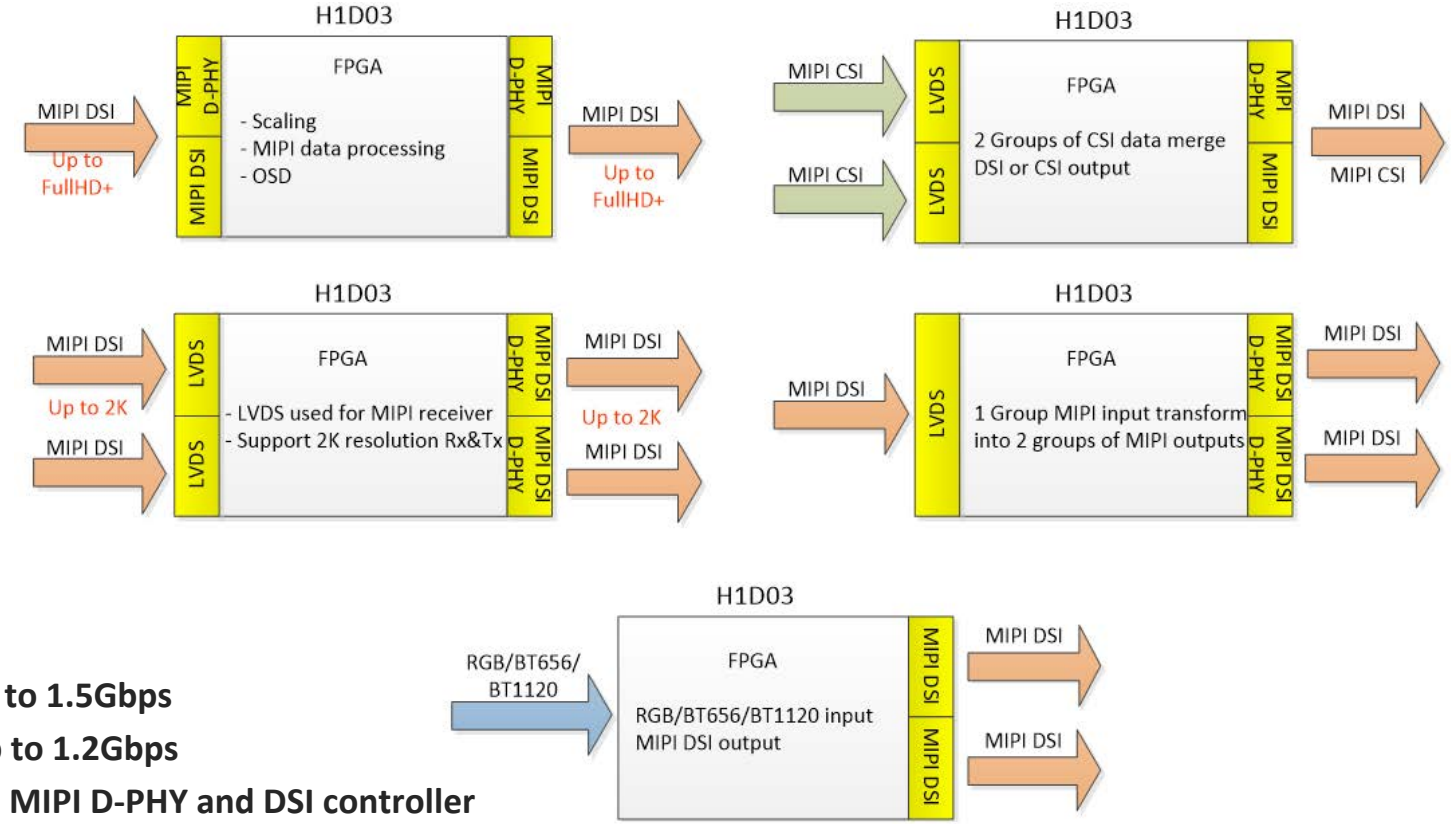
- In China, FPGA using MIPI PHY is trending with several FPGA companies developing one
  - MIPI C-PHY/MIPI D-PHY with MIPI DSI/CSI controller integration is a very good choice for FPGA chip that target MIPI interface bridging solution
  - Compared with using LVDS to emulate MIPI interface, MIPI PHY + Controller hardened core could support higher data rates (1.5Gbps, 2.5Gbps, or higher), is more stable, and consumes less power
  - A hardened MIPI subsystem is an efficient way to reduce power consumption
  - Hardening the MIPI subsystem in an FGPA IC gives the FPGA user the best compromise between flexibility, effort, power, and time-to-market compared to either an ASIC or an FPGA with an unhardened MIPI subsystem
- Why use FPGA to do MIPI interface application?
  - ASIC could cover part of the MIPI interface bridging application, but it more difficult to meet customized requirements such as: video scaling, MIPI command conversion, 1 group of MIPI input to 2 groups of MIPI outputs, MIPI CSI to MIPI DSI

HME H1D03 Features

- **H1D03 FPGA Features**
  - 40nm LP
  - 2K LUT6 (Equivalent 3K LUT4), up to 200MHz
  - 8xEMB18K, 144Kbits
  - 16xDSP, each DSP can be used as 18*18 or 2 12*9
  - LVDS up to1.2Gbps
  - Support LVTTL and LVCMOS 3.3v/2.5v/1.8v/1.2v
- **H1D03 MIPI Interface**
  - On-Chip MIPI D-PHY, up to 1.5Gbps
  - On-Chip DSI Tx&Rx Controller
  - Each MIPI group can be configured as Rx or Tx
  - Support up to 2K resolution (2560x1440) LCD/OLED display
- **H1D03 MCU Features**
  - Enhanced single cycle 8051 core
  - Support UART, SPI, I2C, Timer, and DMA peripheral
- **Other Key Features**
  - 2x2K*32b, 8K*32b SRAM
  - 256bits AES Encryption， Key stored in eFuse
  - On-chip high precision RC-OSC
  - WLCSP72 (3.9mmx3.4mm), W58 (3.9mmx3.4mm), W68 (4.0mmx4.6mm, SiP 64Mb pSRAM)



DSI to DSI, CSI to DSI Bridging

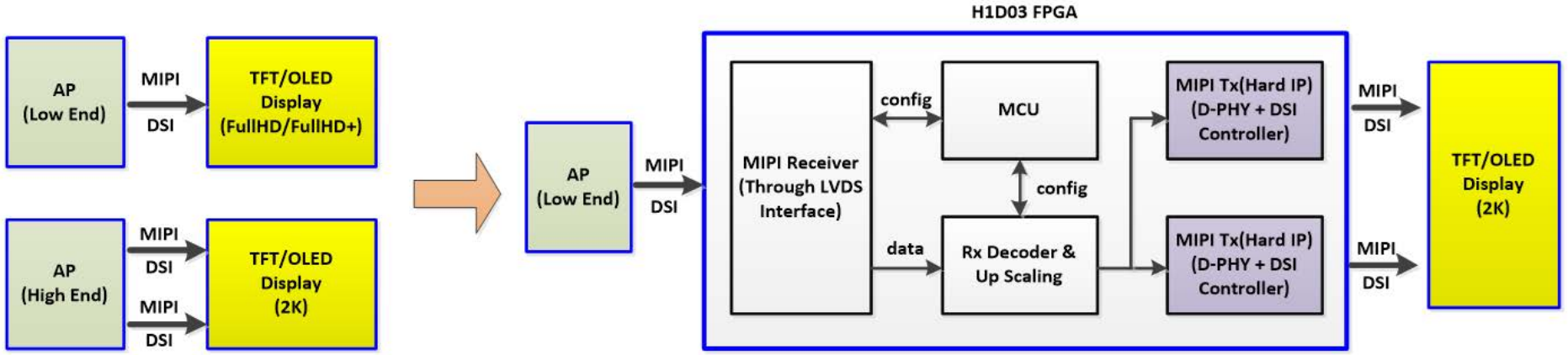


- **MIPI up to 1.5Gbps**
- **LVDS up to 1.2Gbps**
- **On-Chip MIPI D-PHY and DSI controller**

Target Applications for MIPI FPGA

- Consumer application:
  - Cellphone & Tablet MIPI display bridging
  - AR Glass (MIPI to QSPI)
  - e-Paper display
  - Smart home control panel
- Industrial application:
  - Industry camera

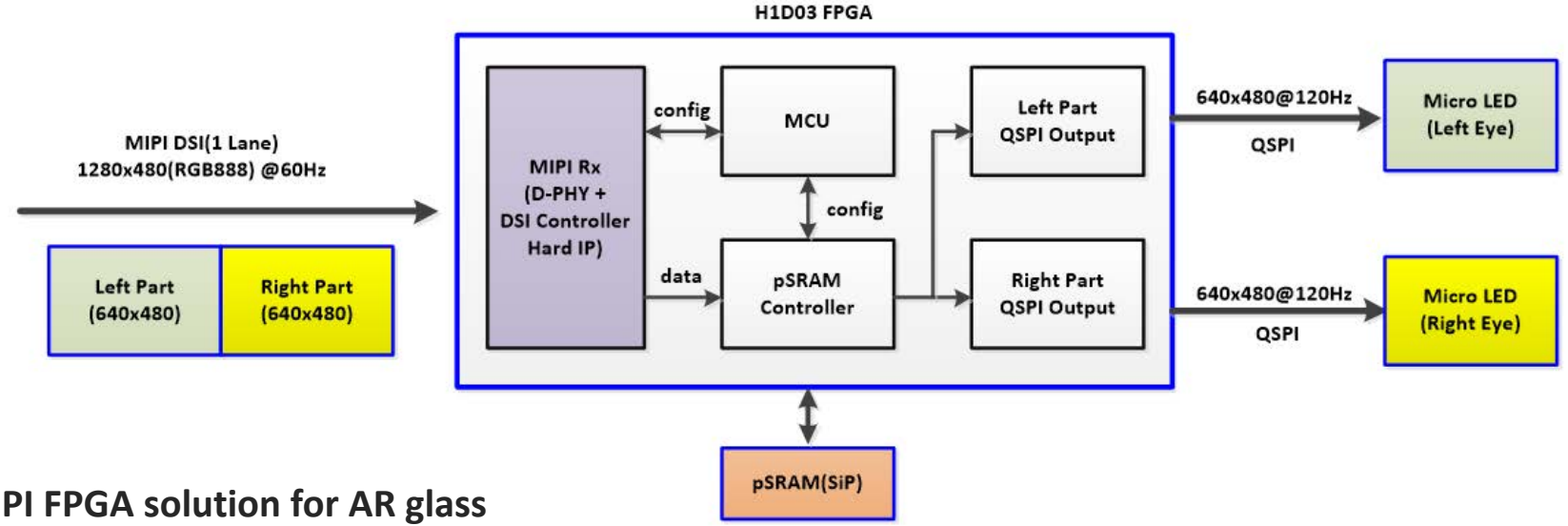
Cellphone & Tablet MIPI Display Bridging Solution



MIPI Display Bridging solution for Cellphone & Tablet

- There are low-end and high-end AP for different Cellphone & Tablet product, only high-end AP has the capability to support 2K (2560x1600) resolution
- MIPI FPGA could help to use low end AP to support 2K display, using MIPI hard IP for interface and FPGA logic to implement up scaling function

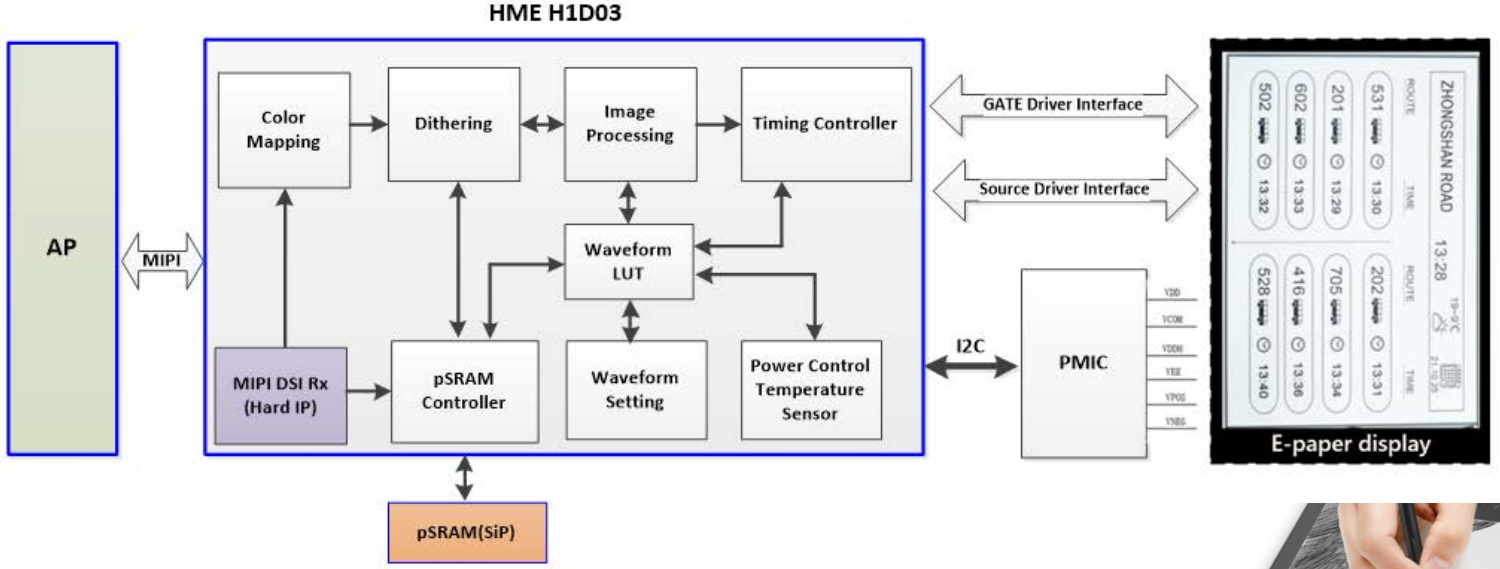
AR Glass (MIPI to QSPI) Solution



MIPI FPGA solution for AR glass

- Receive RGB data from MIPI interface (using MIPI D-PHY and DSI controller Hard IP) and drive the Micro LED with QSPI interface
- Using pSRAM as frame buffer, with the capability to increase the display frame rate from 60Hz to 120Hz
- Small package (4.0*4.6, SiP pSRAM) and low power consumption

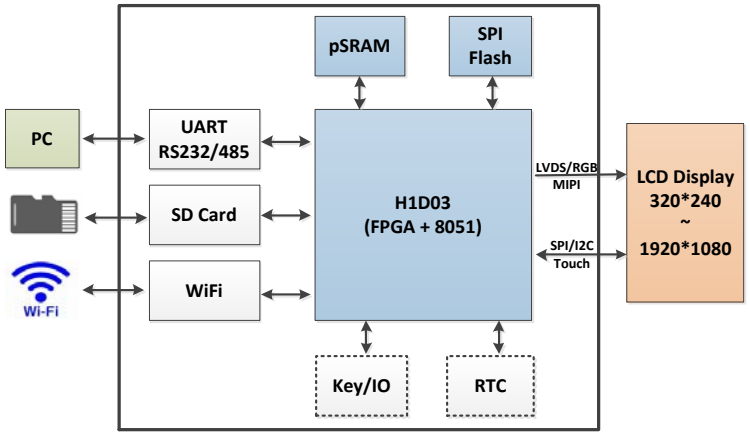
e-Paper Display Solution



MIPI FPGA e-Paper Display Solution

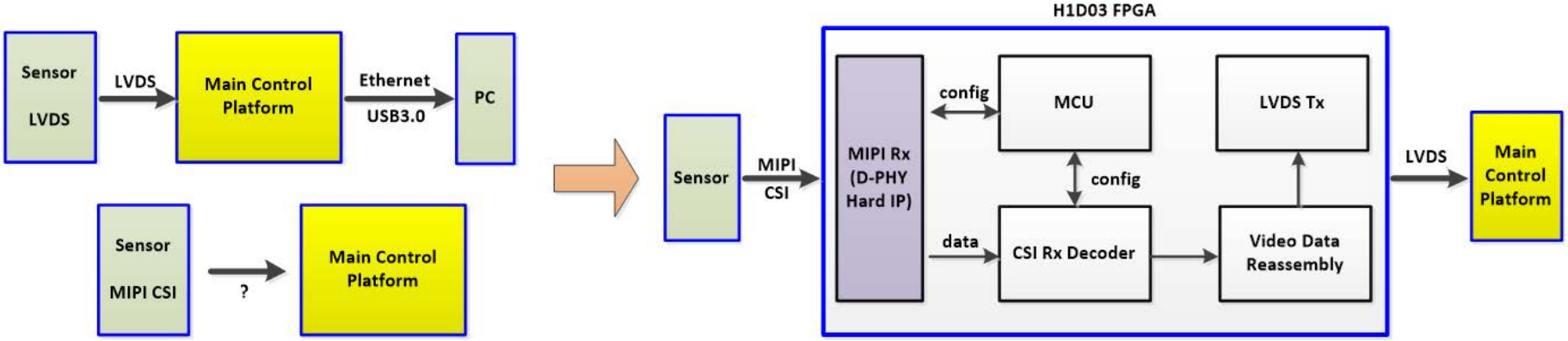
- Single chip solution for e-Paper display control. Most of AP can not support e-Paper display directly, except basic timing control, a MIPI FPGA can also support dithering and color mapping algorithm to get better visual display

Smart Home Control Panel Solution



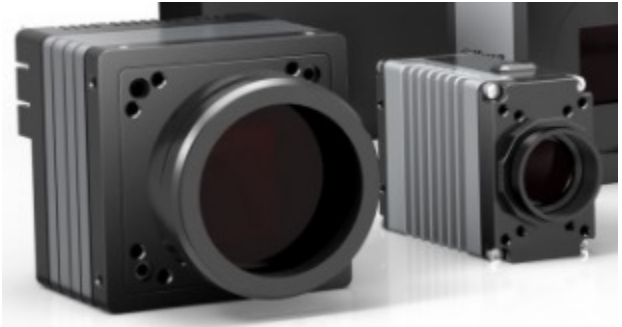
HMI Solution	
Features	**GUI**
• Embedded GUI support • RGB565(16bits)@1080p • LVDS/RGB/MIPI • WiFi network and upgrade support • SD Card support • Provide windows development platform to emulate GUI operation and easy to transform to H1D03	• Complete GUI framework • Good visual effect • Support button, diagram, table, slider and image etc. • Support alpha blending algorithm for transparent effect • Different language support

Industry Camera Solution



MIPI FPGA Industry Camera Solution

- Most of the main controller platform can support sensor with LVDS interface, but can't support MIPI CSI-2 interface
- MIPI FPGA can help to convert MIPI CSI-2 interface into LVDS interface, using MIPI D-PHY hard IP for MIPI receiver, FPGA logic to do CSI-2 decoder and send out data through LVDS interface. It also has the capability to do data reassembly for customized function

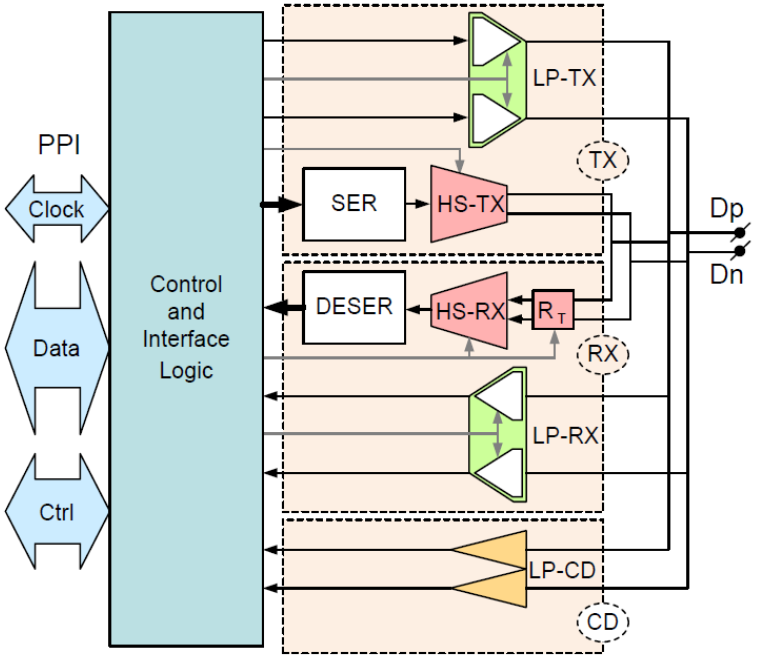


HME-H1D03 in China

- H1D03 is a SoC chip, with MCU inside which provides added benefits:
  - Easy to interface with other device with general interface like SPI/I2C/UART without using extra FPGA logic resource
  - More convenient to configure MIPI D-PHY and MIPI DSI/MIPI CSI-2 controller related registers
  - Suitable for system and power management. MCU support different low power mode, it can also do clock management for MIPI and FPGA's different logic resource
- At the 2020 China IC Design Achievement Award Ceremony (2020年度中国IC设计成就奖颁奖典礼), HME earned the coveted award for “Best FPGA/Processor of the Year”

Mixel MIPI IP Integrated in HME-H1D03

- 2 instances of 4-Lane MIPI D-PHY Universal IP
- Can be configured as transmitter or receiver MIPI D-PHY IP
- Supports MIPI D-PHY v1.1
- Supports MIPI CSI-2 and MIPI DSI/MIPI DSI-2 protocols
- High-speed transmit and receive at 1.5Gbps/lane
- Low-power transmit and receive up to 10Mbps/lane
- Achieved first time silicon success



Mixel MIPI D-PHY Universal IP

Conclusion

- MIPI applications has substantially expanded from Mobile to Mobile and Beyond
- MIPI CSI-2 and MIPI DSI-2 are de-facto protocols for low-power sensor and display systems
- MIPI-based FPGA are useful not only for developing a proof-of-concept, but are also used in consumer and industrial products, reducing time-to-market and development cost
- HME's award-winning product, H1D03 FPGA, integrating Mixel IP demonstrates the wide adoption of MIPI PHY subsystems in MIPI CSI-2 and MIPI DSI applications

Demo

- [Video of demo]

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THANK YOU!

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Q&A