mipi DEVCON
MIPI ALLIANCE DEVELOPERS CONFERENCE

20-21 SEPTEMBER 2022

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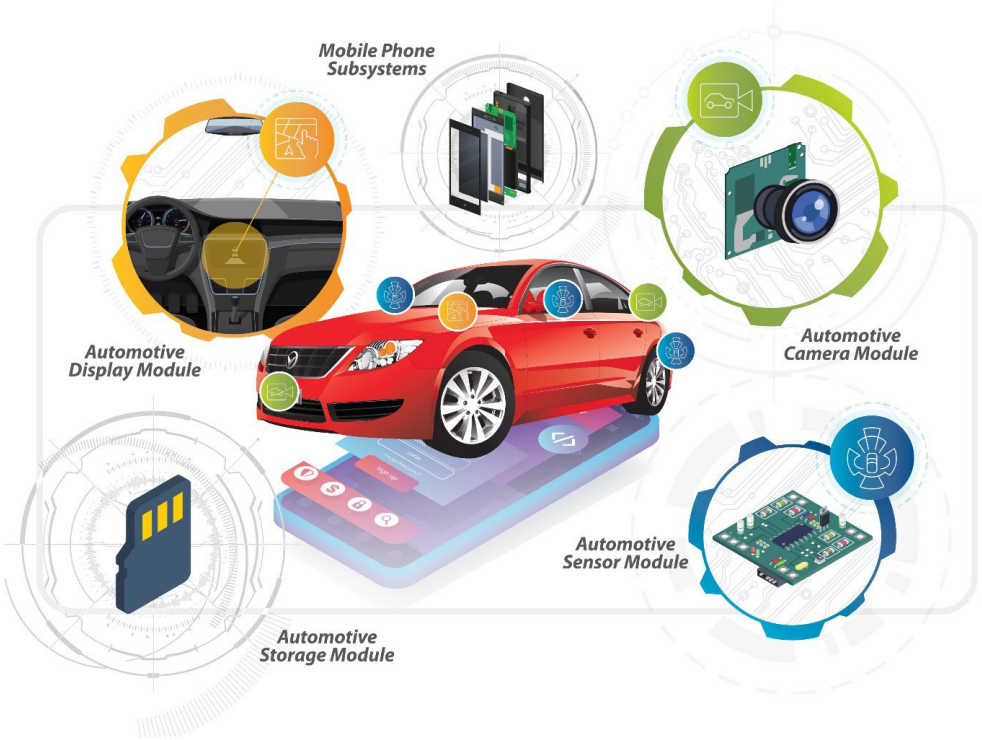
MIPI® Sensor Solutions for Autonomous Driving

Agenda

- Introduction
- Sensors
- Safety
- Summary

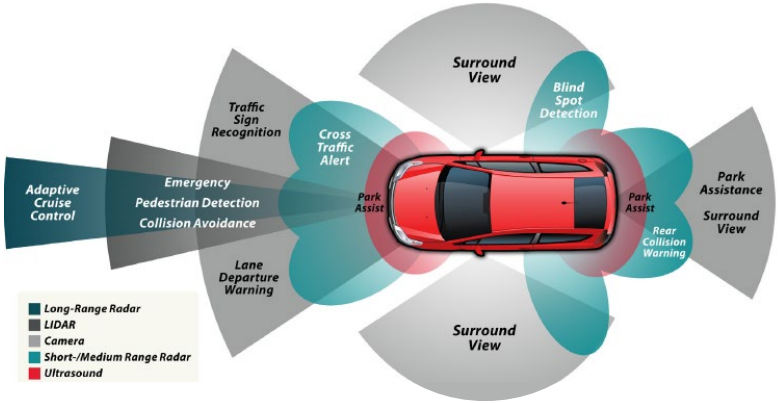
MIPI in Automotive



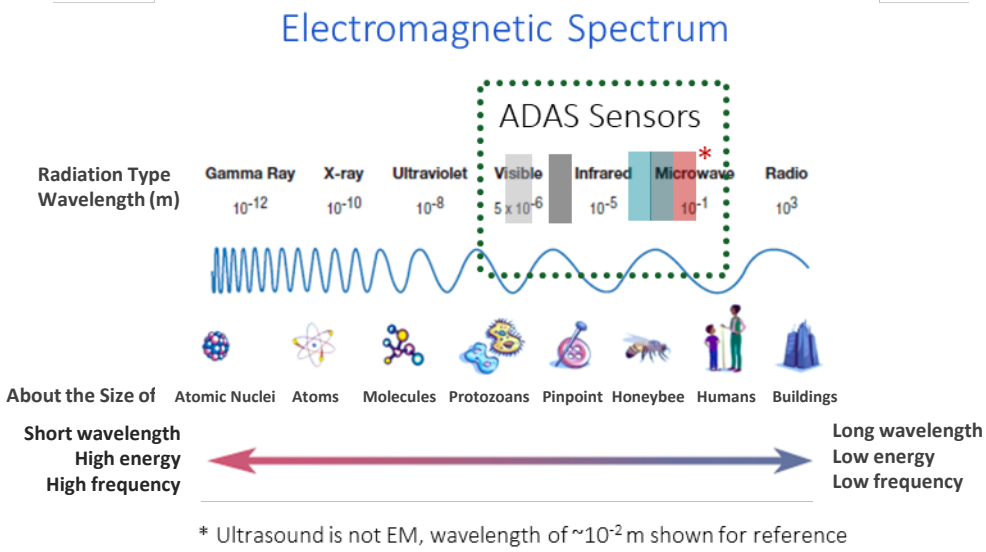
- Auto industry is being transformed by global trends
  - Growing embrace of electric vehicles
  - Increasing vehicle automation
  - Tighter safety
  - Fuel economy standards
- Automotive industry is now leveraging the mobile smartphone technology
  - High-resolution dashboard displays connected to back-up rear cameras
  - Infotainment displays with GPS navigation
  - Multi-wireless Bluetooth, Wi-Fi and 4G/5G cellular connections
  - Advanced Driver Assistance Systems (ADAS)
  - Voice recognition + voice commands

Automotive Sensor Market

- The automotive sensor market is rapidly growing due to the adoption of Advanced Driver Assist Systems (ADAS)
  - Camera, Light Detection and Ranging, Radar and Ultrasound
  - Automobiles can be expected to have 8-12 sensors



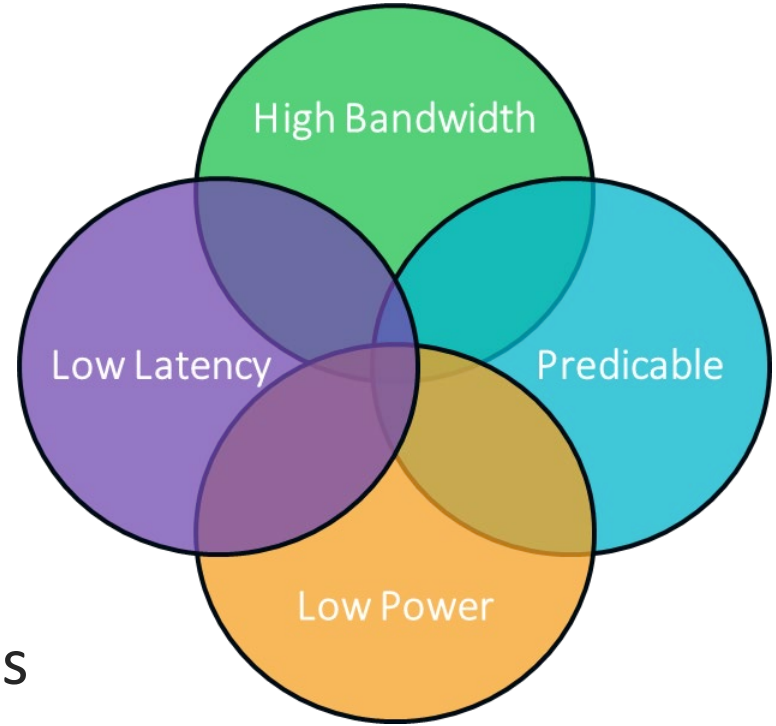
Source: MIPI Alliance White Paper Driving the Wires of Automotive



Architectures Must Balance Many Requirements To Succeed

- High Throughput
- Low Power
- Low Latency
- Continuous Streaming
  - Predictable (no buffering)
- Programable

MIPI CSI-2® Enables trade-offs based on application requirements



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Sensors

MIPI CSI-2 Specification, the Sensor Workhorse

- Each feature builds on a solid foundation
- Continual improvement
- Continual flexibility

Feature	MIPI CSI-2 Specification Version						
	v1.1	v1.2	v1.3	v2.0	v2.1	v3.0	V4.0
Basic image frame using short frame sync packets, long data packs and at least one virtual channel and a MIPI PHY							
D-PHY reference	v1.1	v1.2	v1.2	v2.1	v2.1	v2.5	V3.0
C-PHY reference			v1.0	v1.2	v1.2	v2.0	v2.1
Limit on data lanes per D- or C-PHY serial link	4	none	none	none	none	none	none
I2C							
Generic user-defined, long packets (4 data types)							
Short Packet Data Types							
Long Packet Data Types							
Additional RAW pixel data types				16,20	16,20	16,20,24	16,20,24, 28
Generic user-defined, long packets (4 data types)							
DPCM compression 10-{8,6,7}-10 and 12-{8,7,6}-12							
DPCM compression 12-10-12							
Virtual channel and data type long packet interleaving							
Maximum number of virtual channels (D-/C-PHY)	4/-	4/-	4/4	16/32	16/32	16/32	16/32
Latency Reduction and Transport Efficiency (LRTE)							
LRTE with End-of-Transmission short packets (EoTp)							
Long packet data scrambling							
Smart Region of Interest (SROI)							
Universal Serial Link (USL)							
Always-On Sentinel Conduit (AOSC)							
Multi-Pixel Compression (MPC)							

MIPI D-PHY and MIPI C-PHY

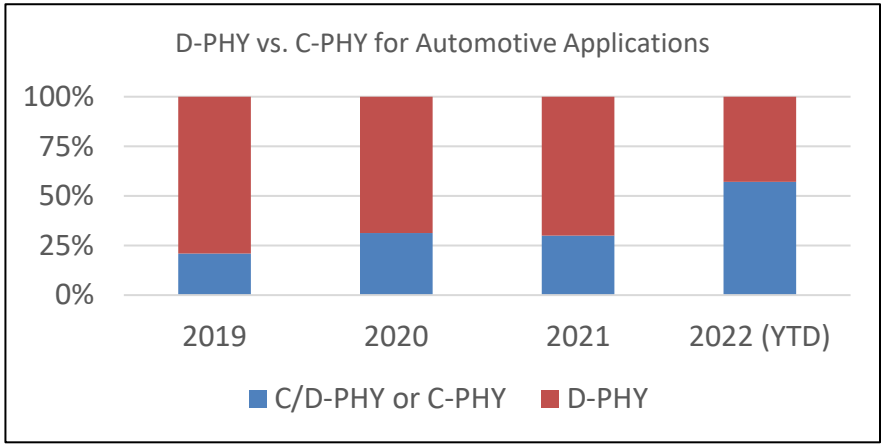
- D-PHY℠ and C-PHY℠ are the foundation of low power architecture
- Multiple generations with increasing speeds and additional features
  - Some features add **power savings**
  - Other features for **IoT applications** requiring long channel, reduce # of wires

Feature	MIPI D-PHY Specification						
	V1.0	V1.1	V1.2	V2.0	V2.1	V2.5	V3.0
Maximum Speed (Standard Channel)	1.0Gbps	1.5Gbps	2.5Gbps	4.5Gbps			9.0Gbps (Standard Channel)
Deskew Calibration							
HS-TX Halfswing HS-RX unterminated							
ALP Mode							
Fast Bus Turnaround							

Feature	MIPI C-PHY Specification					
	V1.0	V1.1	V1.2	V2.0	V2.1	V3.0 (TBD)
Maximum Speed (Standard Channel)	1.7Gsps	2.8Gsps	3.5Gsps	6.0Gsps	6.0Gsps	5.0Gsps (4 Bits/Sym)
LVHS TX HS-RX unterminated						
ALP Mode						
Fast Bus Turnaround						

MIPI D-PHY and MIPI C-PHY in Automotive Applications

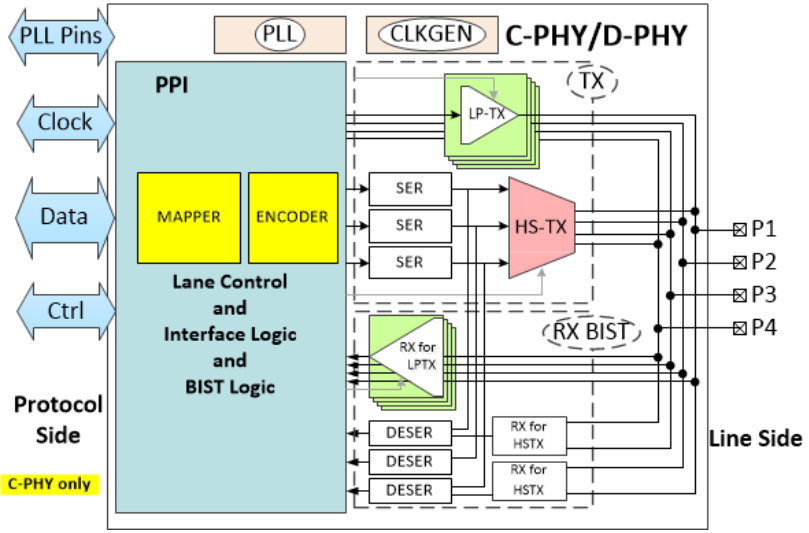
- MIPI D-PHY has been traditionally used when MIPI CSI-2 is needed for automotive applications, having been around for many more years
- MIPI C-PHY initial gained traction in consumer applications
- Increasing use of MIPI C-PHY for automotive applications (primarily for MIPI CSI-2)
- Seeing increasing use of MIPI for “mission critical applications”



Source: Mixel, Inc.

MIPI PHY Solution for Automotive Application

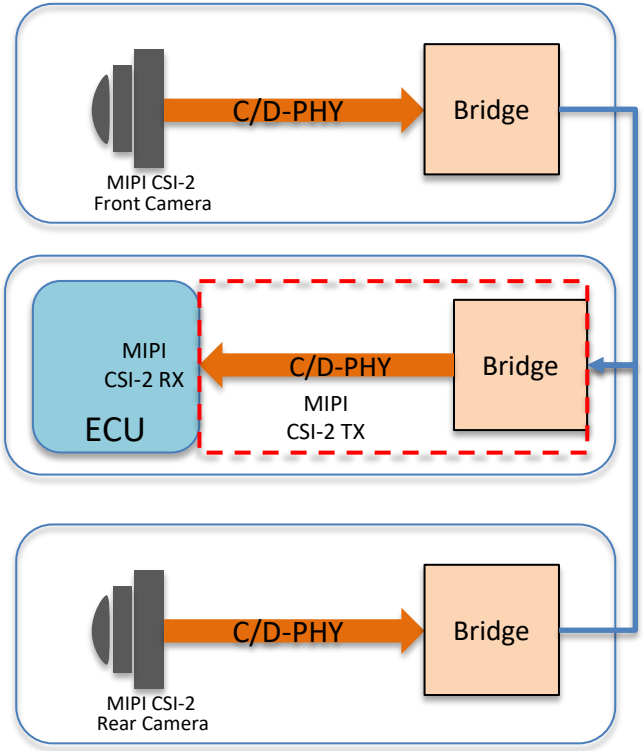
- In automotive applications, testability is essential. MIPI IP may require:
  - In system testability
    - Universal configuration supports loopback and full-speed production testing.
    - Mixel created RX+ and TX+ configurations based on automotive customers' request for in-system, production testing with minimal area penalty
  - For mission critical applications, design for higher sigma and higher junction temperature
  - Design to automotive PDK from foundry
- Additional testing and verification required for automotive IP:
  - Stress test (e.g., voltage stress) with ability to screen out latent defects during testing
  - HTOL to ensure lifetime requirement
  - Reliability simulation
    - Ageing
    - EMIR



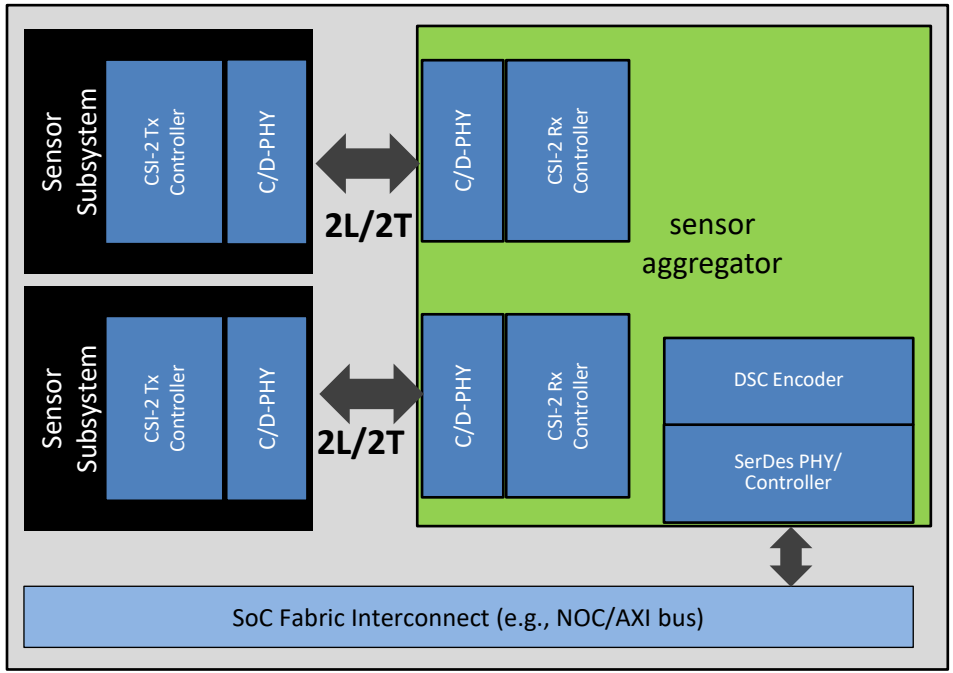
CSI-2 TX+ CD-PHY

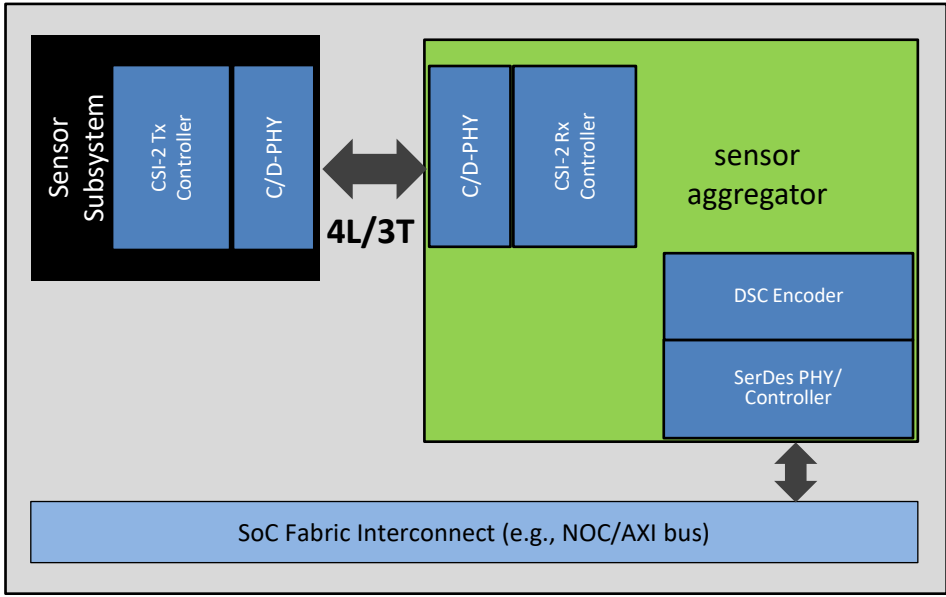
Automotive Sensor Subsystem Architecture

- Design a sensor aggregator chip on ECU side
  - ECU support 1 or 2 sensors
    - System configurable
  - Sensors
    - One high lane rate
    - Two mid-range lane rate
- How can MIPI C/D-PHY support this with MIPI CSI-2 controller?



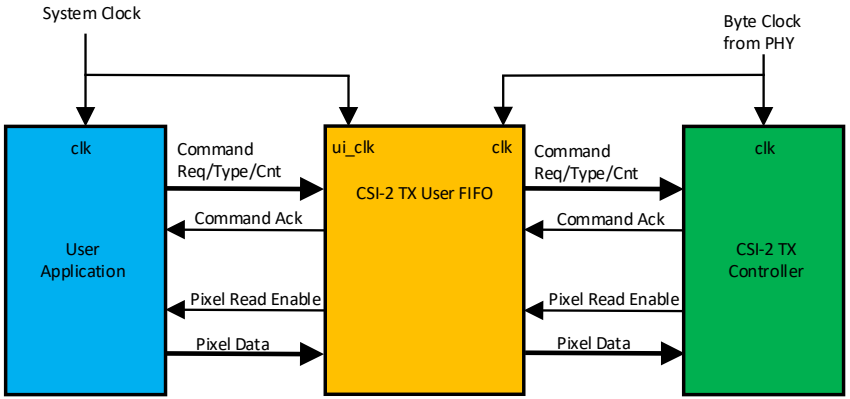
Software Configurable Sensor Aggregator Solution





Bandwidth Matching: User FIFO Overview

- Main purpose is to handle cases where the User Application clock does not match the CSI-2 Tx Controller Clock.
- The User FIFO also handles cases of pixel bandwidth differences. (16 pixels per clock into FIFO, 8 pixels per clock out).
- The User FIFO must be large enough to prevent any gaps or stalls in MIPI data during packet transfer
  - User clock is faster or slower than MIPI clock
- The User Application interface sends packet requests indicating type and pixel count. Once the User FIFO acknowledges the packet request, pixel read enable requests pixel data until pixel count is reached.



Command request include

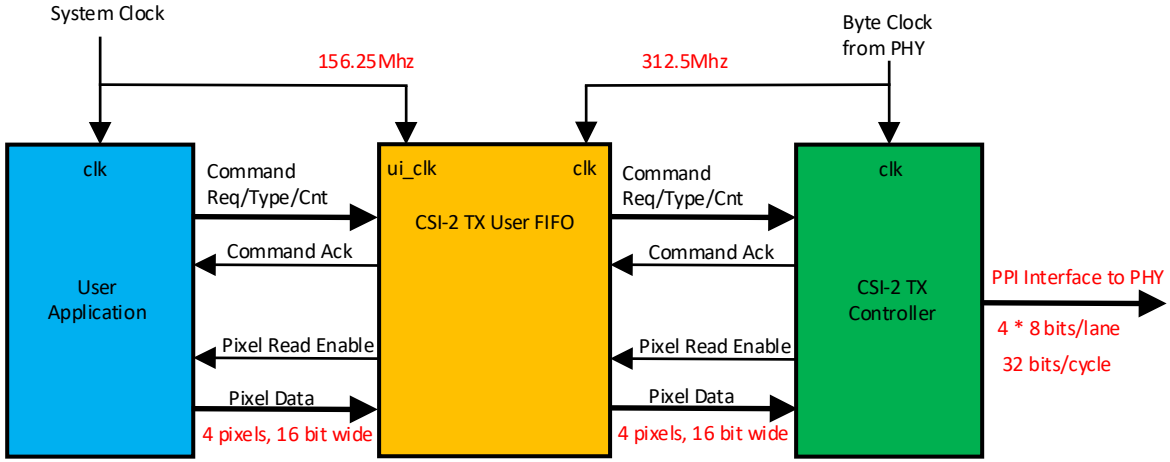
Data Type

Virtual Channel

Number of Pixels

Bandwidth Matching Example

- If MIPI bandwidth is less than User FIFO input bandwidth, then clock can be slower than MIPI clock
- For example:
  - 4 lane (32 bits/cycle) D-PHY clock to controller with controller clock at 312.5Mhz
  - Input to User FIFO is 4 pixels per clock and pixel width is 16-bit pixels
  - 4 * 16 = 64 bits to user interface each cycle User clock can run at 312.5Mhz/2 to keep up with MIPI rate



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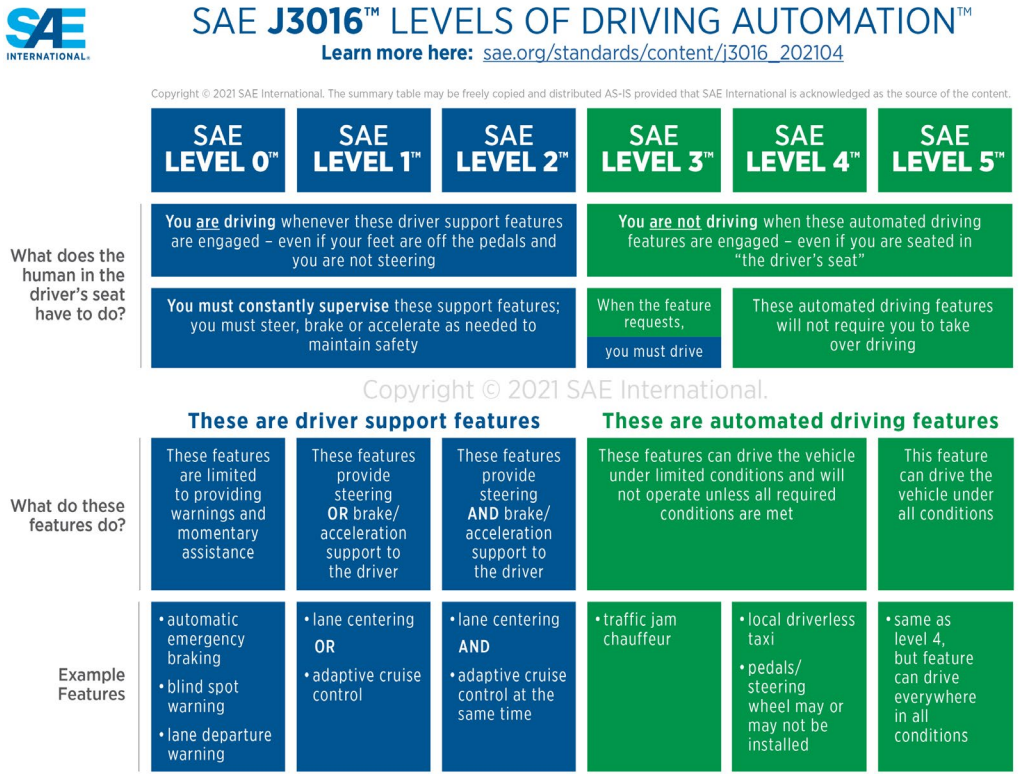
Safety

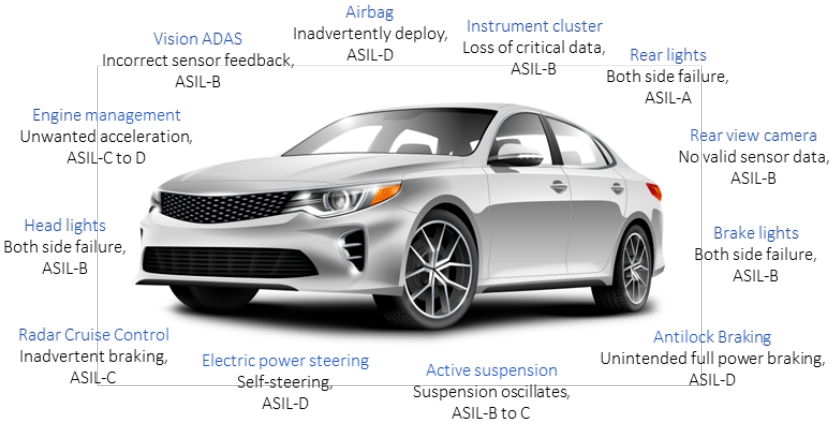
Driving Automation Levels

- Most autopilot falls under SAE Level 2, partial driving automation, which includes hands-free driving, adaptive cruise control, lane change, etc.
- While Level 2 and higher are often talked about, SAE Level 0 and SAE Level 1 also include features that require advanced sensors and cameras such as:
  - Forward Collision Warning (FCW)
  - Automatic Emergency Braking (AEC)
  - Blind sport warning
  - Lane departure warning



ISO26262 Automotive Functional Safety Standard

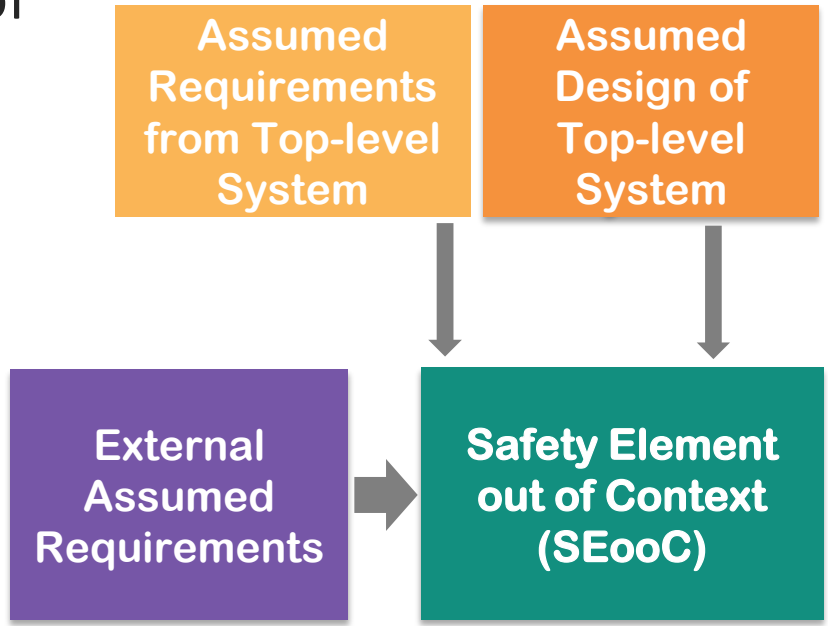
Severity class		Probability class	Controllability class C1	C2	C3
	S1	E1	QM	QM	QM
		E2	QM	QM	QM
		E3	QM	QM	A
		E4	QM	A	B
	S2	E1	QM	QM	QM
		E2	QM	QM	A
		E3	QM	A	B
		E4	A	B	C
	S3	E1	QM	QM	A
		E2	QM	A	B
		E3	A	B	C
		E4	B	C	D



- ASIL Ratings go from Quality Management (QM) then ASIL-A to ASIL-D
- ASIL-C and ASIL-D are considered “high-level safety critical”
- Rating is determined by 3 parameters: Colors correspond to QM (Green), ASIL-A (Yellow) through ASID-D (Dark peach)
  1. Exposure (E): probability of vehicle being in risky situation that causes damage to person or property (E1 is lowest, E4 is highest)
  2. Controllability (C): extent driver can take control of vehicle (C1 is easy to control, C3 is difficult to control)
  3. Severity (S): seriousness or intensity of damage or consequences to life of people (S1 is light/moderate injury to S3 is life threatening)

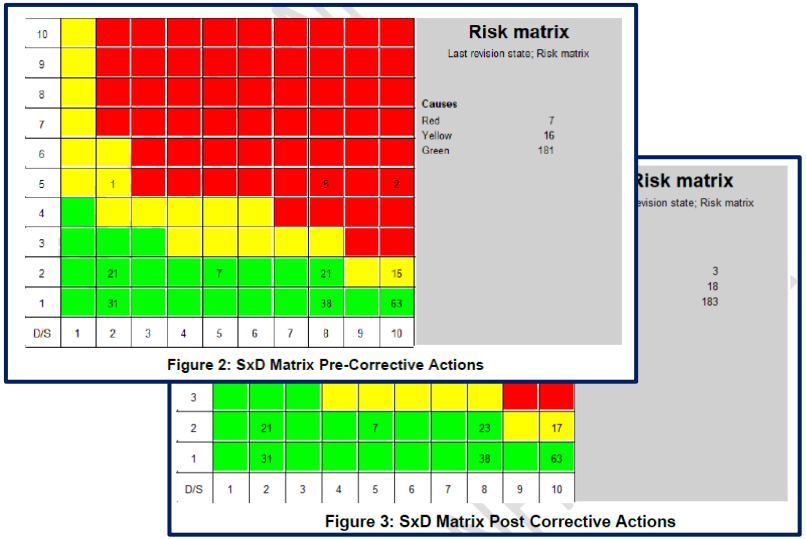
Safety Element out of Context (SEooC)

- IP vendor has no prior knowledge of system
- Safety Manual to cover
  - Assumptions on Safety Functions
  - Assumptions of Use (AoU)
    - Target ASIL
    - Operating Conditions for PHY
  - Safety Mechanisms
    - Internal
    - External
  - Safety lifecycle of the IP



Hardware Safety Analyses

Design failure mode and effect analysis (DFMEA)



DFMEA is used for systematic failure analysis

Failure modes, effects, and diagnostic analysis (FMEDA)

No.	Block / Subblock (unique name)	Block / Component	Failure Rate *Permanent* λ [FIT]	Failure Rate *Transient* $\lambda_{transient}$ [FIT]	Failure Rate Distribution *Permanent*	Failure Rate Distribution *Transient*
1	D-LANE	Mixed Signal Module (MSM)	0.229793	10.927278	37.09%	39.48%
2	C-LANE	Mixed Signal Module (MSM)	0.052690	2.457030	8.50%	8.88%
3	Common MSM Blocks	Mixed Signal Module (MSM)	0.039728	3.633763	6.41%	13.13%
4	PLL	Mixed Signal Module (MSM)	0.120189	5.101928	19.40%	18.43%
5	IO Pad Ring	Mixed Signal Module (MSM)	0.135088	1.350884	21.80%	4.88%
6	dphy clock master	CIL-TOP	0.001493	0.149260	0.24%	0.54%
7	dphy clock slave (BIST)	CIL-TOP	0.000501	0.050109	0.08%	0.18%
8	dphy data master	CIL-TOP	0.009383	0.938207	1.51%	3.39%
9	dphy data slave (BIST)	CIL-TOP	0.012794	1.279374	2.07%	4.62%
10	test mode block (BIST)	CIL-TOP	0.017059	1.705831	2.75%	6.16%
11	ulps pll control	CIL-TOP	0.000384	0.038381	0.06%	0.14%
12	Control Common MSM blocks	CIL-TOP	0.000426	0.042646	0.07%	0.15%
13	Lane Alignment Logic	CIL-TOP	0.000019	0.002132	0.00%	0.01%

FMEDA is used to analyze hardware IP random faults

CSI-2 Controller Safety BIST For Autonomous Driving

- CSI-2 Controller Safety Targeted BIST
  - Concentrates on fault detection mechanisms
  - Tests ECC, CRC, parity and other safety mechanisms on power up
  - Can be trigged by system software/firmware for period testing during operation
- Advantages over system level BIST
  - Deeper test of error detection mechanisms
  - Always run even if BIST is not done at a higher level
  - Creates an early confirmation that IP is functional
  - Provides confidence that safety mechanisms are functional
  - Provides a guaranteed level of safety coverage that system BIST may not provide

BIST does not replace SOC testing:

Interfaces are not targeted for application specific traffic patterns

CSI-2 Controller Protection and Safety Watchdog

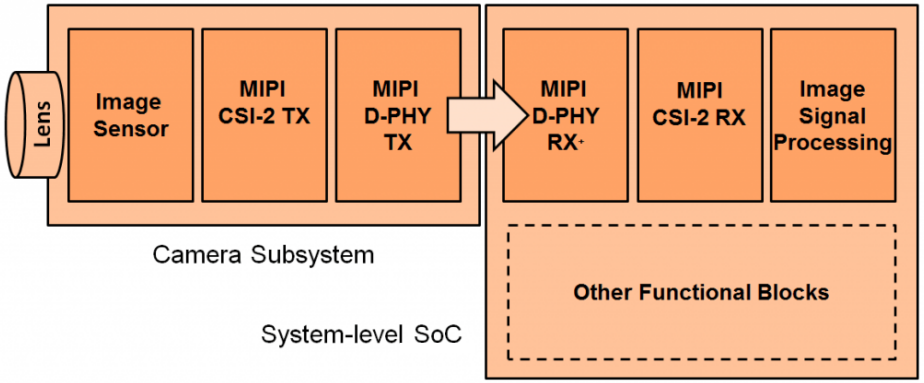
- Data Protection
  - Parity protection on pixels and pixel buffers
  - MIPI protocol header ECC and packet data CRC
- Critical Logic Protection Through Redundancy
  - Data Formatting, Packing Logic, critical state machines
  - Critical logic blocks compare duplicate outputs
- Data Order Protection
  - Packet number field in user interface FIFO stores packet numbers
  - Internal error triggered on nonsequential packet numbers
- Watchdog
  - Area/Power efficient way to detect faults that stop the Controller from making forward progress
  - Follows a sequence of input and output signals and checks internal signals

CSI-2 Controller Fault Recovery

- Detection Reporting to System
  - IRQ on error back to the system
- Fault Recovery
  - Support soft reset of all state machines and critical logic
- Methodology
  - CSI-2 Controller assert IRQ on error
  - System software/firmware reads error status enables
    - Soft reset only the Rambus CSI-2 Controller
    - Soft reset entire system
    - Hard reset entire system
- System software/firmware can also execute BIST before beginning sending/receiving real packets

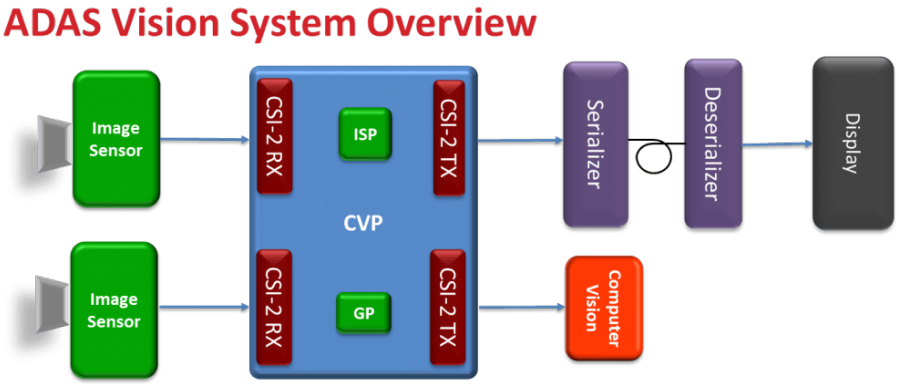
Customer Use Case: NXP Camera-to-Processor Connection

- Camera sub-assembly has the camera sensor and supporting circuitry for image capture and for organizing the image data for transmission using a D-PHY Tx macro
- Camera image is serialized and sent across to an Image Signal Processing sub-assembly containing the supporting circuitry for receiving the data – a D-PHY Rx macro
- Physical connection between the Tx and Rx side is made using a MIPI interface
- Mixel provided MIPI D-PHY with Rambus CSI-2 controller to NXP for this application



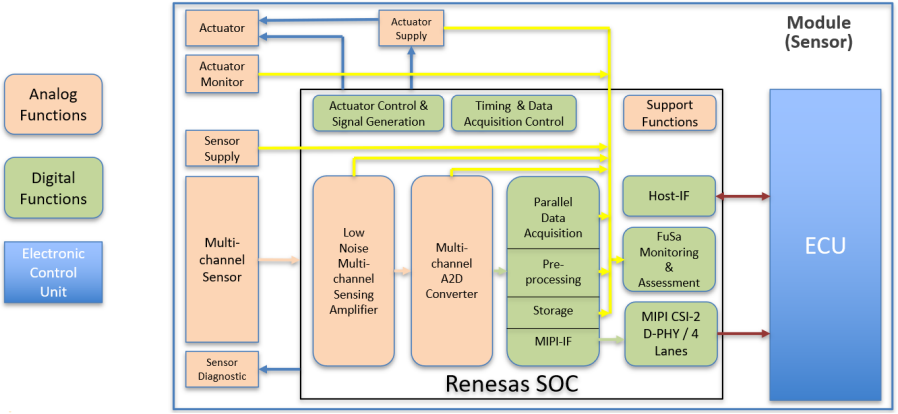
Customer Use Case: GEO GW5 ADAS Vision

- ADAS uses CSI-2 as communication link between the sensors and CVP
  - CVP drives processed video through a MIPI CSI-2 TX interface to an automotive SerDes link, which drives a high-resolution display through MIPI D-PHY based DSI interface
  - For computer vision applications, the unprocessed high-resolution video is transmitted from a CVP to a computer vision processor through another pair of MIPI CSI-2 TX/RX interfaces.
- Data sent over MIPI D-PHY physical layer
- GEO GW3 and GEO GW4 also used Mixel MIPI D-PHY with Rambus CSI-2 controller



Customer Use Case: Renesas (IDT) Automotive SoC

- Multi-channel sensor interface w/ parallel channel acquisition
  - Data acquisition control operating at hundreds of MHz
  - Actuator control and signal generation using GHz time base (supports cm level resolution)
- CSI-2 Tx 4 Lane D-PHY @2.5GBs/lane
  - Up to 10Gbps to HOST-ECU
  - Tx FIFO for bandwidth matching
- Safety Requirements
  - AEC-Q100 Auto grade 1, supporting Tj=150°C
  - ISO26262 ASIL-B supported by
    - Internal safety mechanisms for data path, configuration, and supply monitoring
    - External safety mechanisms for module level data path and supply monitoring



Summary

- MIPI was designed from the ground up for low-power applications and as a result, MIPI CSI-2 has become the de facto standard for automotive camera and sensors
- Cars require increasing number of sensors as automotive features progress from Level 0 to Level 3 and higher
- MIPI PHY and MIPI CSI-2 targeted to automotive applications need to support many testability features, including in-system testing
- By leveraging ASIL-B Functional Safety deliverables and/or ASIL-B certified IP, automotive SoC designers can target higher ASIL levels for their product, essential for mission critical applications

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Q&A