



MIPI ALLIANCE DEVELOPERS  
CONFERENCE

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**Advanced Micro Devices, Inc./Xilinx Inc.**

**MIPI Sensor System-Interop and  
Debug for Vision Applications  
on a SOM**

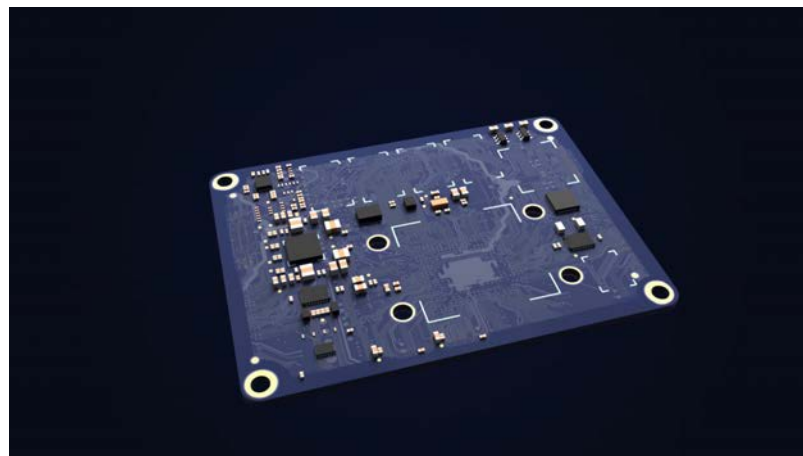
20-21  
SEPTEMBER  
2022

# Agenda

- Introduction to SOM
- SOM market & projections
- Vision applications: Concept to production with SOM
- Accelerated applications
- System level challenges
- Q&A

# What's a System-on-Module (SOM)?

- Alternative to single board computers focused on enabling customized embedded systems
- A credit card sized module with an integrated SoC (CPU/GPU/FPGA), power, security module, & flexible I/O
- Offers more flexibility & contoured solutions
- Plugs into a carrier/base board for flexible application specific peripheral carrier card design

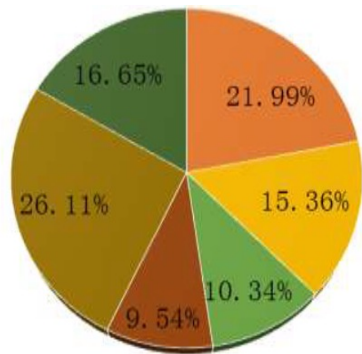


# Advantages of SOM

- Reduces effort of ground-up electronics design
- Customers start at a more evolved point vs. chip-down design
- Enables customers to build multiple products based off the same SOM platform
- SW developers to start sooner, and HW designers to finish early in the cycle.

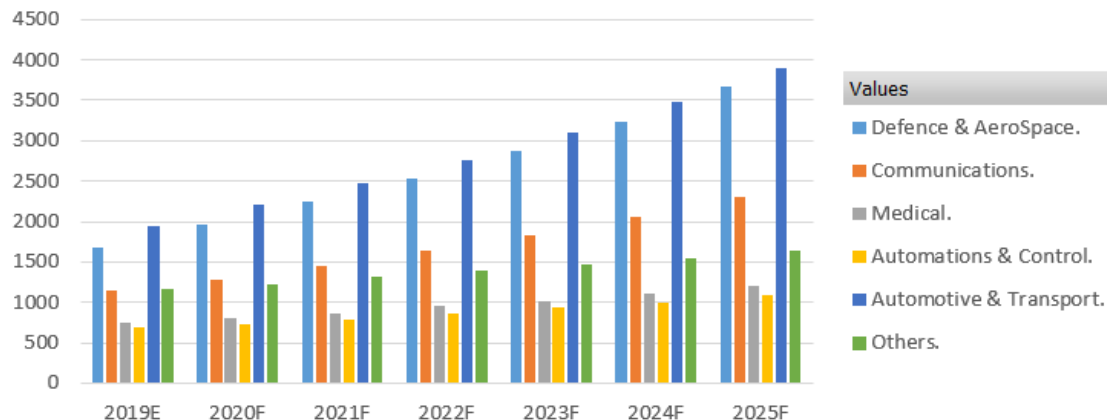
# SOM Market Size and Application

- Global SOM Sales by Application



- Defense & Aerospace
- Medical
- Automotive & Transport
- Communications
- Automations & Control
- Others

- Global SOM Sales forecast by Application



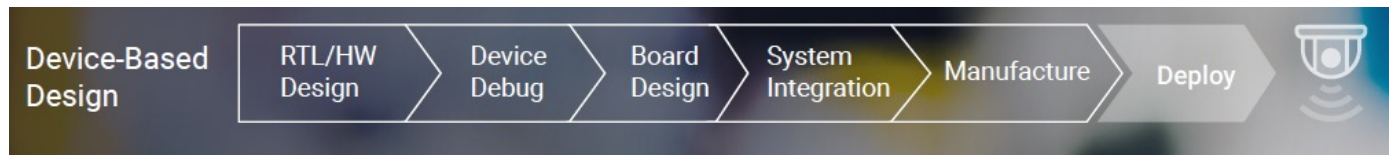
**11%**  
SOM Market CAGR

**\$2.3B**  
SOM TAM by 2025\*

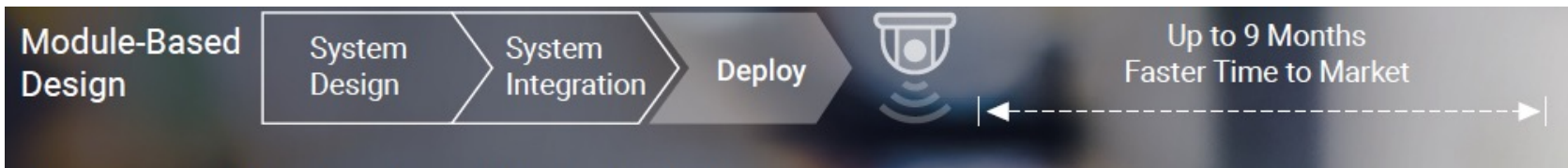
Source: Expert Interview, Secondary Sources and QYR Electronics Research Center, July 2019

# SOM: Board Level HW Abstraction

- Chip-down style
  - Evaluate & select specific device
  - Build hardware prototype & prove all functional interfaces

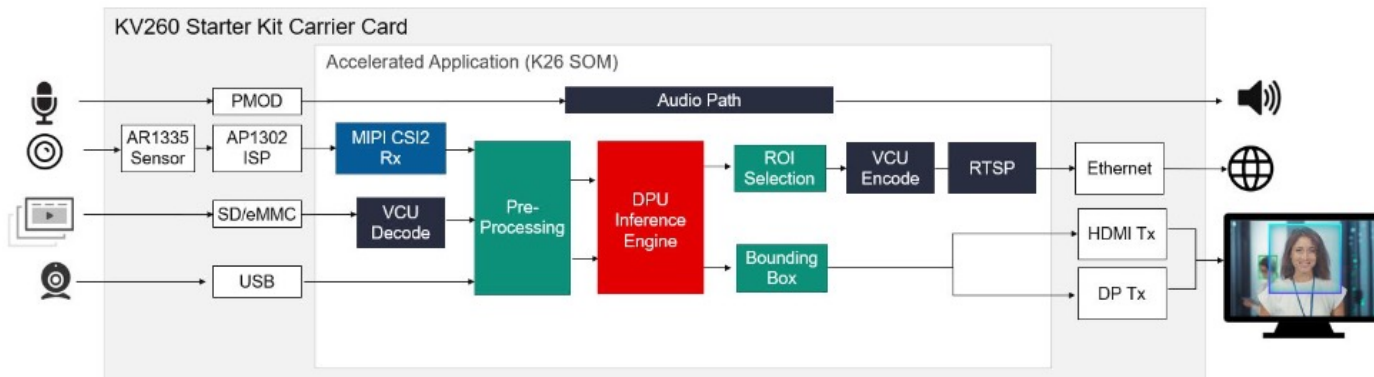


- SOM based
  - Production ready OTS board with SoC, DDR4, and multiple MIPI compliant programmable interfaces
  - SW references with FPGA based acceleration prebuilt configurations



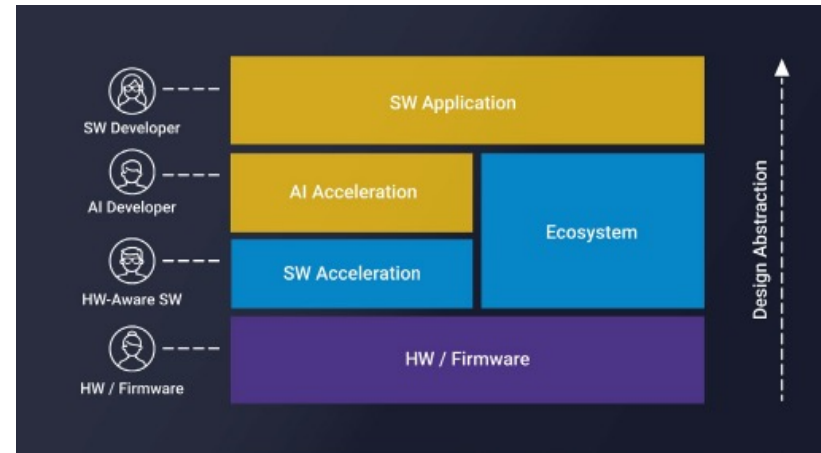
# KV260 Vision AI Starter Kit

- Provides a framework for building & customizing video platforms
  - Capture pipeline
  - Video processing pipeline
  - Acceleration pipeline
  - Output pipeline



# Kria Starter Kit Accelerated Applications

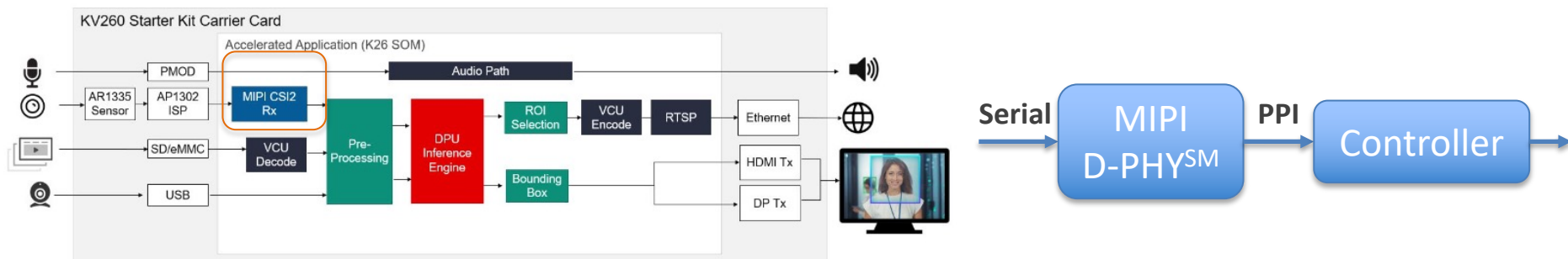
- Adaptive SOM simplifies application carrier card HW design & developer to focus on SW and AI development
- Prebuilt reference platforms , API's enable full customization of FPGA based HW & acceleration capabilities
- AMD-Xilinx tools provide mapping of ML development environments like Python, C++, TensorFlow & PyTorch to FPGA accelerated HW on SOM





# System Level Challenges

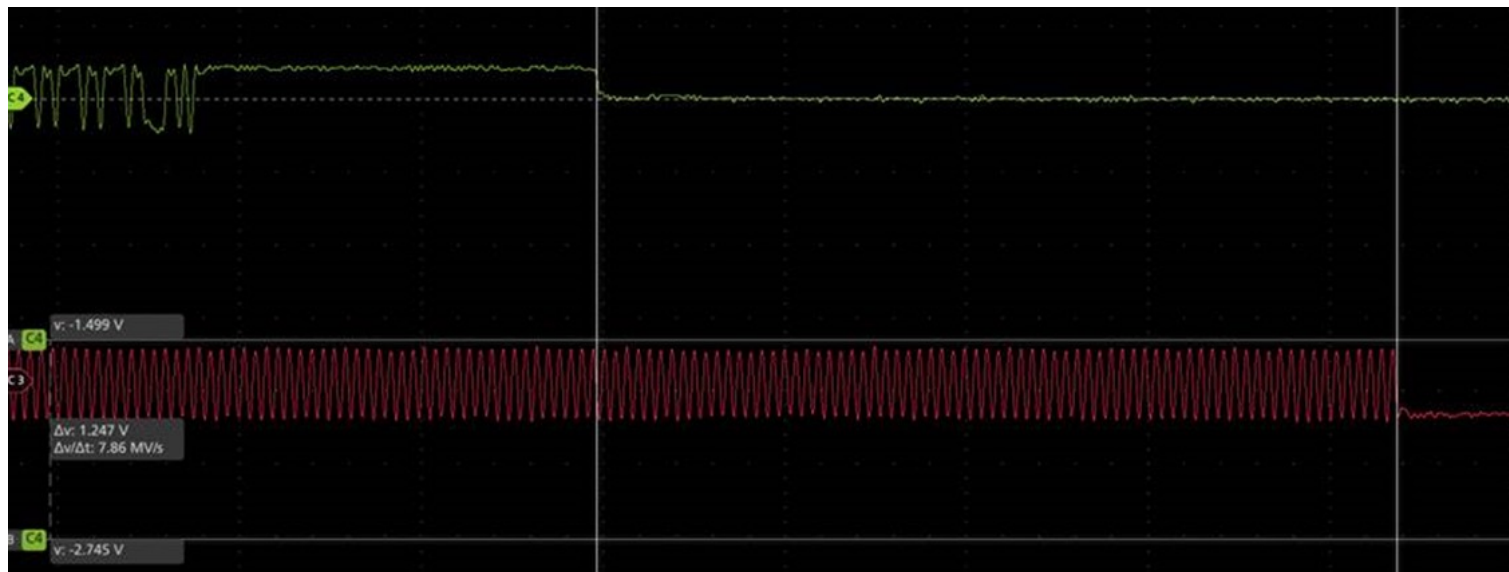
## Issue: Image freezes



- Status at Controller: No output
- Status at MIPI D-PHY<sup>SM</sup>: Receiving packets without errors

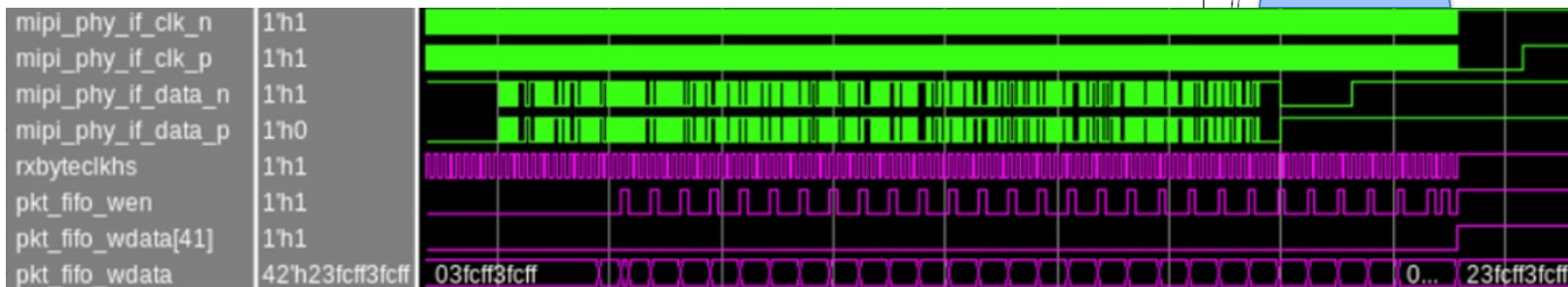
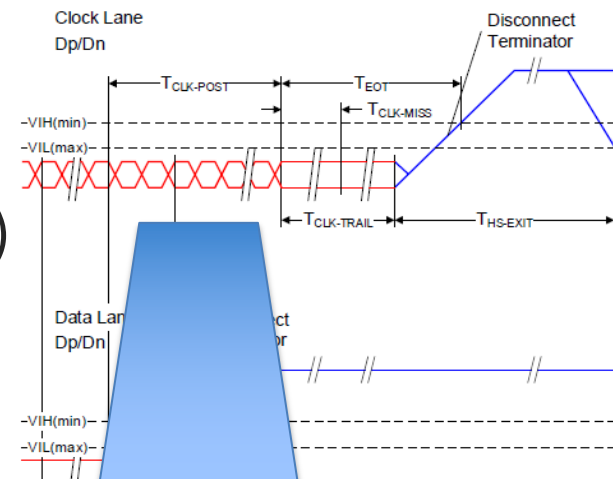
# System Level Challenge (Sensor Debug)

- Sensor output: HS <-> LP patterns looks good
  - Non-continuous clock mode



# System Level Challenge (Controller Debug)

- Debug at Controller FSM:
  - PPI data not processed fully
  - Is it due to less rxbyteclkhs? (recovered clock)



## System Level Challenges (Analysis & Solution)

- Utilized debug capabilities (ILA) in SOM FPGA PL fabric
- Analyzed sensor Tclk-post vs IP requirements
- Analyzed the system behavior and internal fabric logic for different Tclk-post settings
  - **SOLUTION**: Increasing Tclk-post setting of sensor resolved the issues
  - Batch testing PASSED
- Sensors used in SOM design: AR1335, AR0144, RPi etc.

# System Level Challenges (Other Debug Scenarios)

- Other general challenges
  - Source generate user defined data along with Pixel data
    - Impact: Image corruption
    - Solution: Downstream video pipe must demux Pixel vs user defined data type
  - Source slightly out of spec (Ex: Less Tlpx period)
    - Impact: Controller don't detect LP-HS transitions (LP-11 -> LP-01 -> LP-00)
    - Solution: Tune Tlpx of source
  - Source need more settle time before sending Sync pattern
    - Impact: Controller reports synchronization errors
    - Solution: Tune  $T_{HS-SETTLE}$  parameter of receiver

## Summary

- SOM with industry standard interfaces & communication protocols reduces development time
- SOM facilitates application and HW design with a greater degree of abstraction from chip-down designs
- SOM FPGA PL provides flexible I/O and I/O debug capabilities
- Closure of “Global timing parameters” to ease system level challenges



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THANK  
YOU!

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The logo for MIPI DEVCON. It features the word "mipi" in a lowercase, sans-serif font with a multi-colored dot matrix above the letters. Below it, the word "DEVCON" is written in a bold, uppercase, sans-serif font, with "DEV" in red and "CON" in black.

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# Q&A

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