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Cadence Design Systems

**Next Generation Verification  
Process for Automotive and  
Mobile Designs with MIPI  
CSI-2<sup>SM</sup> Interface**

MIPI ALLIANCE  
DEVELOPERS  
CONFERENCE

19 OCTOBER 2018  
**SEOUL**

# Agenda

- Typical Verification Challenges of MIPI CSI-2<sup>SM</sup> designs
- IP, Sub System and System Level Verification
- Simulation verification methodology for MIPI CSI-2<sup>SM</sup> spec compliancy
- Acceleration Methodology Overview
- Concepts for building MIPI CSI-2<sup>SM</sup> acceleration-ready environment
- MIPI CSI-2<sup>SM</sup> IP Level: From simulation to acceleration

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# MIPI CSI-2<sup>SM</sup> adoption

- Widely adopted serial high-speed protocols
- Implemented in complex systems, for a variety of applications in different markets:
  - Mobile
  - Video Games
  - Automotive
  - Multimedia
  - Virtual reality, augmented reality and others



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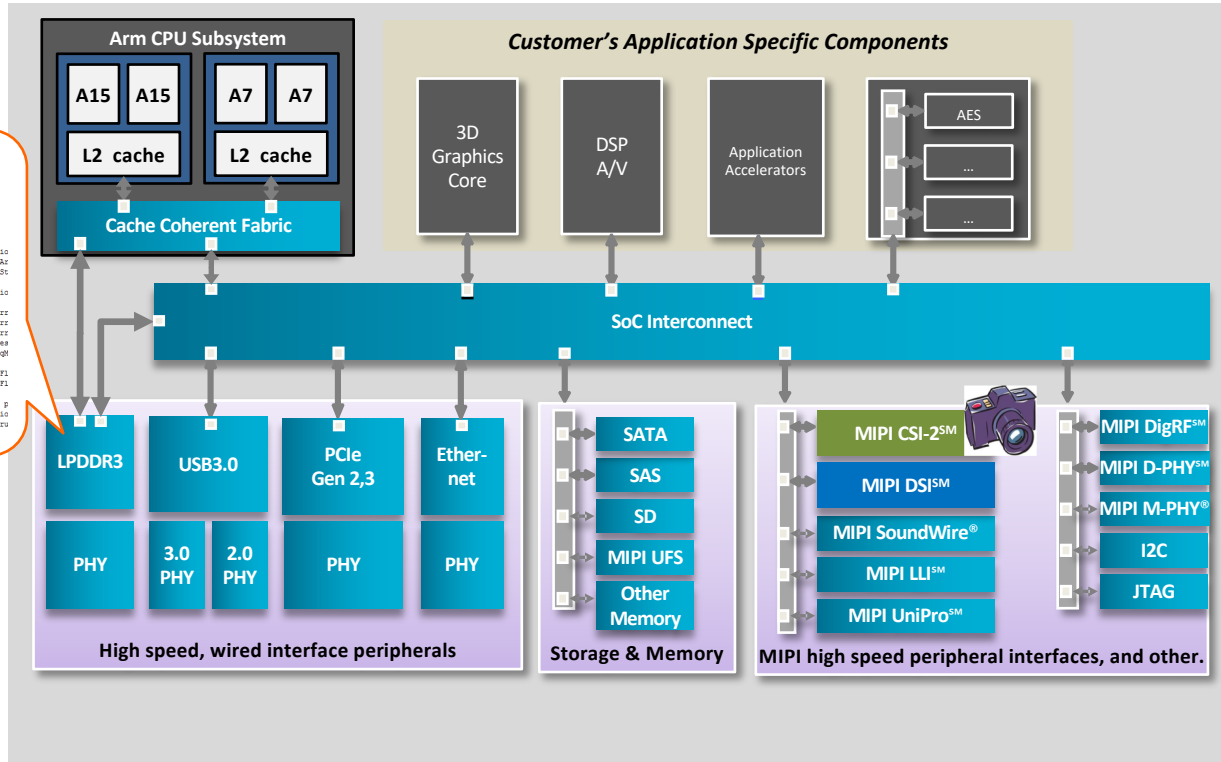
# MIPI Interfaces usage example in Complex SOCs

**Software**

```

versionStr = GetSVVer();
if (versionStr == -1) {
    return false;
} else if (versionStr == 0) {
    if (isStrEq (isOpers) {
        // Given "M20 2.0.0.11"
        tempArray = version;
        tempString = tempAr;
        versionArray = tempStr;
    } else {
        versionArray = version;
    }
}
var versionMajor = versionArr;
var versionMinor = versionArr;
var versionRevision = versionArr;
// Is the major revision > equal
if (versionMajor > parseFloat(tempI
) return true;
) else if (versionMinor == parseFl
if (versionMinor > parseFl
return true;
else if (versionMinor == p
if (versionRevisio
return tru
    
```

**Further complicated by hardware/software interactions**



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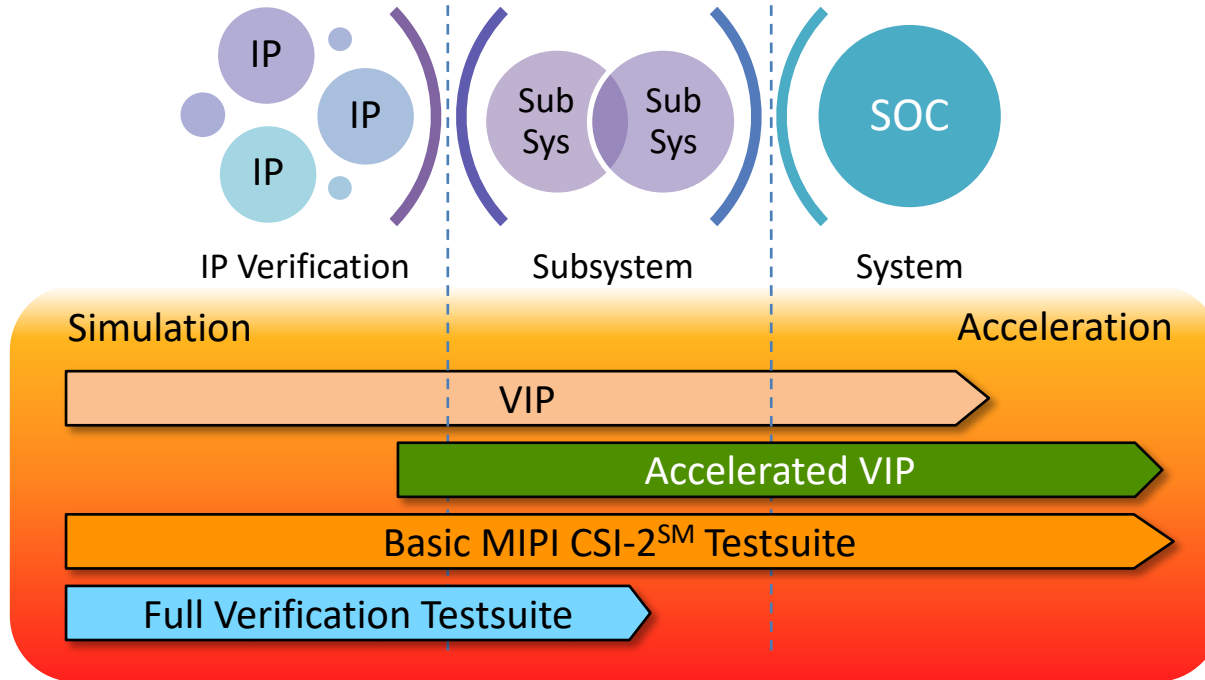


# MIPI CSI-2<sup>SM</sup> Verification Challenges

- Reach system verification coverage goals prior to code freeze
- MIPI CSI-2<sup>SM</sup> spec compliancy based on design and system configuration
- Time to market: Requires parallel development of hardware and software design, early in development cycle
- Validating software and hardware integration
- Create and validate real world scenarios in a pre-silicon environment

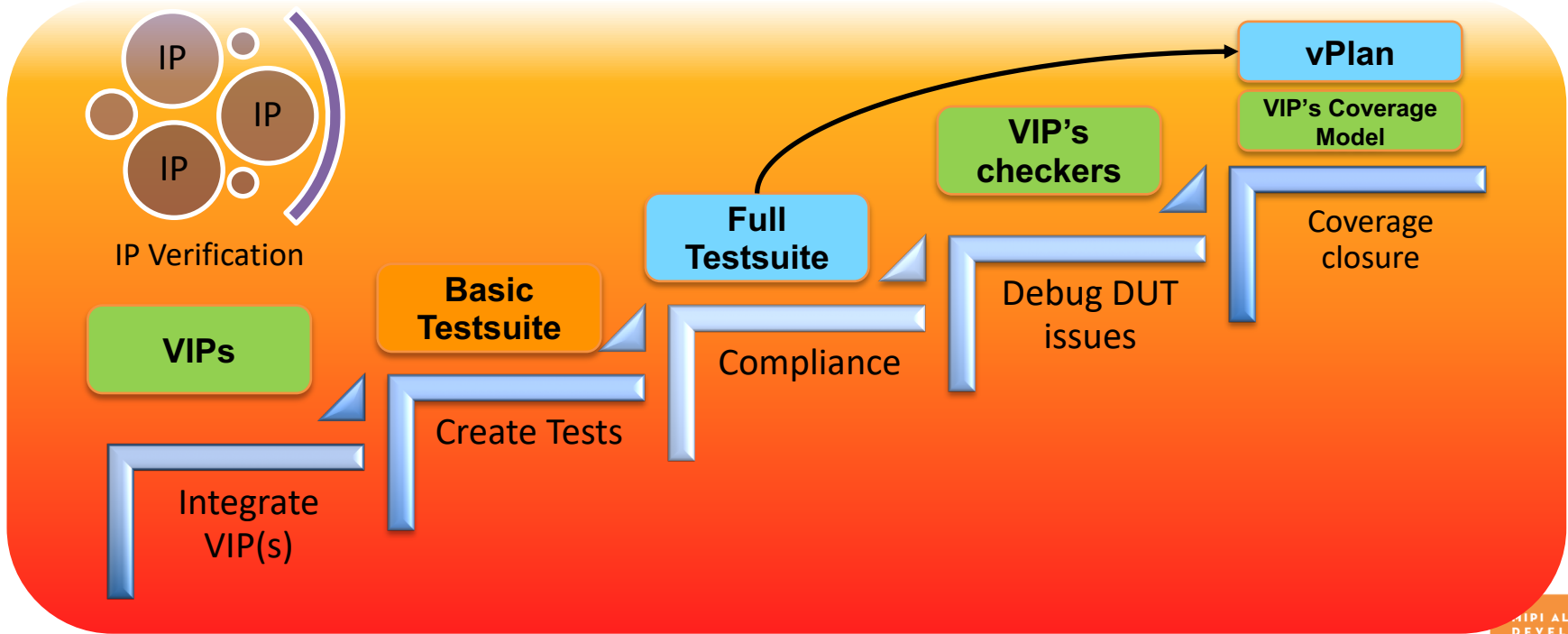
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# Design Verification Flow



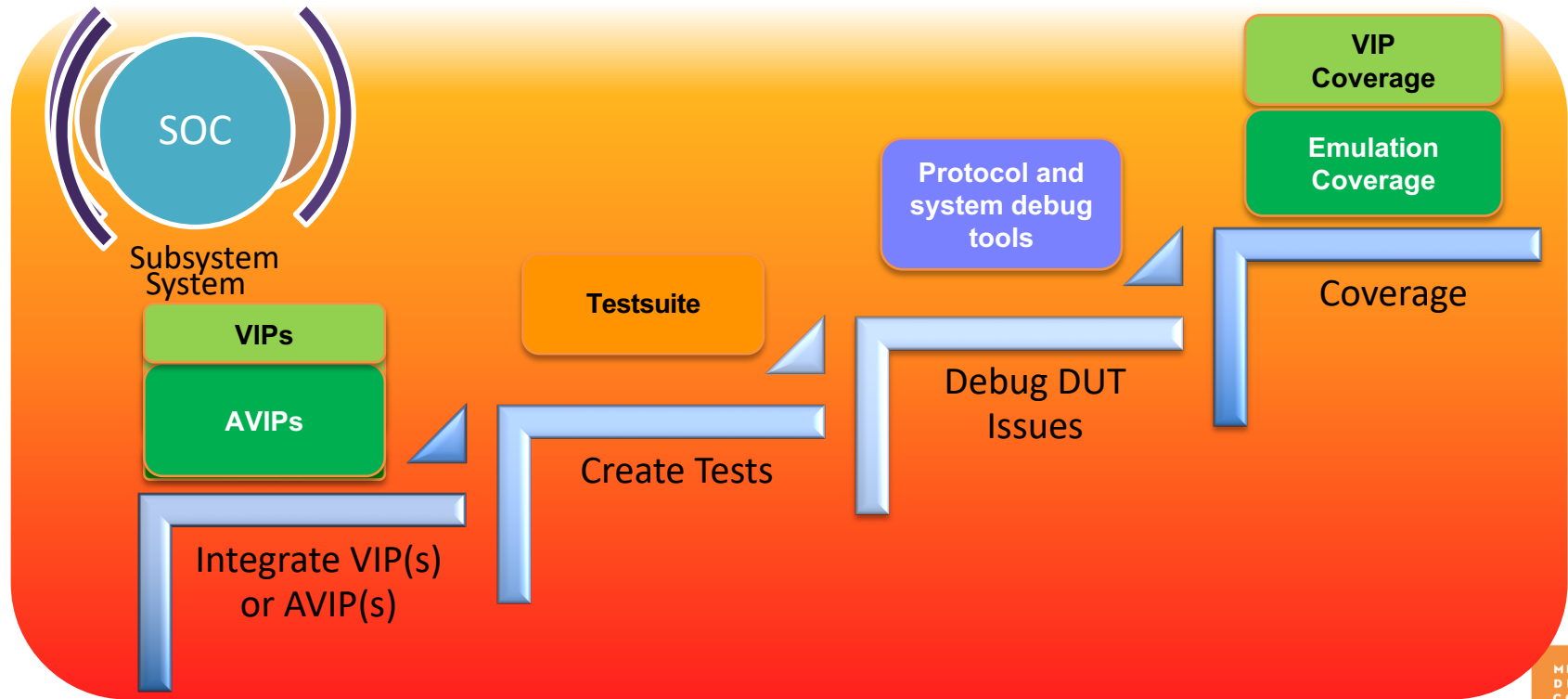
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# IP-Level Verification



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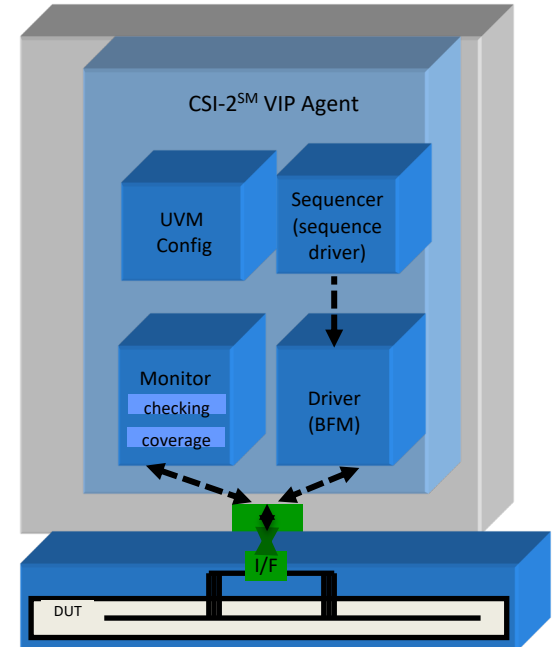
# Sub-System/SoC Level Verification



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# Verification methodology for Spec compliancy

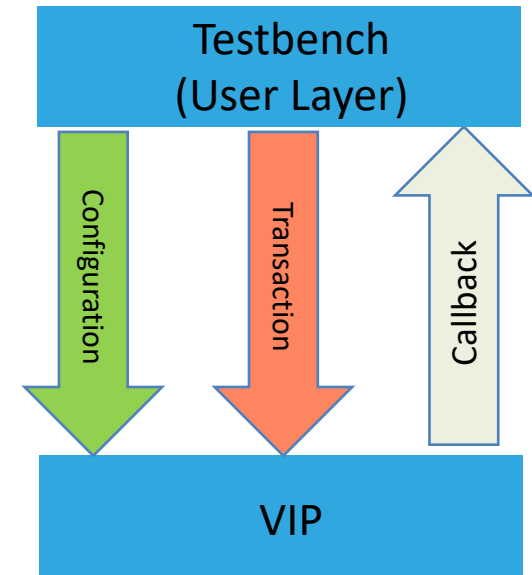
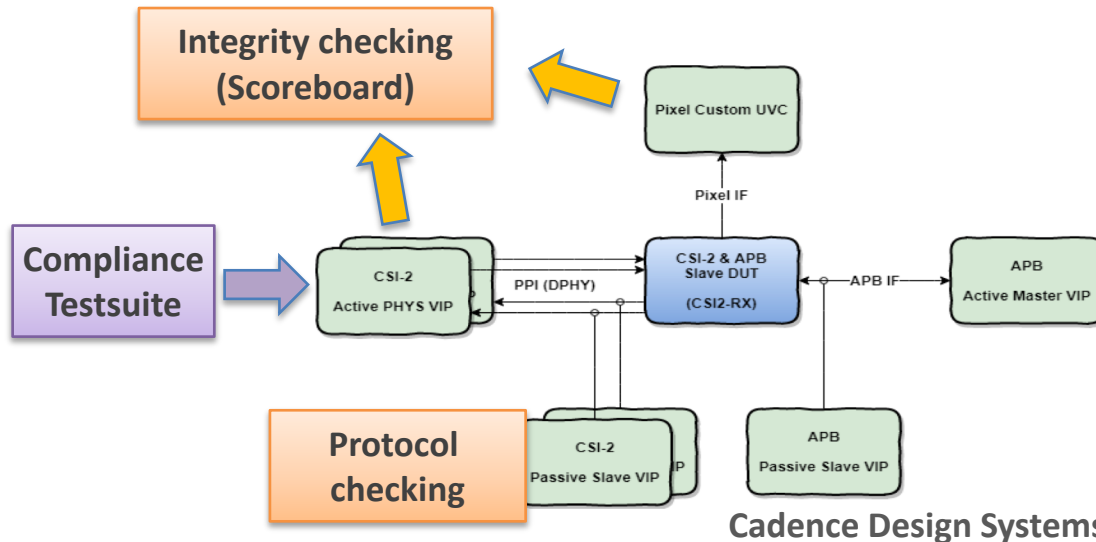
- Spec verification is based on two aspects:
  1. MIPI CSI-2<sup>SM</sup> I/F spec compliance
    - Protocol checking based on MIPI CSI-2<sup>SM</sup> spec
    - Coverage aligned to the design configuration
    - Complete Testsuite to cover MIPI CSI-2<sup>SM</sup> DUT
  2. System behavioral correctness
    - Integrity checking based on system definition



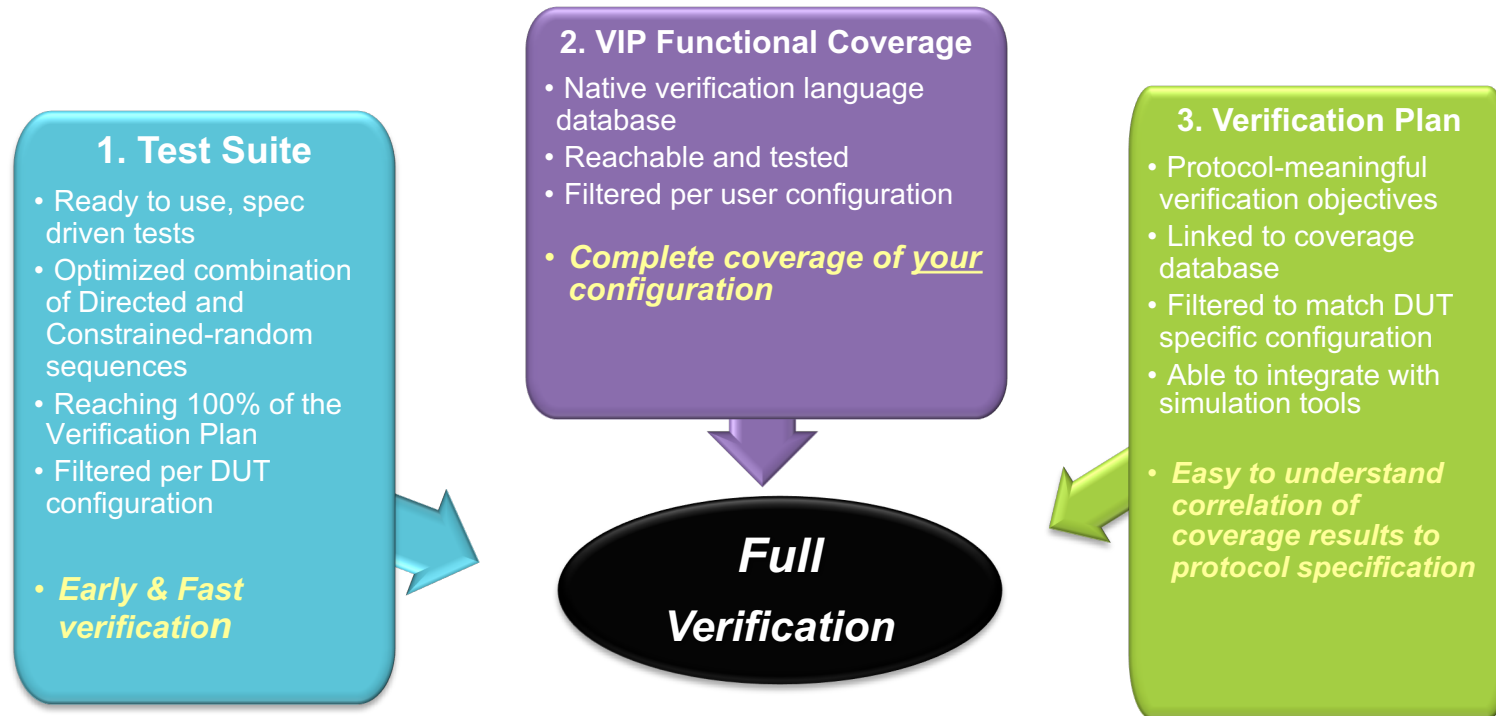
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# Verification methodology for Spec compliancy

- User needs full visibility into and controllability over VIP on Configuration, traffic injection, protocol checking and functional coverage

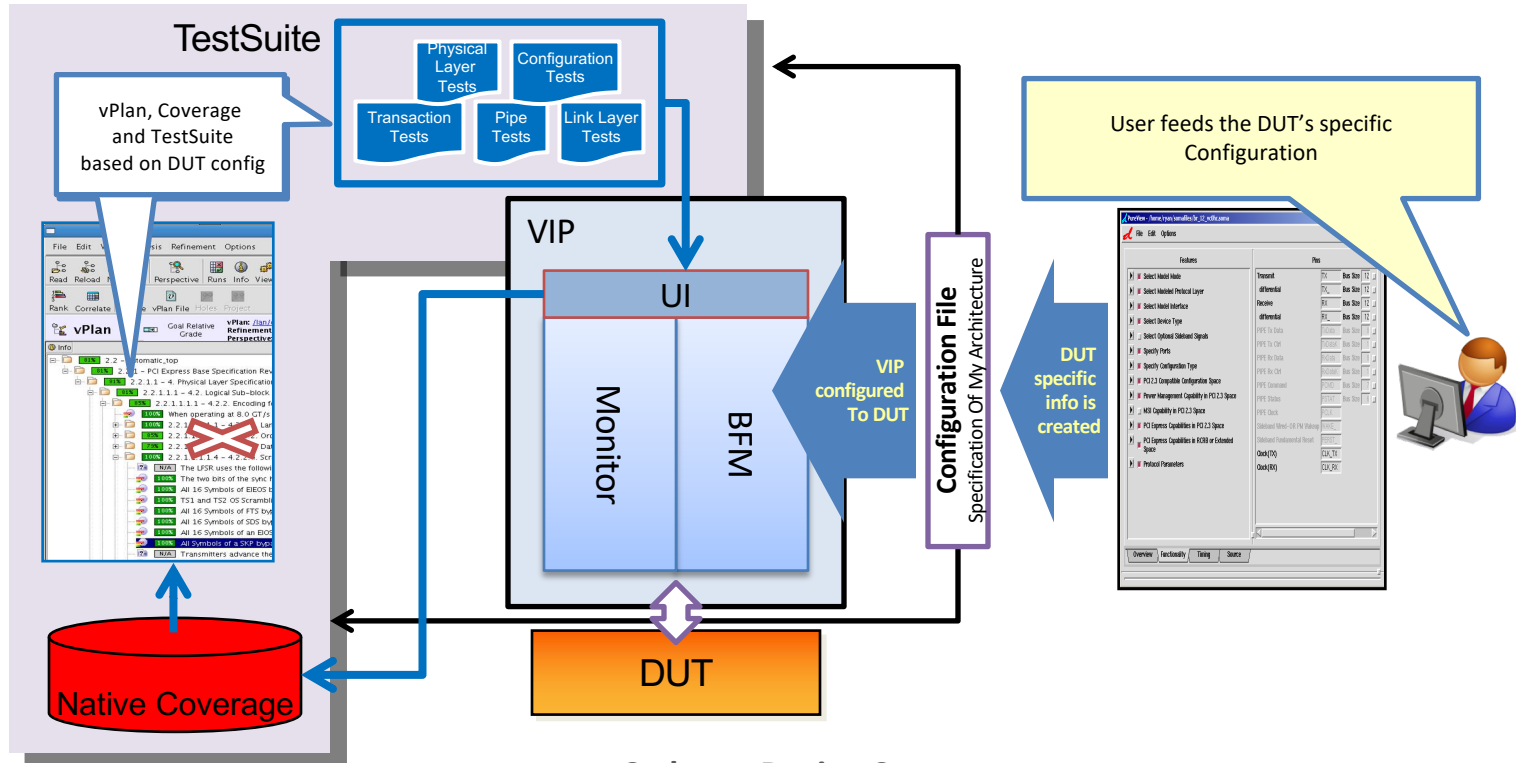


# Verification methodology for Spec compliancy



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# Verification methodology for Spec compliancy



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# How to create the MIPI CSI-2<sup>SM</sup> Verification Plan?

Version 1.3  
29-May-2014

Specification for CSI-2

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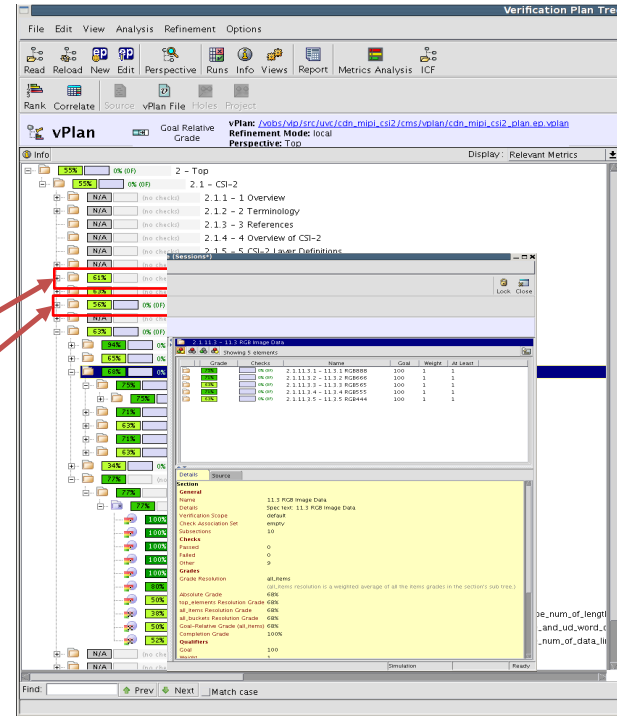
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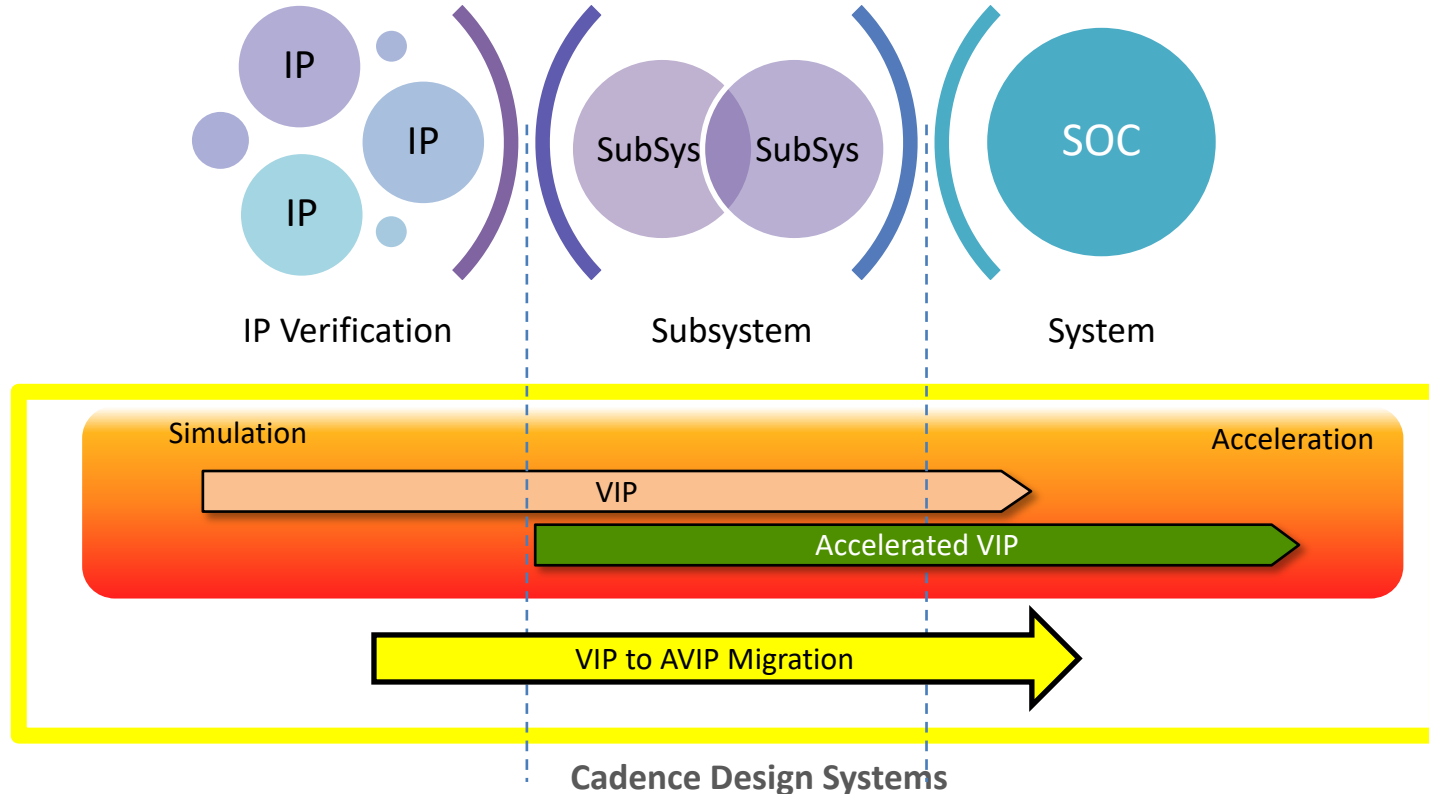
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# Development Flow and VIP Tools Map

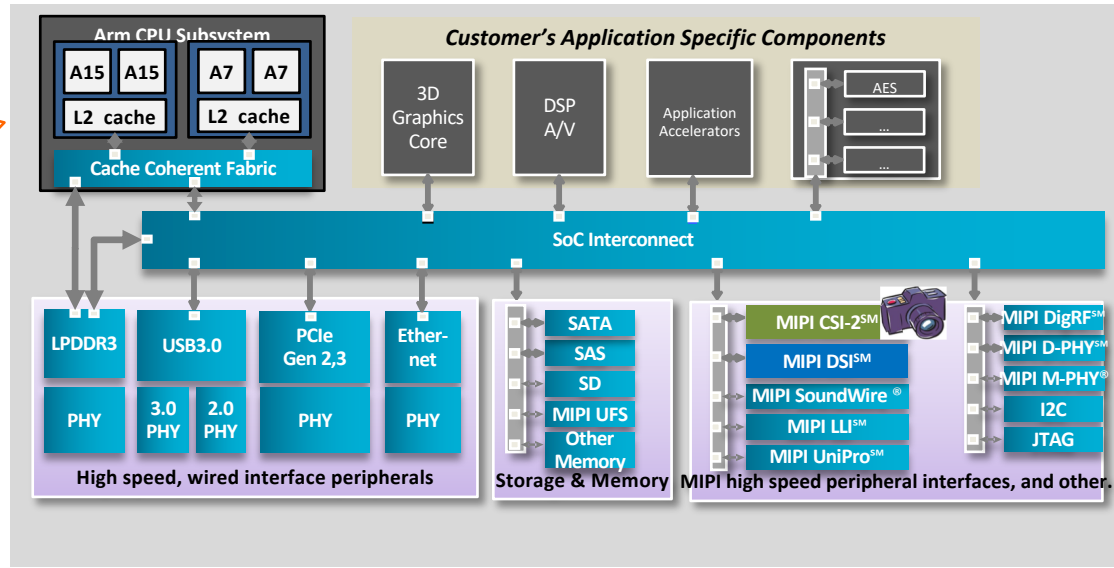


# Why Acceleration ?

**Software**

```

versionStr = GetVerStr();
if (versionStr == "-1") {
    return false;
} else if (versionStr != "0") {
    if (strcmp(versionStr, "2.0.0.11") != 0) {
        // Given "MMN 2.0.0.11"
        tempArray = versionStr;
        tempStr = tempArray;
        versionArray = tempStr;
    } else {
        versionArray = versionStr;
    }
}
var versionMajor = versionArray;
var versionMinor = versionArray;
var versionRevision = versionArray;
// Is the major revision unique?
if (versionMajor > parseFloat(tempStr))
    return true;
} else if (versionMajor == parseFloat(tempStr))
    return true;
} else if (versionMinor == p
else if (versionRevision == p
if (versionRevision
return true;
    
```



Complex SoCs, comprised of tens of millions of logic gates, will impede software simulators, even when running on the fastest servers.

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# Overview of hardware assisted verification

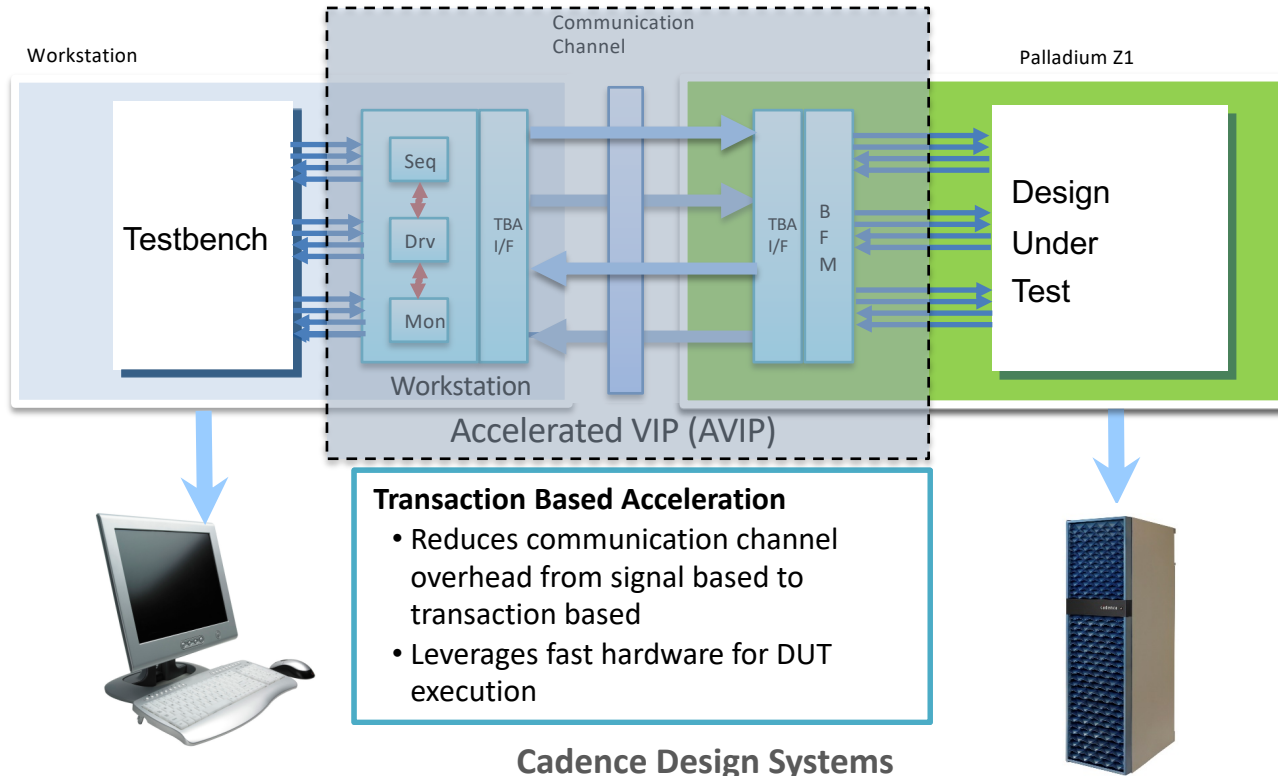
- Emulator assisted verification
  - Simulation Acceleration
  - Virtual Emulation
  - In-Circuit Emulation
  
- FPGA Prototyping



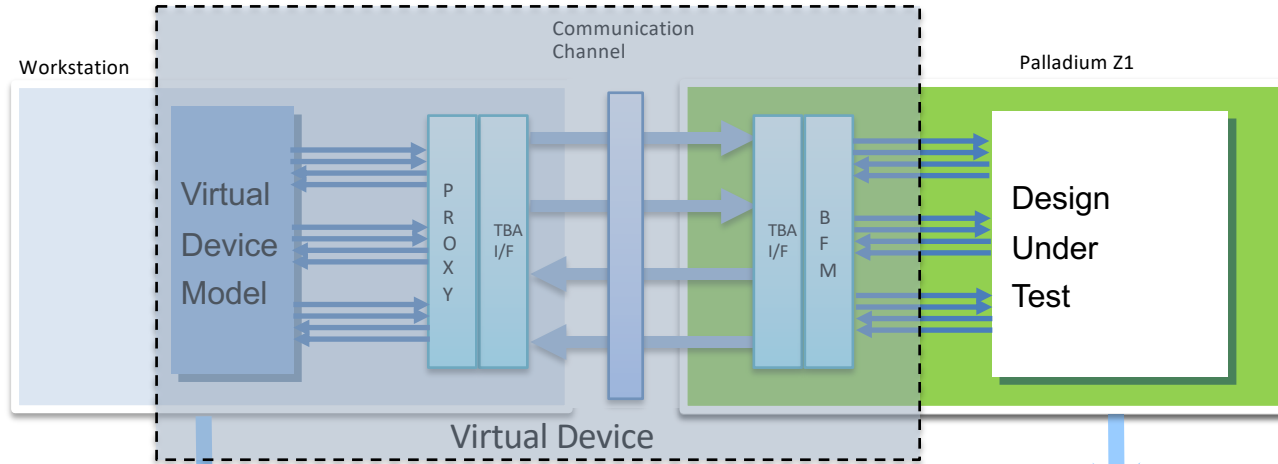
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# Simulation Acceleration & Accelerated VIP

## Transaction Based Acceleration



# Virtual emulation & Virtual Device



**Virtual emulation**

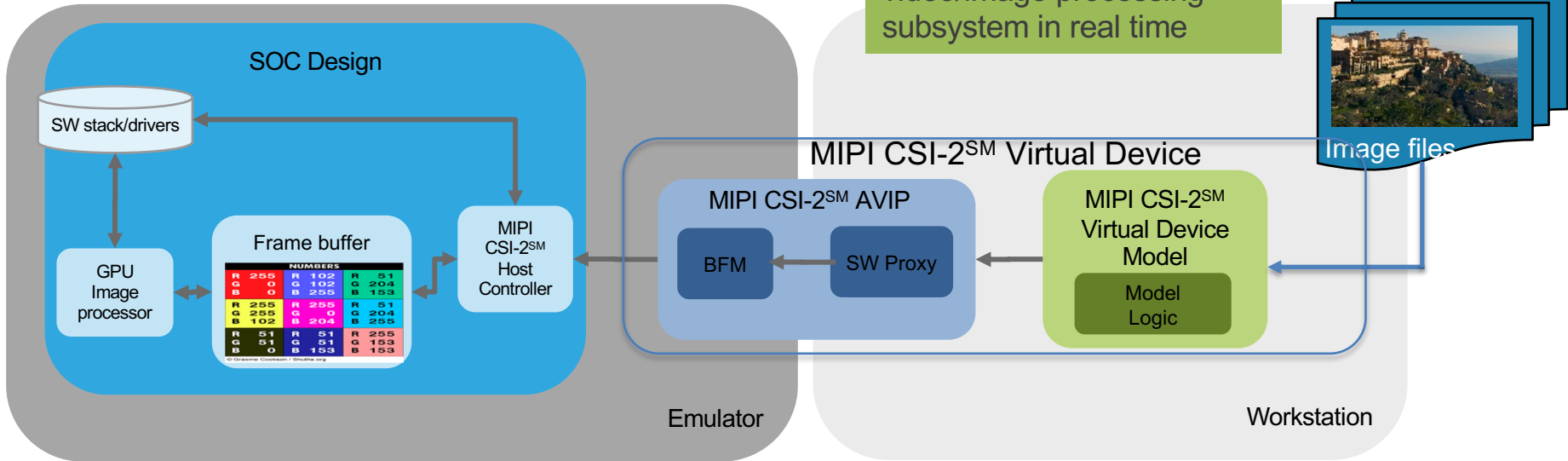
- Enables testing the design with real-world traffic
- Leverages fast hardware for DUT execution



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# MIPI CSI-2<sup>SM</sup> Virtual Device

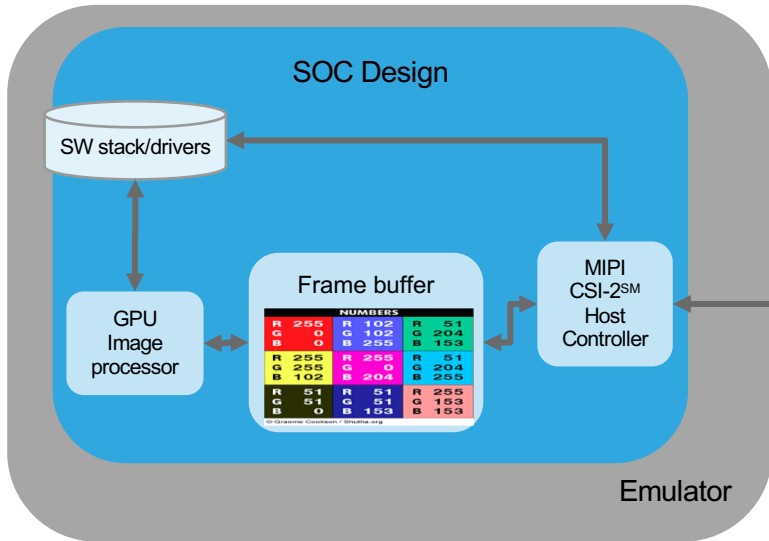
Enables visualization of the HW/SW operation of the video/image processing subsystem in real time



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# MIPI CSI-2<sup>SM</sup> Emulation/Prototyping with real sensor

Enables connection of real sensors to emulated SOC designs for live video and closed loop testing



Frame buffer

NUMBERS					
R 255	R 102	R 51	G 204	G 102	G 204
B 0	B 255	B 153	B 153	B 153	B 153
R 255	R 255	R 51	G 204	G 102	G 204
G 255	G 0	G 204	B 255	B 102	B 204
B 102	B 204	B 255	B 255	B 153	B 153
R 51	R 51	R 255	G 153	G 51	G 153
G 51	G 51	G 153	B 153	B 51	B 153

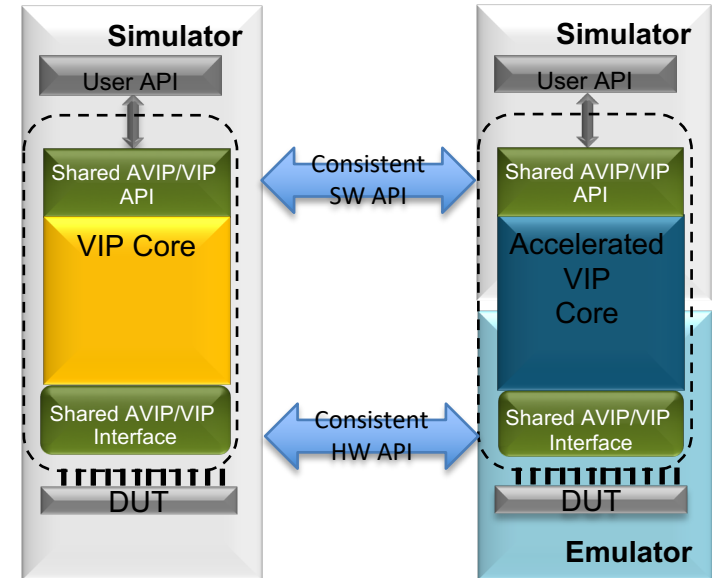


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# Concepts for building an acceleration-ready environment

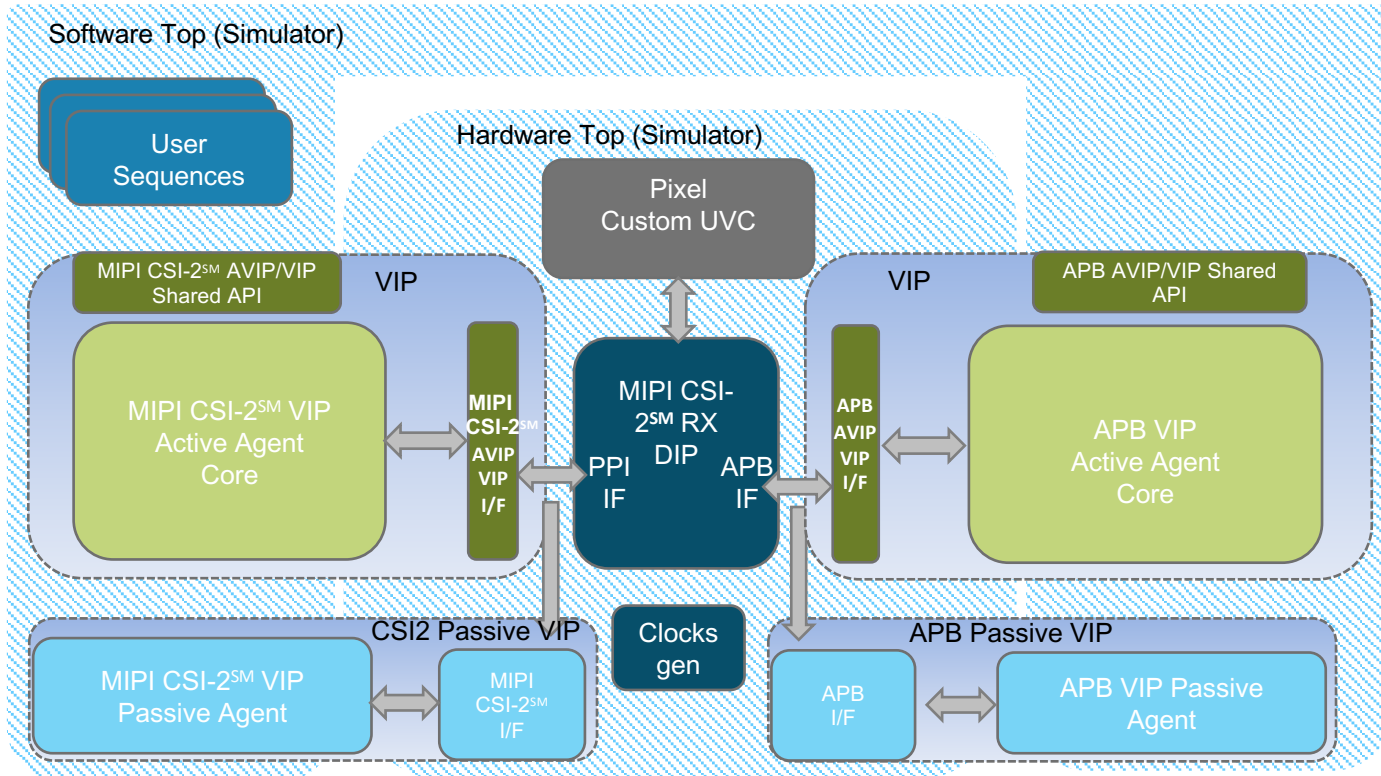
- Use consistent API for VIPs/AVIPs
- Use Dual-Top structure for the verification environment
  - The Hardware top will include the DUT, Interfaces, clocks generation, etc.
  - The software top will include the SW Verification Environment.
- Use event based delays instead of cycle/time based delays whenever possible.
- Pre define simulation and acceleration subset of shared sequences



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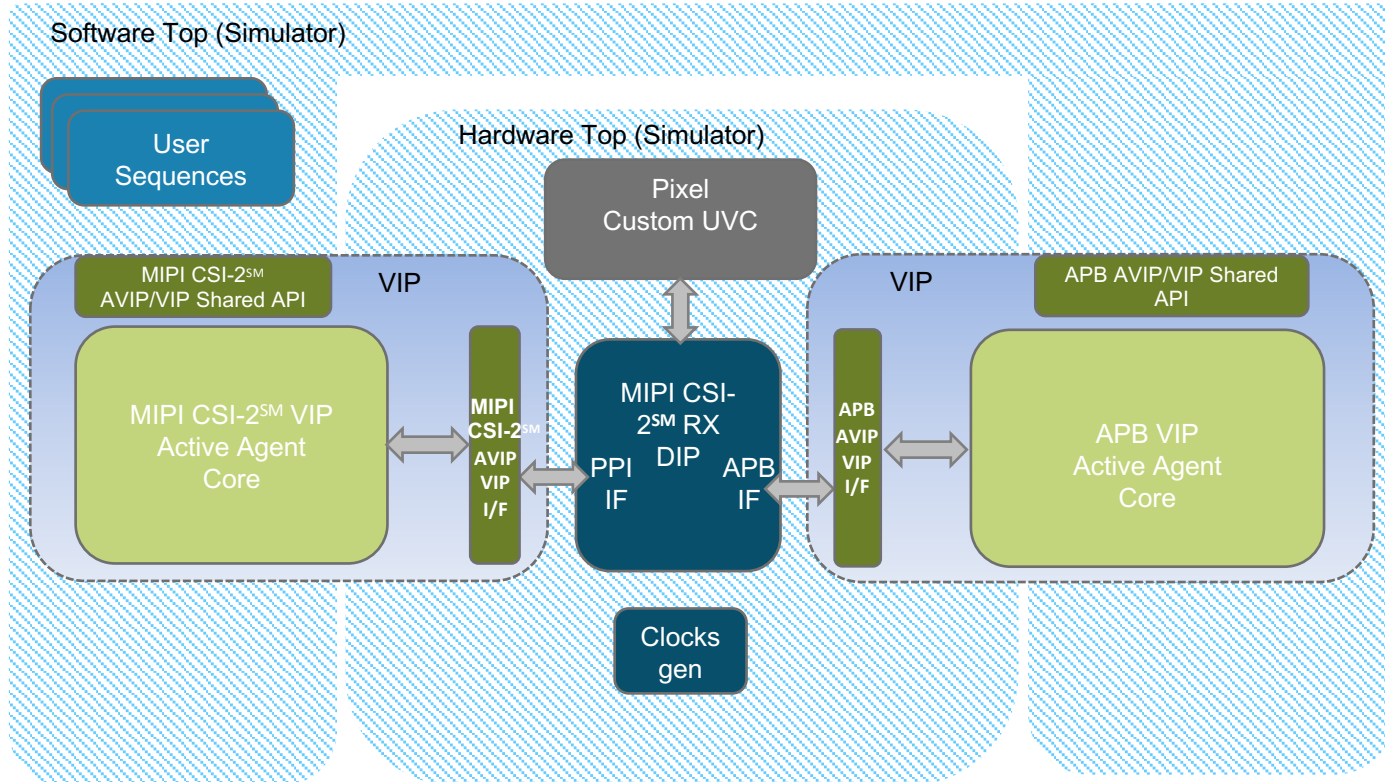
# MIPI CSI-2<sup>SM</sup> IP Level: From simulation to acceleration

## Simulation stage



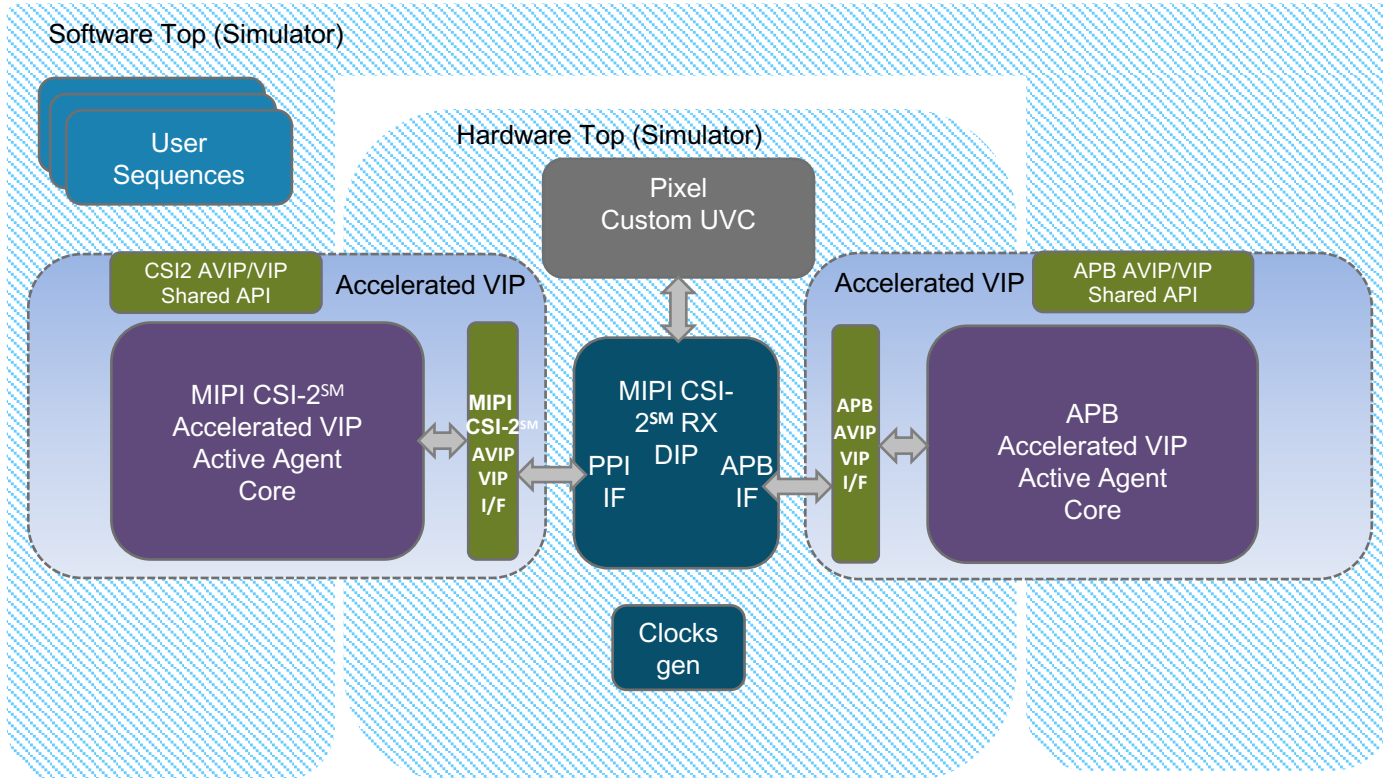
# MIPI CSI-2<sup>SM</sup> IP Level: From simulation to acceleration

## Step #1 Disabling passive agents used at IP level stage



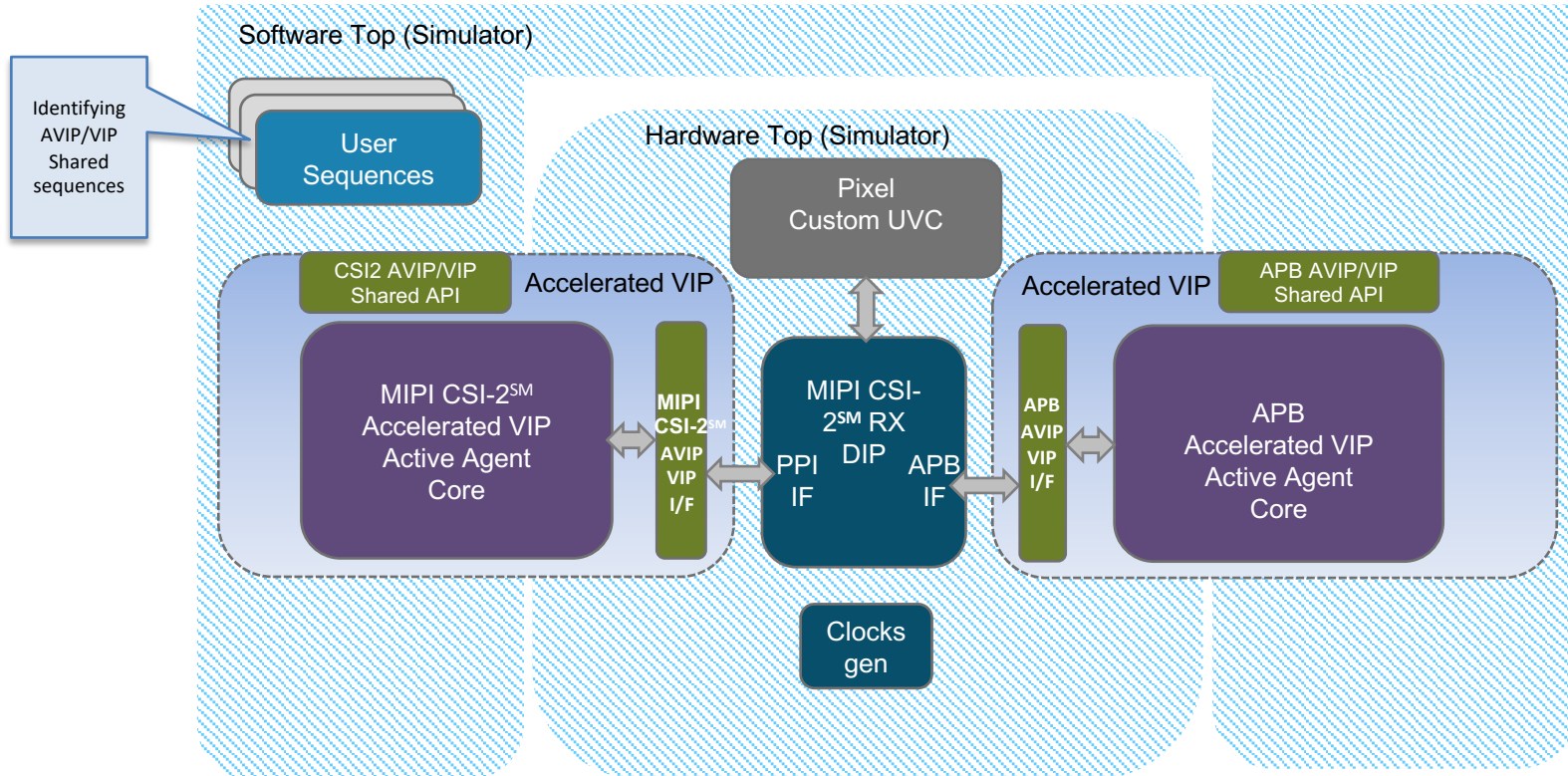
# MIPI CSI-2<sup>SM</sup> IP Level: From simulation to acceleration

## Step #2 Migrating to Accelerated VIPs



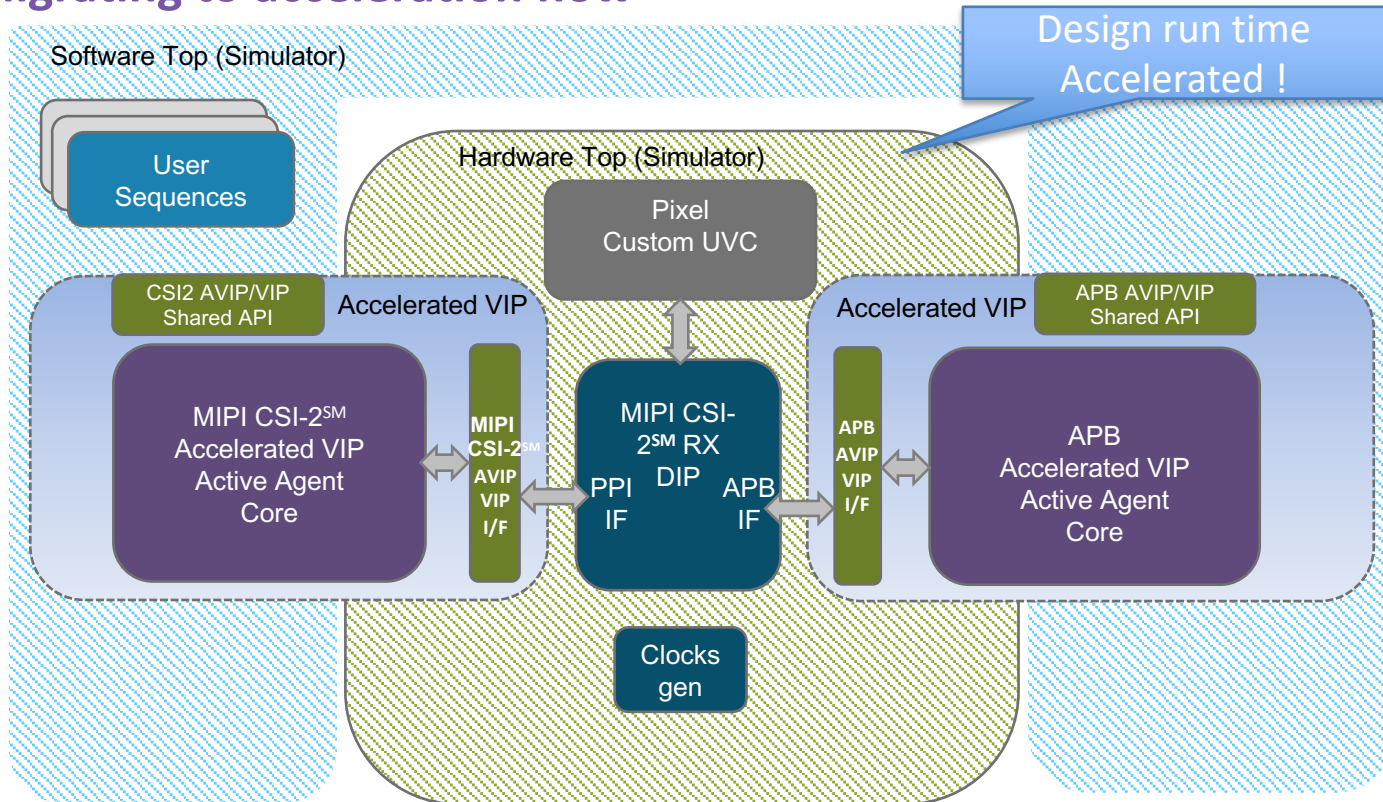
# MIPI CSI-2<sup>SM</sup> IP Level: From simulation to acceleration

## Step #3 Choosing the subset of sequences required for acceleration



# MIPI CSI-2<sup>SM</sup> IP Level: From simulation to acceleration

## Step #4 Migrating to acceleration flow



# Summary: Advantages of using acceleration

- Enables orders-of-magnitude gains in throughput over Simulation
- Enables re using selected parts of your simulation verification environment
- Enables advanced technologies with virtual emulation, like:
  - Hybrid operation for optimal partition of the design between HW and SW to achieve maximum speedup
  - Connection to Virtual Devices, Virtual machines, etc.
- Enables OS-level benchmarks and driver bring-up

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## ADDITIONAL RESOURCES

- MIPI Camera WG URL: <https://members.mipi.org/wg/camera-wg/dashboard>
- MIPI CSI-2<sup>SM</sup> Spec URL: <https://members.mipi.org/wg/camera-wg/document/75006>
- Cadence Verification IP URL: <https://ip.cadence.com/ipportfolio/verification-ip/simulation-vip>
- Cadence Accelerated VIP URL: <https://ip.cadence.com/ipportfolio/verification-ip/accelerated-vip>

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