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Synopsys

**Powering AI and Automotive
Applications with the MIPI
Camera Interface**

MIPI ALLIANCE
DEVELOPERS
CONFERENCE

19 OCTOBER 2018

SEOUL

Agenda

Adoption of MIPI CSI-2SM Image sensors beyond mobile

AI and automotive examples

CSI-2 interface overview

Meeting reliability requirements of automotive applications

Supporting artificial intelligence (AI) applications

Summary

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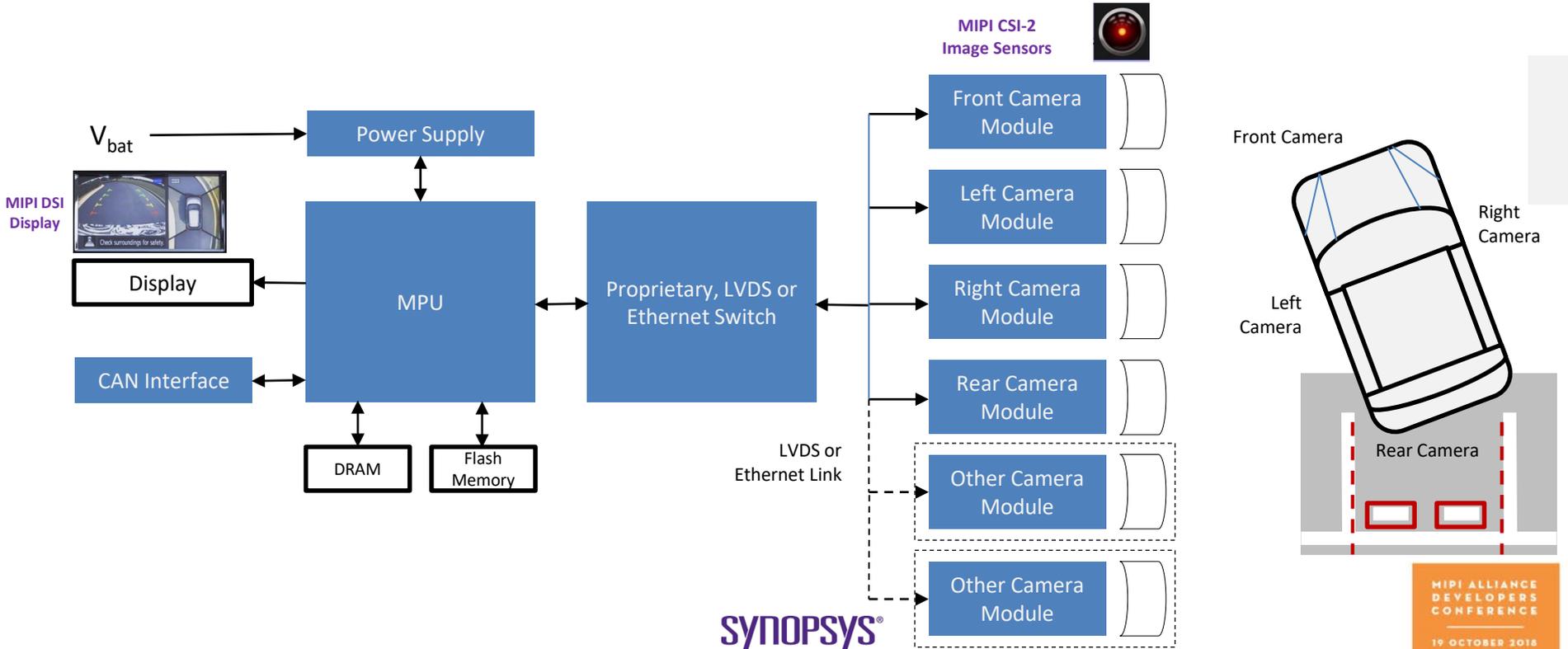
Industrial & Surveillance Applications

Using MIPI CSI-2 Image Sensors



Example of MIPI in an Automotive Application

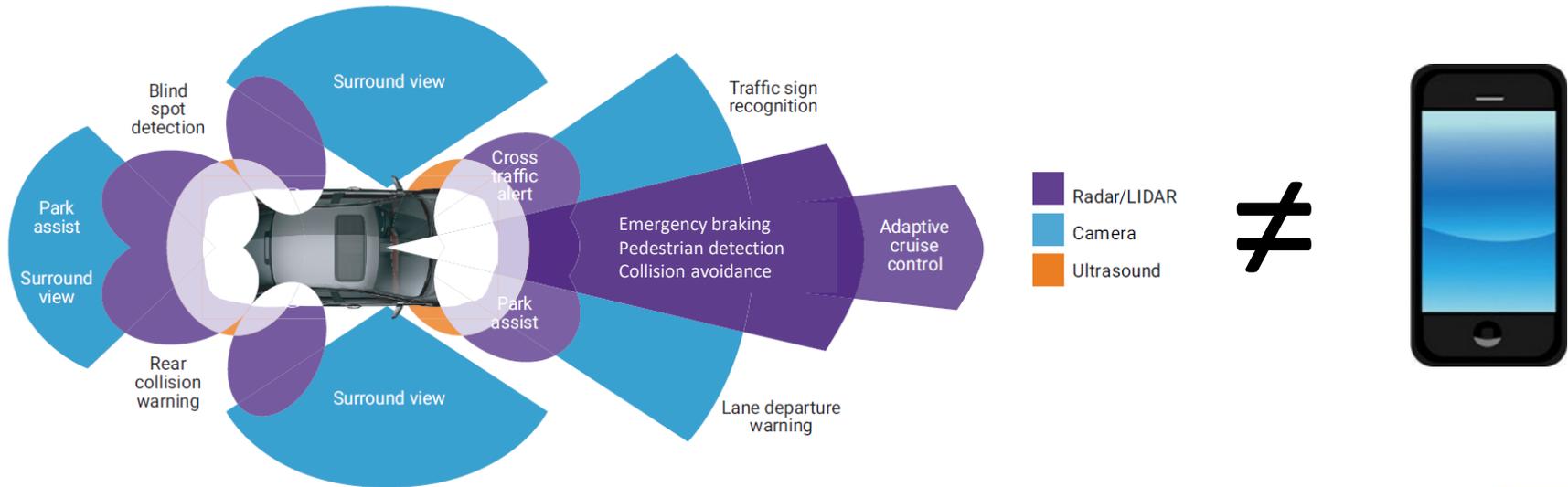
MIPI CSI-2 Image Sensors & DSI Display



Safety-Critical ADAS Applications

Require ISO 26262 Functional Safety Compliance and ASIL Certification

Electronics failure can have hazardous impact



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MIPI Specs for Automotive Applications

Infotainment

- Navigation
- Audio/Video
- Entertainment

Driver Information

- Instrument clusters
- Voice recognition
- Hi-def displays
- Surround view

mipi alliance *Auto*
System Diagram



Camera
MIPI CSI



Display Gauge
MIPI DSI



Sensor
MIPI I2C



Connectivity (LTE, Wi-Fi, BT)
MIPI DigiRF, MIPI RFPE



Display
MIPI DSI



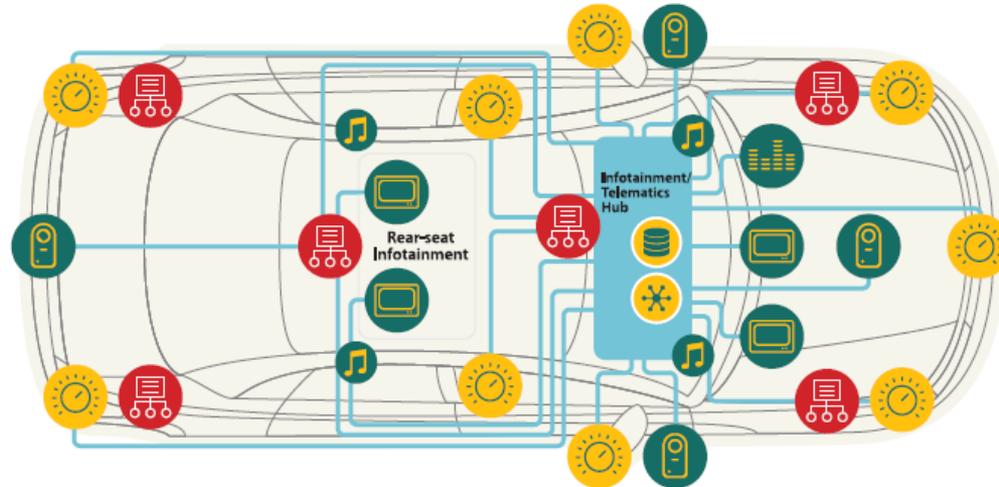
Audio
MIPI SoundWire, SLIMbus



Storage
UFS/MIPI UniPro-M



Network Bridge
(MIPI to/from Auto SerDes)



Vehicle Networks & V2X

- Real time video & data network
- Gateways
- Telematics
- V2V
- V2I
- Security

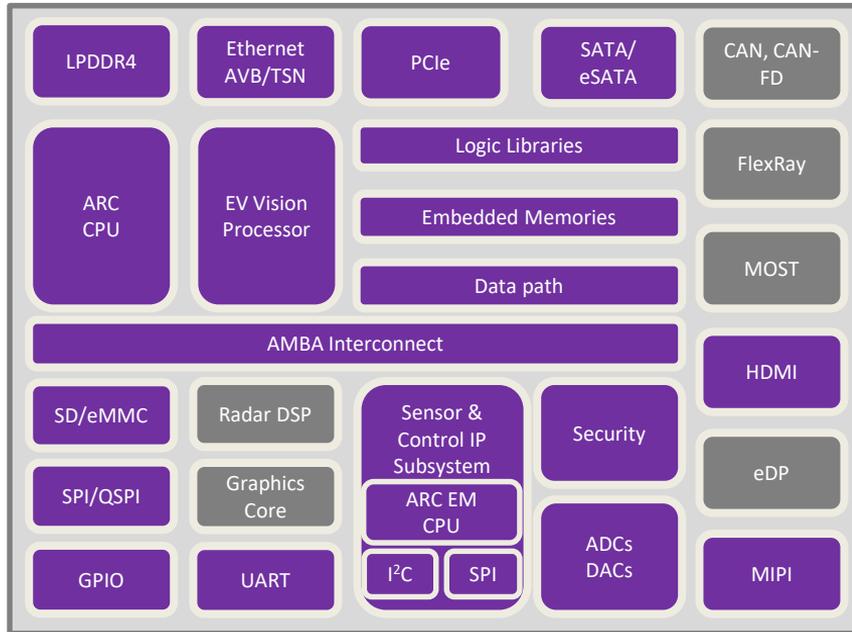
Driver Assistance

- Parking assist
- Lane departure warning & Lane keep aid
- Pedestrian detection & correction
- Automatic emergency braking

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Centralized ADAS Domain Controller SoC Architecture

Encompassing Numerous IP



- Interfaces: LPDDR4/4x, Ethernet AVB/TSN, MIPI, HDMI, PCI Express, SATA, ADC
- Embedded vision
- Security
- Sensor fusion
- Going to advanced process nodes
- Requires functional safety

Key Requirements of Automotive-Grade IP

Reduce Risk and Accelerate Qualification for Automotive SoCs

-  **Functional Safety**
Accelerate ISO 26262 functional safety assessments to help ensure designers reach target ASIL levels
-  **Reliability**
Reduce risk & development time for AEC-Q100 qualification of SoCs
-  **Quality**
Meet quality levels required for automotive applications

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Artificial Intelligence

Artificial Intelligence
Mimics human behavior

Machine Learning
Uses advanced statistical algorithms to improve AI

Regression

Bayesian

Clustering

Decision Trees

Vector Machines

Neural Networks

Deep Learning
Training of neural networks

Convolutional

Recurrent

- Artificial Intelligence mimics human behavior
- Machine learning uses advanced statistical models to find patterns & results
- Deep learning is a specialized subset of machine learning using neural networks data to recognize patterns

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Edge Inference Connectivity for Deep Learning

Cloud Connectivity

- Ethernet

Chip-to-Chip Connectivity

- PCI Express
- CCIX

Super Image Resolution

- USB/DP
- HDMI

Audio

- USB
- PDM/I2S
- ARC Data Fusion IP Subsystem

Wireless Sensor Connectivity

- Bluetooth 5 Link Layer & PHY
- 802.15.4 MAC & PHY



Memory Performance

- DDR/LPDDR
- HBM2
- Embedded Memories & Logic Libraries

Vision

- MIPI CSI-2 & MIPI D-PHY



Sensor Connectivity

- MIPI I3C Controller
- ARC Sensor and Control IP Subsystem

Deep Learning SoC Challenges

Unique Requirements for Processing, Memory, Connectivity

Specialized Processing

- Heterogeneous processing (scalar, vector, neural network)
- Massively parallel, matrix multiplication (neural network)
- Model compression via pruning and quantization – (Increases irregular compute intensity and memory accesses)

Memory Performance

- Capacity and bandwidth constraints
- Cache coherency requirements
- Advanced processes maximize on-chip SRAM to reduce data movement

Real-Time Connectivity

- Reliable and configurable connectivity to AI data centers
- Real-time interface to sensors, images, audio, cloud, and more
- Reduced energy via power management features and FinFET technologies

MIPI CSI-2 Specification

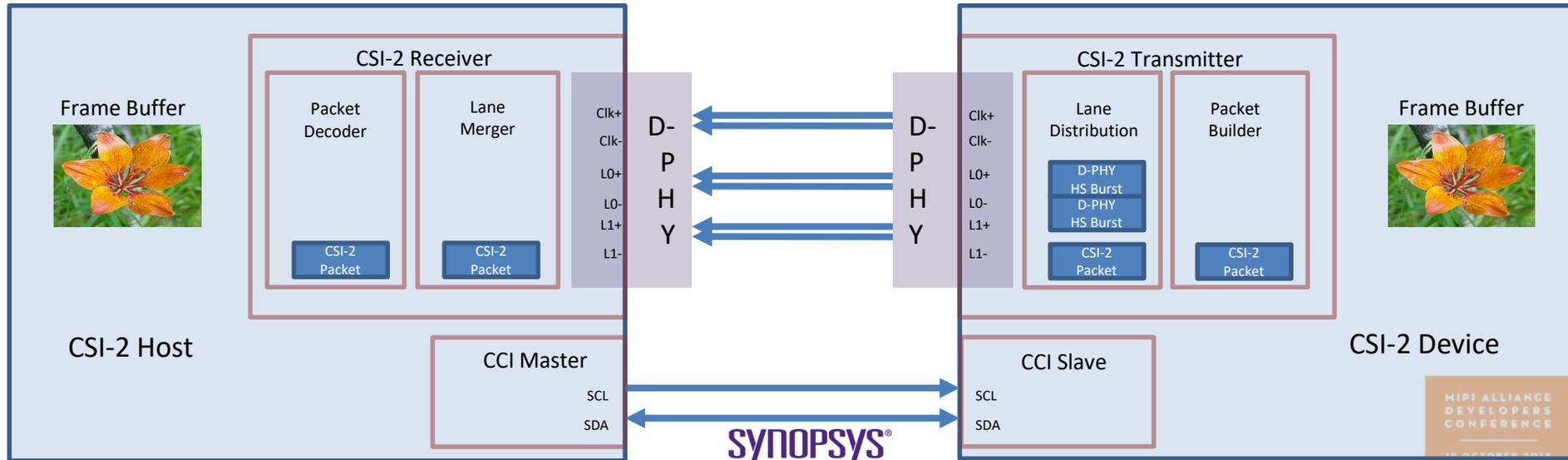
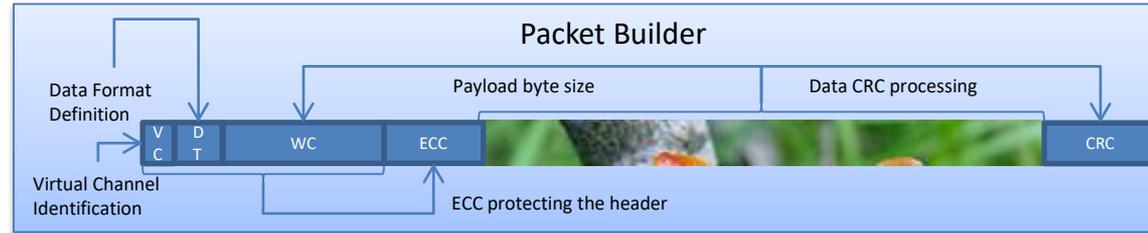
MIPI Camera Serial Interface 2 (CSI-2)

Key Improvements; From Mobile to Imaging & Vision

CSI-2 Specification version Approval Date	<u>v1.x</u>	<u>v2.x</u>	<u>v3.X</u>	TBD
vX.0	29-Nov'05 <ul style="list-style-type: none"> First release. 	28-Mar'17 <ul style="list-style-type: none"> D-PHY v2.1 support C-PHY v1.2 support RAW 16/20 & DPCM 12-10-12 PPI width extension (up to 32) LRTE Scrambling Extension of Virtual Channel 	Target: Q4'18 <ul style="list-style-type: none"> D-PHY v3.0 support C-PHY v2.0 support RAW24 EoTp USL sROI - Phase 1 	Target: Q4'19 <ul style="list-style-type: none"> GLD sROI - Phase 2 AR/VR Security Functional Safety Sync Image Sensor Unified Packet Header A-PHY
vX.01	14-Feb'11 <ul style="list-style-type: none"> D-PHYSM v1.0 support 			
vX.1	14-Feb'11 <ul style="list-style-type: none"> D-PHY 1.0 support 	09-Apr'18 <ul style="list-style-type: none"> I3C SDR & HDR_DRR support RAW24 EoTp Interleaved Encryption 		
vX.2	10-Sep'14 <ul style="list-style-type: none"> D-PHY v1.2 support 			
vX.3	07-Oct'14 <ul style="list-style-type: none"> C-PHY v1.0 support 			



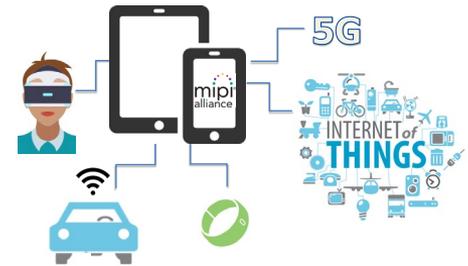
MIPI CSI-2 Over D-PHY



New Imaging Features for Automotive and Other Applications

- RAW-16 and RAW-20 color depth
- Latency Reduction and Transport Efficiency (LRTE) feature
- Differential Pulse Code Modulation (DPCM) 12-10-12 compression
- Scrambling to reduce Power Spectral Density (PSD) emissions
- Expanded number of virtual channels from 4 to 32

Image Quality/HDR - Latency - Reliability - Aggregation



Source: MIPI Alliance

RAW-16 & RAW-20 Color Depths

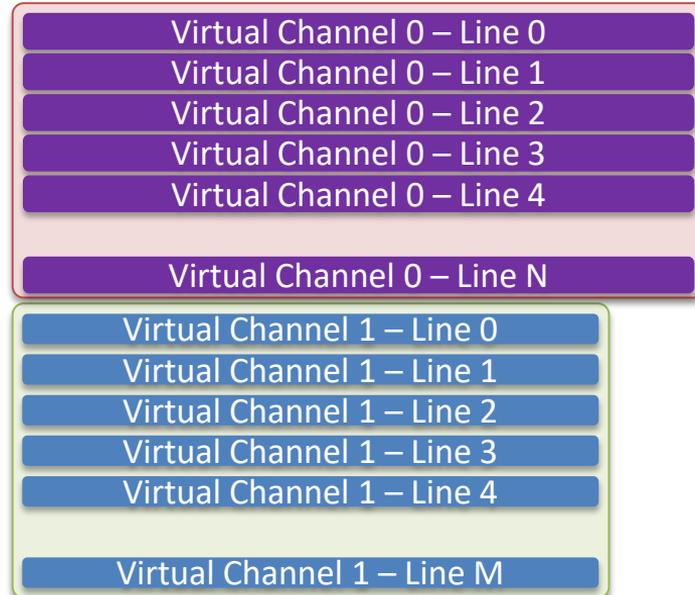
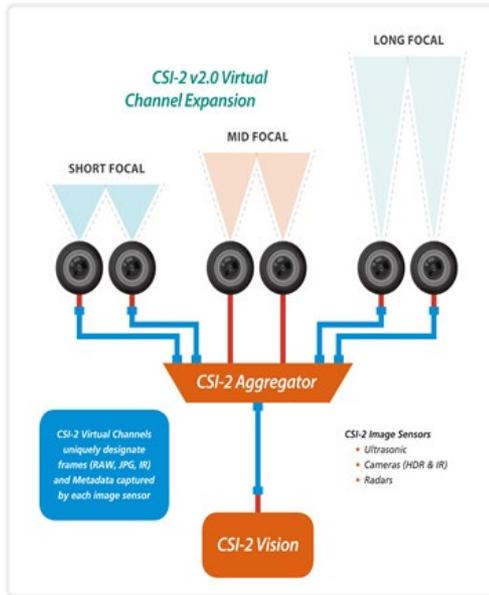
- CSI-2 v1.3 color depths are sufficient for Mobile. Visually, there is almost no change between RAW14 and RAW16/20
- RAW-16 and RAW-20 color depth bring advanced vision capabilities to Automotive and Industrial applications
 - Improves image capture when the environment changes suddenly and dramatically, for example in a big change in lighting condition



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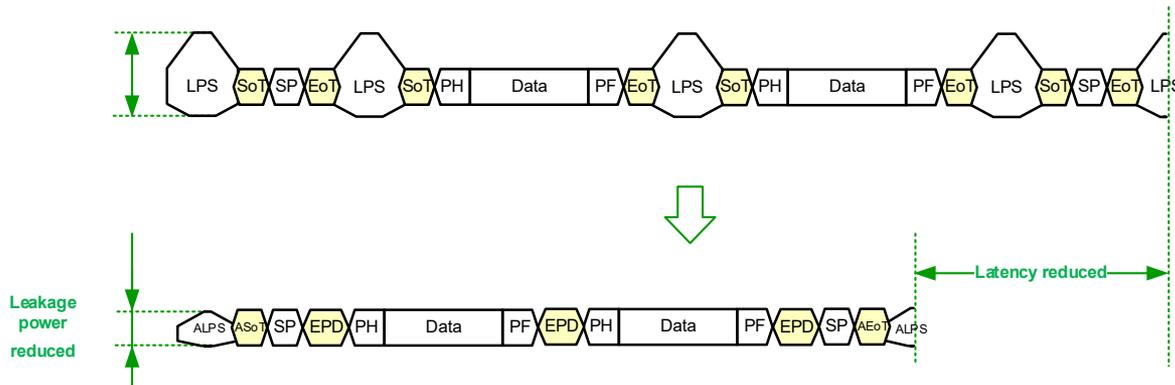
Up to 32 Virtual Channels

- To accommodate the larger number of image sensors and their multiple data types
- To support multi-exposure and multi-range sensor fusion for Advanced Driver Assistance Systems



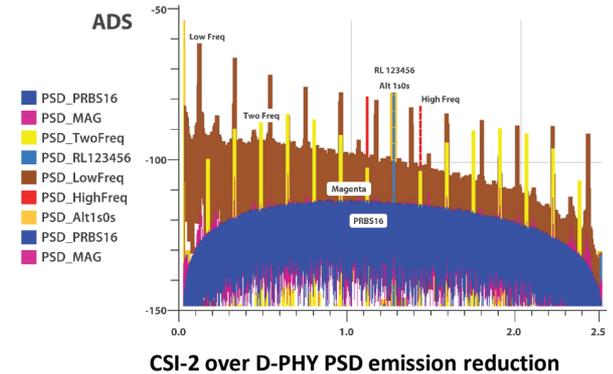
Added Latency Reduction & Transport Efficiency (LRTE)

- LRTE reduces frame transport latency & leakage power due to frequent "High Speed - Low Power" transitions.
- This will enhance image sensor aggregation and multi exposure for real-time perception and decision making applications



Scrambling and New Compression Scheme

- Galois Field Scrambling reduces power spectral density (PSD) emissions
 - Minimizes PSD emissions from aggressor components, which are particularly beneficial when placed near sensitive receiver
- New DPCM 12-10-12 compression to further boost image quality
 - Superior SNR using reduced bandwidth PHY
 - Removes more compression artifacts when comparing with previous MPI CSI-2 v1.3 compression mode

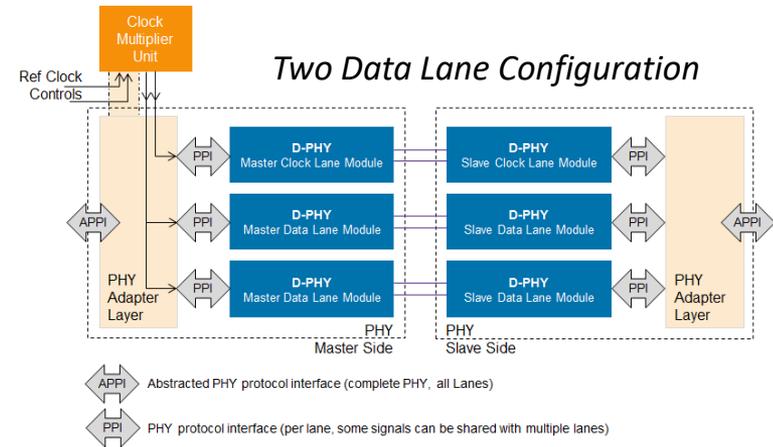


DPCM 12-8-12 vs DPCM 12-10-12

MIPI D-PHY Architecture

The Popular Physical Layer for MIPI CSI-2 and DSI Protocols

- Synchronous Forwarded DDR clock link architecture
- One clock and multiple data lanes configuration
- Static/dynamic de-skew supported through calibration
- Calibration hand-shake not supported
- No encoding overhead
- Low-power and high-speed modes
- Primarily targeting camera and display
- Spread spectrum clocking supported for EMI/EMC considerations
- Large eco-system, proven in millions of phones, cars



Benefits and Evolution of MIPI D-PHY

- Higher data rate enables ultra-high-definition cameras and displays
- Easier adaption of newer technologies
- Backward compatible
- Reliable with sufficient margins
- New specs augment existing ecosystem
- Growing market applications and segments
- Longer channel length

		Rx D-PHY Specification Version									
		D-PHY v2.1		D-PHY v2.0		D-PHY v1.2		D-PHY v1.1		D-PHY v1.0	
		Max Speed (Gbps)	Deskew Initialization	Max Speed (Gbps)	Deskew Initialization	Max Speed (Gbps)	Deskew Initialization	Max Speed (Gbps)	Deskew Initialization	Max Speed (Gbps)	Deskew Initialization
Tx D-PHY Specification Version	D-PHY v1.0	1.0	-	1.0	-	1.0	-	1.0	-	1.0	-
	D-PHY v1.1	1.5	-	1.5	-	1.5	-	1.5	-	1.0	-
	D-PHY v1.2	2.5	Yes	2.5	Yes	2.5	Yes	1.5	-	1.0	-
		1.5	-	1.5	-	1.5	-				
	D-PHY v2.0	4.5	Yes	4.5	Yes	2.5	Yes	1.5	-	1.0	-
		1.5	-	1.5	-	1.5	-				
	D-PHY v2.1	4.5	Yes	4.5	Yes	2.5	Yes	1.5	-	1.0	-
		1.5	-	1.5	-	1.5	-				

Note:
Cells containing dashes ('-') indicate that Deskew Initialization is not required

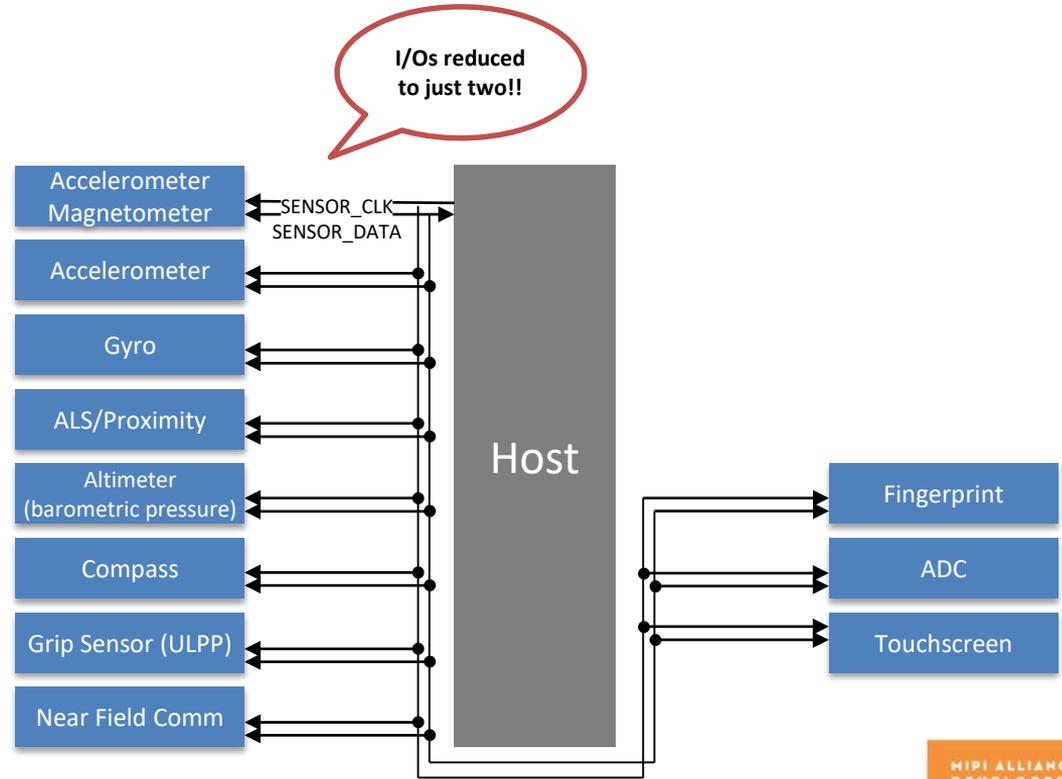


MIPI I3CSM Specification

MIPI I3C Overview

- Two wire serial Interface up to **12.5 MHz**
- **Supports Legacy I²C Slave** Devices
- I3C Single Data Rate (**SDR**) Mode
- I3C High Data Rate (**HDR**) Modes
- In-band Interrupts, Command support
- Dynamic Addressing
- Timing synchronization (aSync, Sync)

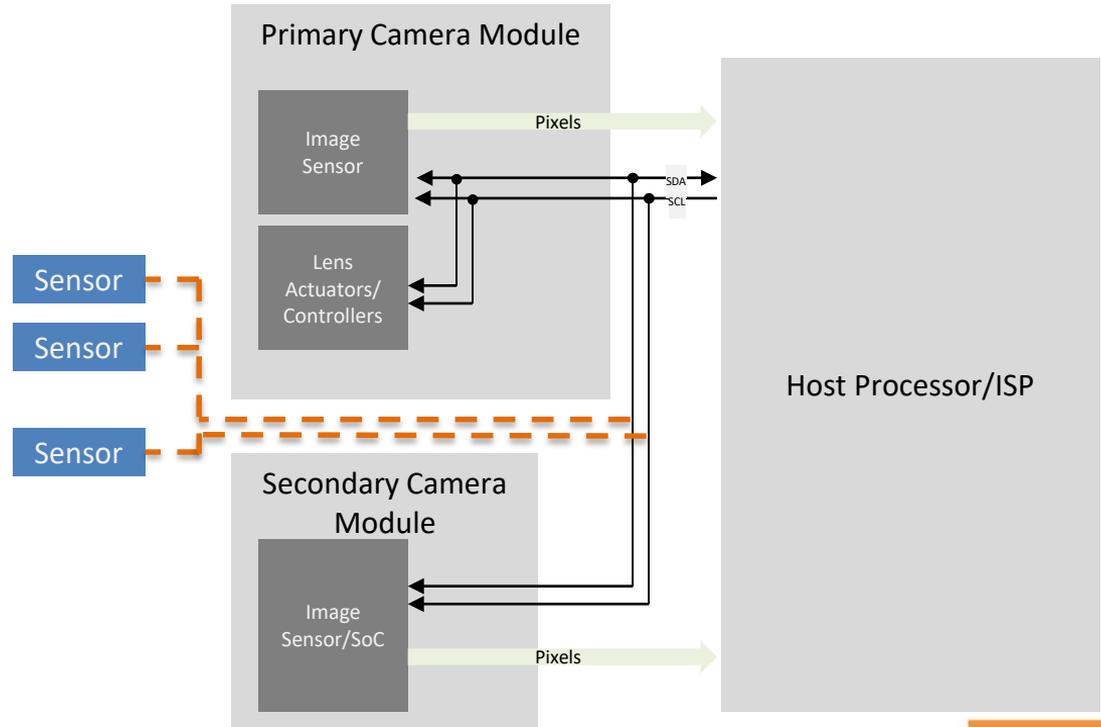
I2C FM	: Upto 400Kbps
I2C FM+	: Upto 1Mbps
I3C SDR	: 11.1 Mbps*
I3C HDR-DDR	: 22.2 Mbps*
I3C HDR-TSL	: 25.6 Mbps*
I3C HDR-TSP	: 33.4 Mbps*
* SCL@12.5Mhz	



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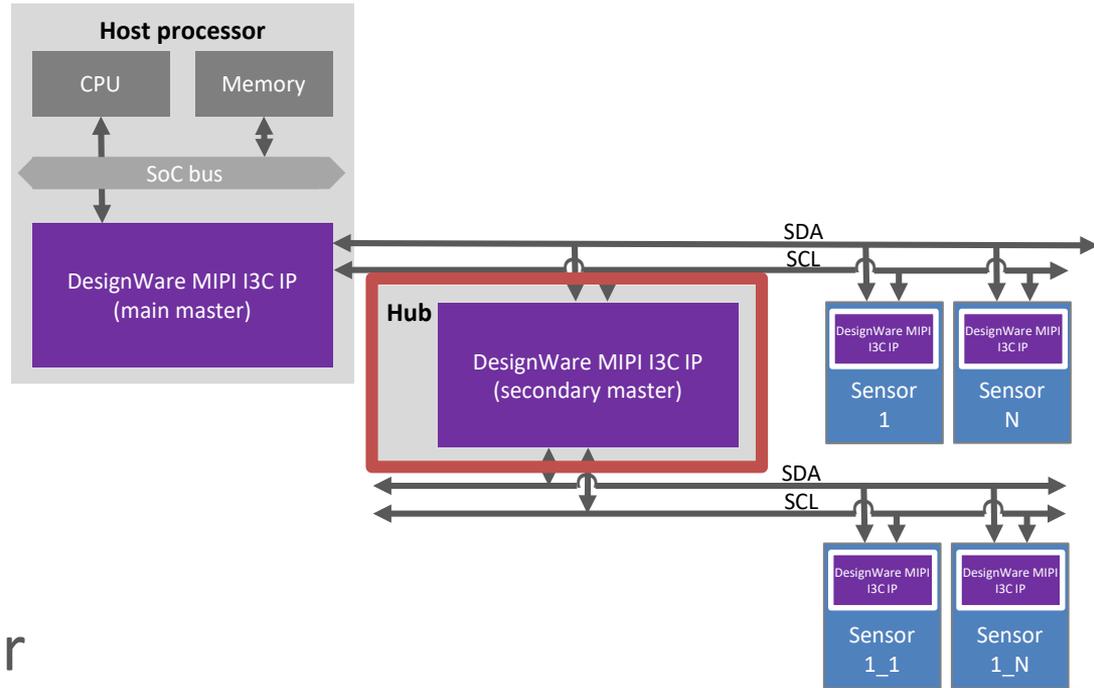
MIPI CSI-2, D-PHY & I3C

- Supports advances in imaging for new applications: Health, Convenience, Security, Lifestyle, Efficiency
- Camera Controller Interface (CCI) and Always-ON advancement considerations using I²C and future MIPI I3C



MIPI I3C Enables Efficient System Architectures

Example: Sensor Hub



Low Power, More
Efficient System,
Faster Data Transfer

Meeting Automotive and AI Requirements

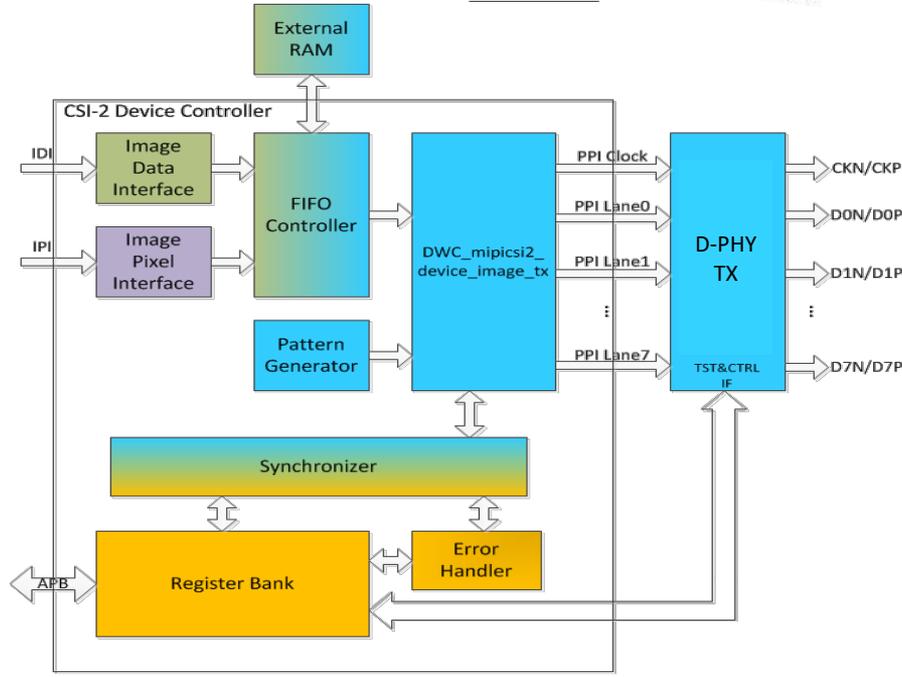
Automotive Safety Features

DesignWare MIPI CSI-2 Device Controller IP



- ECC Protection on Packet Header stored in Memory
- ECC Protection on IDI/IPI Packet Header
- Parity Protection on IPI Data Path
- Parity Protection on Configuration Registers
- IPI/IDI Overflow Protection
- CRC Protection on Packet data path
- IDI Header and payload Data checks
- Module Redundancy Protection for critical logic e.g. Error Handling, Channel Select

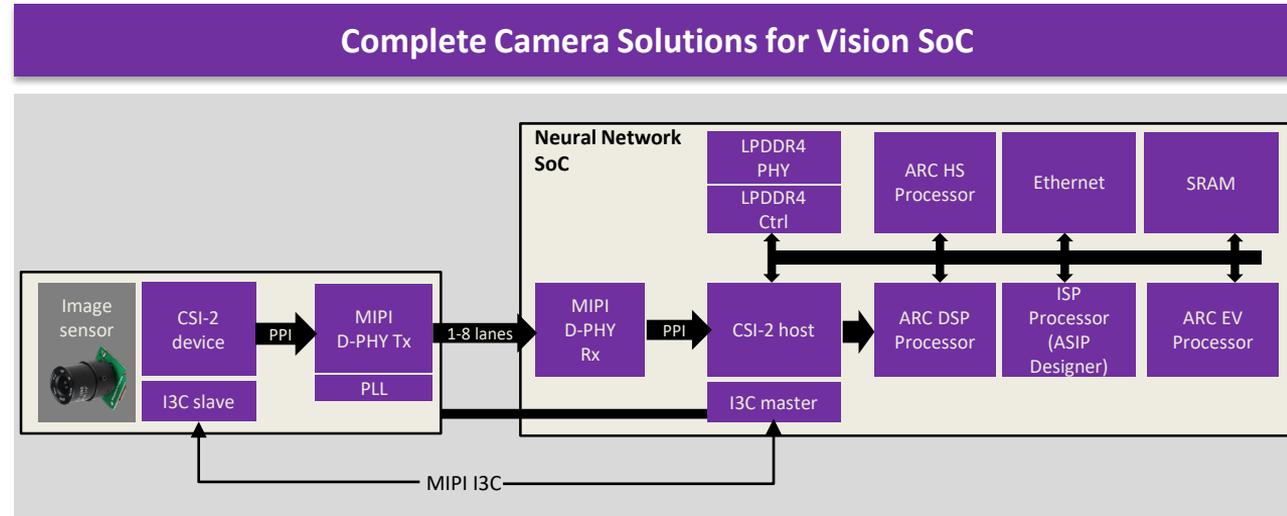
Certification for ISO 26262 Part 5 HW



Camera & Sensor Connectivity for Machine Vision

DesignWare MIPI CSI-2 and I3C Solutions

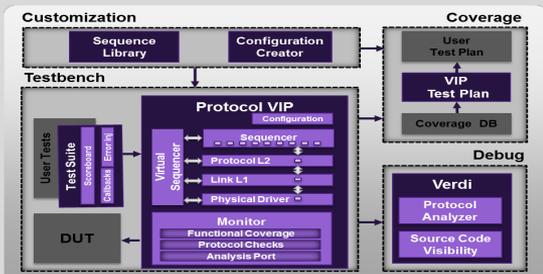
- Supports enhanced color depth using RAW16/20 formats for machine vision
- Multiple virtual channels accommodate larger number of image sensors supporting multi-exposure and multi-range sensor fusion
- Connect multiple sensors and cameras on a standard I3C two-wire interface



VC Verification IP for MIPI

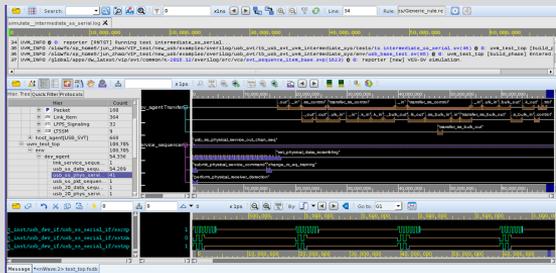
Integration

Testbench/VIP Languages & Methodologies



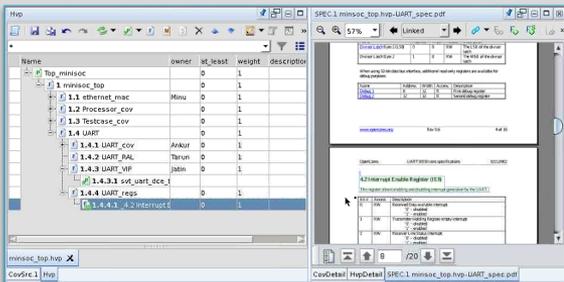
Performance

Number and Length of Tests



Coverage

Complete solution for Planning and Coverage



Debug

Signal to Protocol



- CSI-2 up to 2.1 with C-PHY up to 1.2 and DPHY up to 2.1
- DSI-2 1.0 with C-PHY 1.1 and DPHY 2.0
- DSI up to 1.3 with D-PHY up to 1.2
- DigRF v4 1.10, 1.00 and 0.64
- DBI 2.0
- DPI 2.0
- HSI
- I3C 1.1
- SoundWire
- RFFE
- SPI 2.0
- M-PHY 4.1/4.0
- UniPro 1.8/1.6

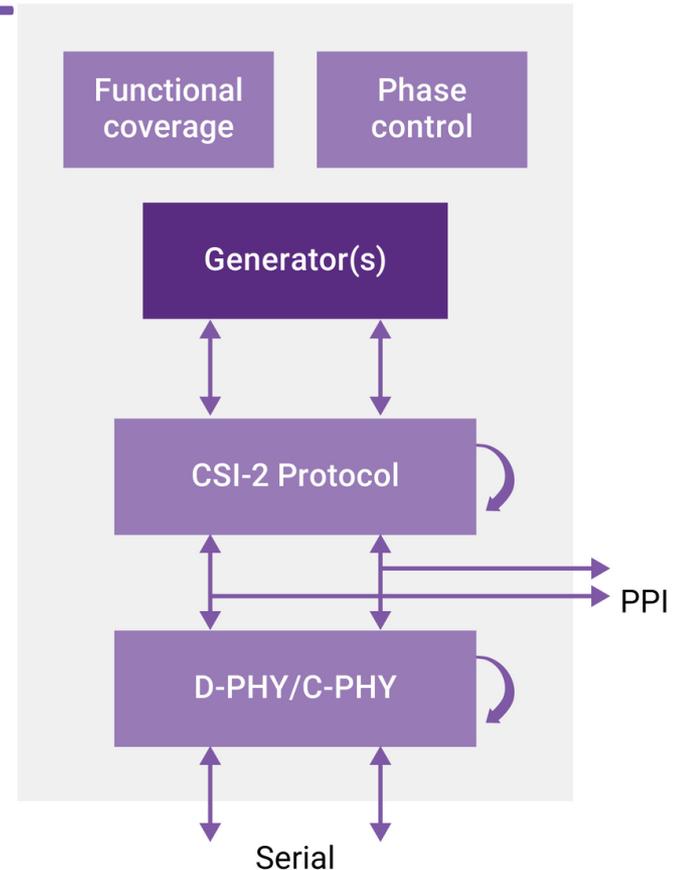
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VC Verification IP for MIPI CSI-2

Architecture and Key Features

- **Source code Test Suite (optional)**
- **Specifications supported**
 - CSI-2 2.1/2.0 with C-PHY 1.2/1.1 and D-PHY 2.1/2.0
 - CSI-2 1.3 with C-PHY 1.0 and D-PHY 1.2
 - CSI-2 1.1/1.2 with D-PHY 1.2/1.0
- **CSI-2 Transmitter and Receiver**
- **Physical Layer**
 - Configurable to C-PHY/D-PHY
 - Serial and Parallel (PPI) interface
 - High Speed and Escape Mode
 - Multi-Lane support (1 to N)
 - Configurable global timing parameters
 - Run-time reconfiguration of dynamic parameters
 - Lane transaction error injection

- **Protocol Layer**
 - 4 virtual channels (CSI-2 1.x)
 - 16 virtual channels (CSI-2 2.0 with D-PHY)
 - 32 virtual channels (CSI-2 2.0 with C-PHY)
 - All types of packets (short and long)
 - Interleaved and normal frames
 - Operative/Inoperative line and frame number
 - ECC generation, CRC generation and checking
 - Error detection and recording
 - Data Scrambling Support
 - Compression for RAW Data Type Support
 - LRTE with D-PHY and C-PHY

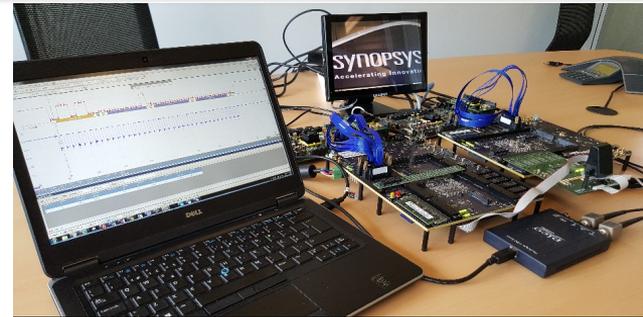
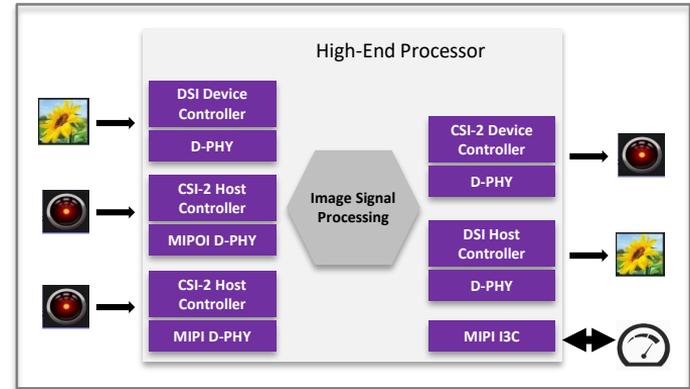


Silicon-Proven DesignWare MIPI IP Solutions

Single-Vendor Solution, Production-Proven, Interoperable

Complete camera, display and sensor interface IP solutions

- MIPI CSI-2, D-PHY and I3C protocols
 - Proven in 65nm - 7nm nodes customer designs
 - Automotive grade 1 and grade 2 PHYs
- Enables new set of applications in Automotive, AR/VR, IoT markets
 - Lowers integration risk for application processors, bridge ICs and multimedia co-processors
- Future proof IP supporting variety of speeds, proven in silicon
 - Reduces cost and power for multiple instantiations
 - Testability features enable low cost manufacturing



Industry's first MIPI I3C Demo



ADDITIONAL RESOURCES

- Synopsys DesignWare MIPI IP Solutions
 - www.synopsys.com/mipi
- MIPI CSI-2 Spec URL
 - <https://mipi.org/specifications/csi-2>



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