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MIPI ALLIANCE DEVELOPERS CONFERENCE

19 OCTOBER 2018

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Ahmed Ella
Mixel Inc.

Jeffrey Lukanc
Synaptics

Dual Mode MIPI C-PHY℠/D-PHY℠ Use in VR Display IC

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Outline

- GPU to Pixel VR Display System
- Mixel C-PHY℠/D-PHY℠ IP in VXR7200
- Summary

GPU to Pixel VR Display System

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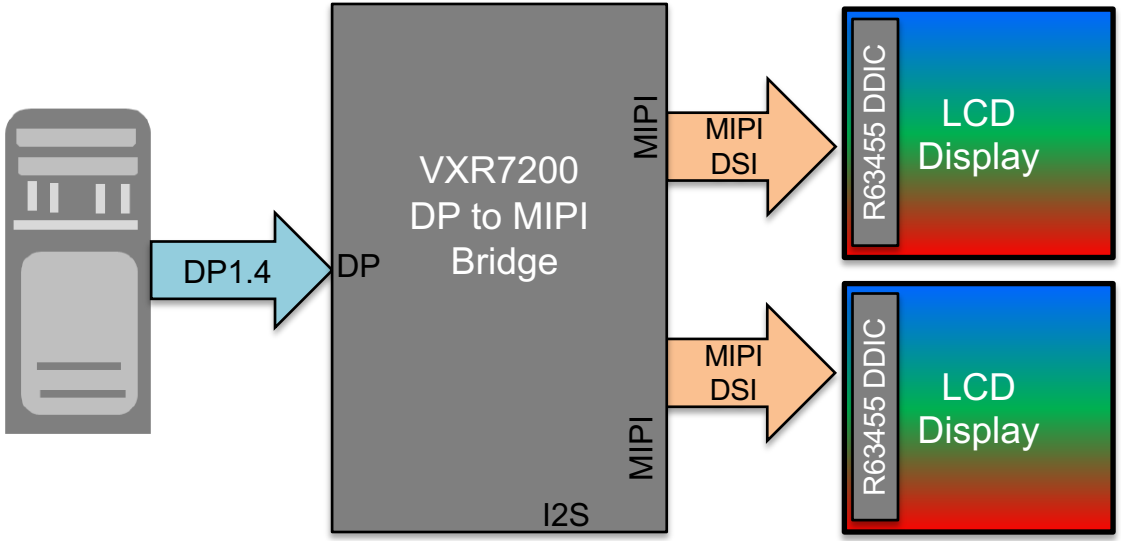
GPU to pixel VR display system overview

Video over DP or USB-C connector from PC or smartphone

MIPI D-PHY or C-PHY interface to displays



Flexible and Optimized GPU-to-Pixel Video Solution

VR Displays Drive Video Interface Technology

1. **PPI >1000 eliminates "screen door" effect & enables ability to read text**
   - Resolution: 2Kx2K minimum, better = 3Kx3K, ideal = 4Kx4K
2. **Display responsiveness**
   - For crisp LCD images, need to allocate frame time for pixel settling and backlight flashing
   - Additional time required for LCD to settle drives higher DP + MIPI bandwidths
3. **VR systems require higher video bandwidths to match display resolutions**
   - Need 32Gbps raw bandwidth GPU to display
   - Need DP DSC support to exceed dual 5.5M pixel displays
   - Need MIPI DSC support to exceed 6.2M pixel displays
   - Need SPR support for optimized OLED bandwidth
   - Foveal transport support allow full resolution foveal images at ½ the DP or MIPI bandwidth

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Synaptics VR Bridge & VR DDIC Chipset Overview

- **VR Bridge chip features**
  - DP1.4 with FEC
  - ~1 Line time video latency
    - Latency = lag = unresponsive HMD video
    - Low latency enables video to match USB Audio
  - SST or MST video formats
    - Either PC or cellphone applications
  - DSC or Synaptics SASPC compression
  - Supports 1-4 DDIC per display
  - D-PHY℠ @ 2.5Gbps Tx
  - C-PHY℠ @ 2.5Gsym/sec Tx
- **VR DDIC chip features**
  - Combo C-PHY℠/D-PHY℠ Rx
  - DSC or Synaptics SASPC decoders
  - Drive up to 4Kx3K displays
  - Built-in Foveal Transport image overlay
  - FIFO to adjust panel load/scan time
    - No need for buffering video in bridge
  - Pixel overdrive
  - Local dimming

VESA & MIPI Display standards interoperability

VR Bridge manages both DisplayPort and MIPI sides of bridge

- Provides display requirements to GPU via EDID/DisplayID
  - Video formats: Sub-Pixel Render, 420, 444, 8-bit, 10-bit
  - Compression: Compression algorithm and settings
  - Timing: allocate addition frame time for pixel settle and backlight flashing
- Configures the VR DDIC
  - Video formats: Sub-Pixel Render, 420, 444, 8-bit, 10-bit
  - Compression: Compression algorithm and settings
  - Panel scan time, settle time, backlight flash time
  - Pixel overdrive LUT
  - Local dimming settings
  - FIFO bandwidth settings

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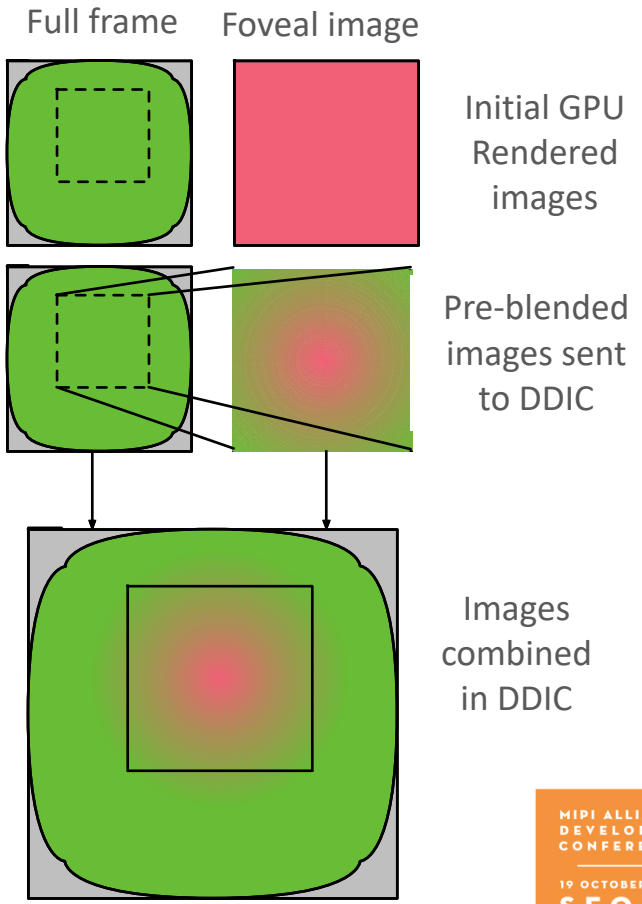
Introducing Foveal Transport

Foveal Rendering

- Renders a foveal image and a low res background image
- Both images are combined and sent at full resolution to a display
- Reduces render time, but benefits are not shared with system!

Foveal Transport

- GPU sends both images to displays ***without merging them***
- Gaze point location is embedded in the display data
- DDIC scales full frame and overlays the foveal image
- Chromatic and lens distortion algorithms for each image
- **Uses ½ the data and ½ the link bandwidth!**



Why dual-mode C-PHY℠/D-PHY℠ interface is required

- Large legacy display infrastructure requires MIPI D-PHY support for initial bring-up
- MIPI C-PHY required to match DP HBR3 bandwidth and display scan timing
- MIPI DSI-2℠ & DCS℠ are compatible with DP 1.4 enabling GPU to display compression
- Foveal Transport is compatible with both DP and MIPI DSI-2

Parameter	No Compression	2:1 Compression Bridge to Display	2:1 Compression GPU to Display	3:1 Compression GPU to Display	Foveal Transport GPU to Display	2880x1920 Display
MIPI data/line (bytes)	10,710	6,390	6,390	4,950	6,390	per Eye
MIPI total bandwidth (Gbps)	15	9	9	7	9	per Eye
Minimum MIPI C-PHY link:	6-trio C-PHY	4-trio C-PHY	4-trio C-PHY	3-trio C-PHY	4-trio C-PHY	per Eye
Minimum MIPI D-PHY link:	None	8-lane D-PHY	8-lane D-PHY	8-lane D-PHY	8-lane D-PHY	per Eye
DP data/line (bytes)	17,808	17,808	8,904	5,936	8,904	Host I/F
DP total bandwidth (Gbps)	32	32	16	11	16	Host I/F
Minimum DP link:	4-lane HBR3	4-lane HBR3	4-lane HBR2	2-lane HBR3	2-lane HBR3	Host I/F

Reduced MIPI & DP PHY Lane Usage Saves Power

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Mixel C-PHY℠/D-PHY℠ IP in VXR7200

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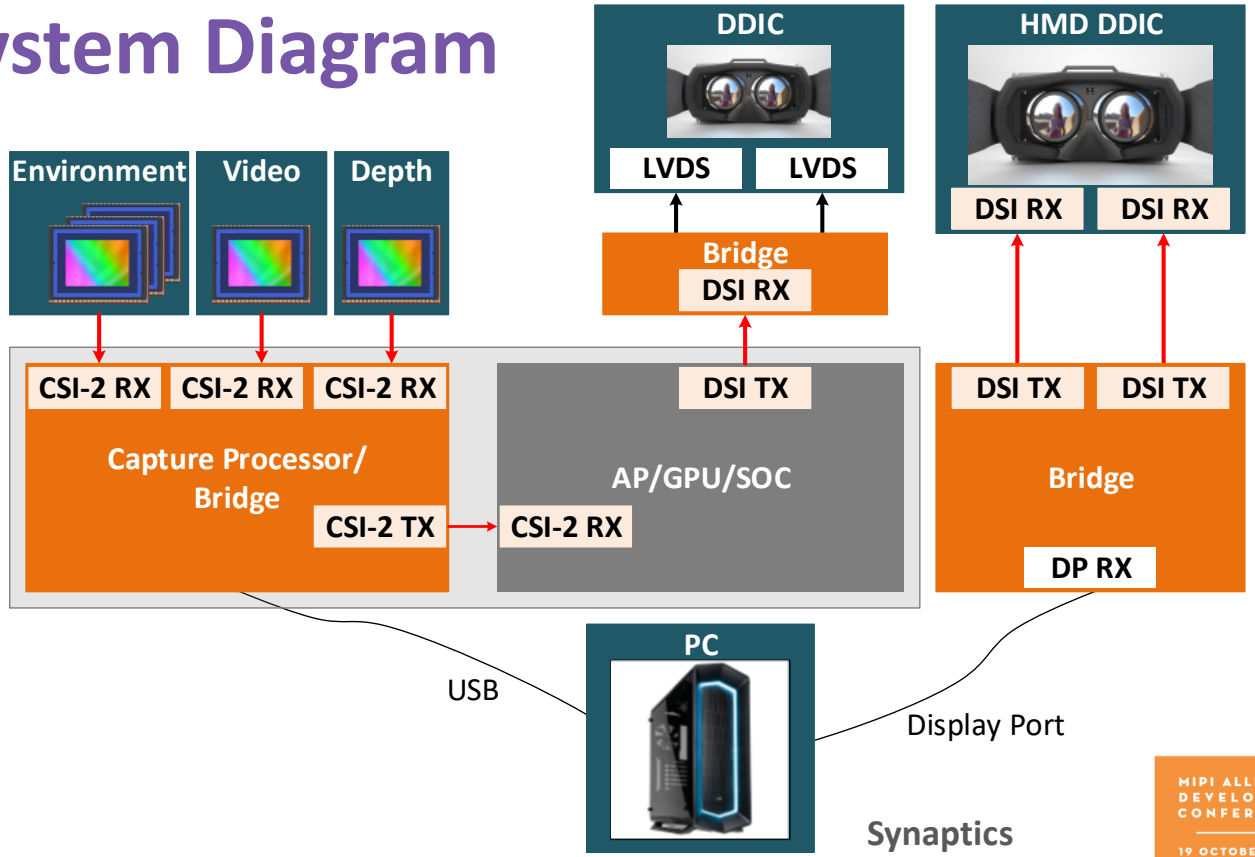
XR Generic System Diagram

- VR Flavors
  - Smartphone
  - Standalone HMD
  - Tethered VR
- Displays
  - Immersive Devices
  - Holographic Devices



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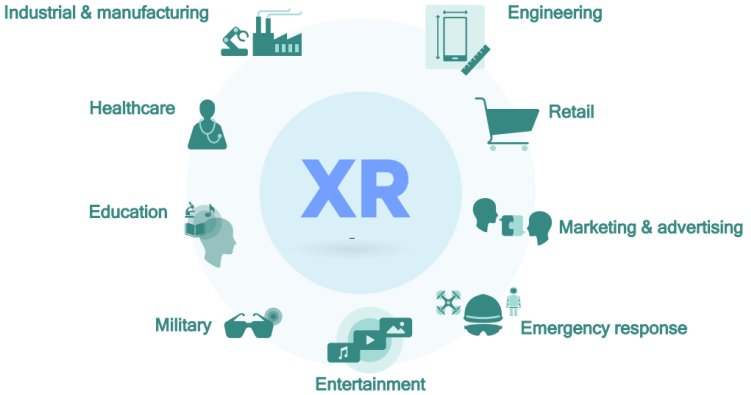
XR System Challenges

- High Bandwidth Requirements
  - High display resolution
  - Faster frame rate
  - Higher sensor resolution
  - High dynamic range
- SOC Design Constraints
  - Low Power / Heat
  - Package / Minimal pin count
  - Minimize die area
  - Support multiple use cases

Power and thermal efficiency is essential for XR

MIPI Spec Attributes

- Typical for **XR** Market
  - High bandwidth
  - Low power
  - Low EMI



From Qualcomm Extended Reality

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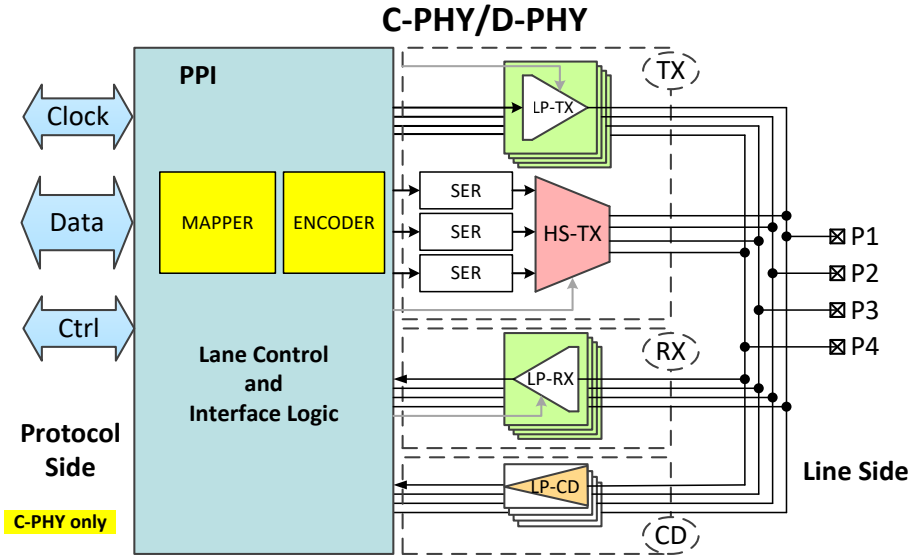
Mixel C-PHY℠/D-PHY℠ IP integrated in VXR7200

- Dual Mode PHY
  - D-PHY v1.2
  - C-PHY v1.1
- DSI-2 Controller
- Four Lane in D-PHY mode (10 pins)
- Three Lane in C-PHY mode (9 pins)
- Supports lane swapping and pin swapping features
- Supports de-skew calibration in D-PHY
- Supports T1 and T2 modes in C-PHY
- BIST with 100% coverage for HM



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MIPI D-PHY℠ and C-PHY℠ Comparison

Parameter	D-PHY v1.2	C-PHY v1.1
Adoption	Long history of use, wide adoption	Accelerated adoption, co-exists with D-PHY
Power/Gbps	Efficient	Higher efficiency
Maximum Bandwidth @2.5Gsps	10Gbps for 4 Lanes (10 pins)	17.1Gbps for 3 Lanes (9 pins)
Minimum number of pins	4	3
Flexibility	All lanes operate together.	Each lane can work independently.

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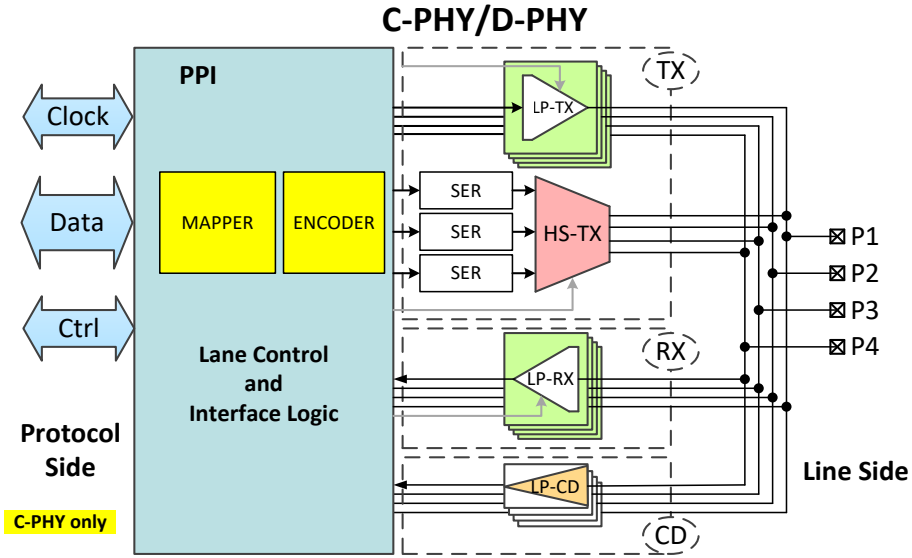
Advantage of Mixel Dual PHY MIPI C-PHY℠/D-PHY℠

- Sharing of the serial interface pins
- All D-PHY blocks are re-used for the C-PHY to minimize overhead
- Combo PHY provides the flexibility to support both PHY's using same pins with minimal overhead, while enhancing PPA



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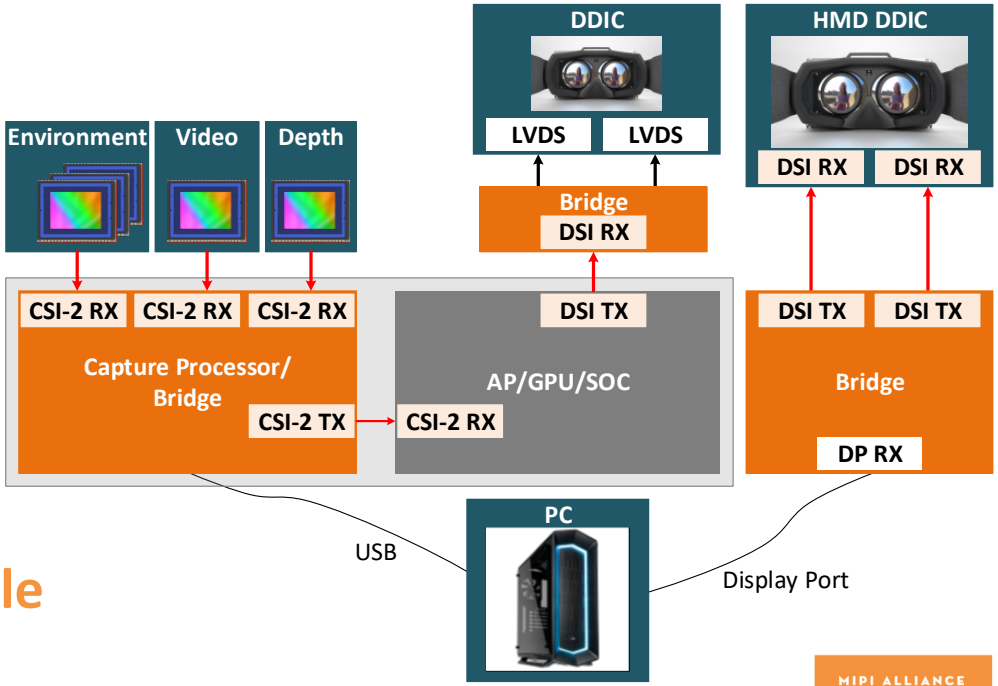
C-PHY℠/D-PHY℠ flexibility in XR System Considerations

- System Designers need to consider
  - Total resolution requirements
  - Application targeted
  - Number of ports
  - Number of lanes per port
  - Rate per lane

The flexibility of C-PHY/D-PHY makes it ideal solution for multiple applications and use-cases



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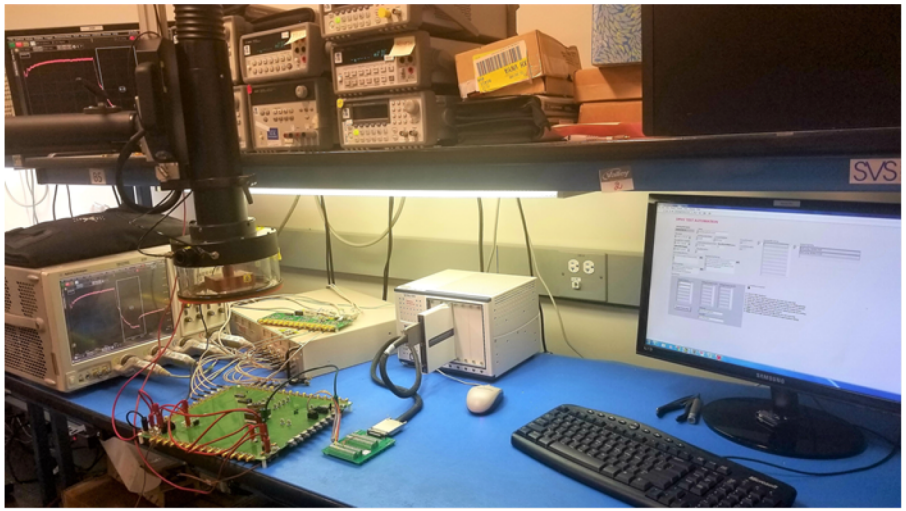
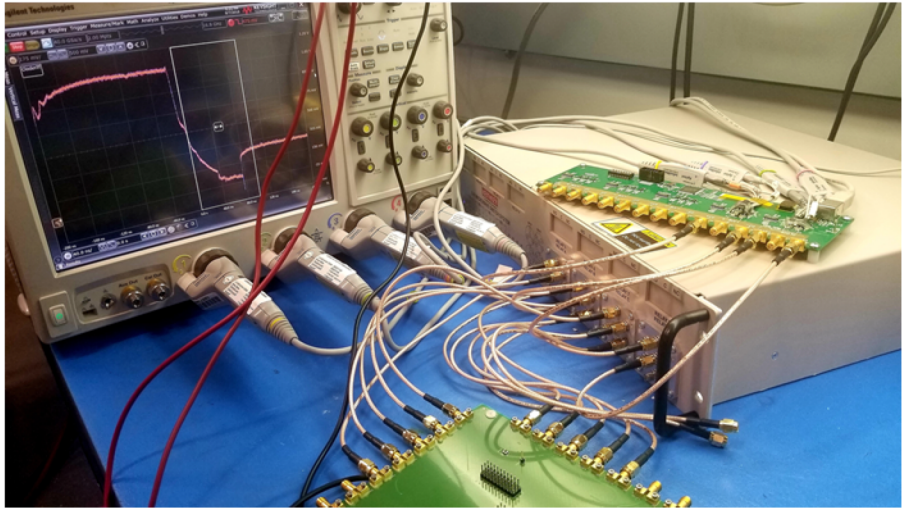
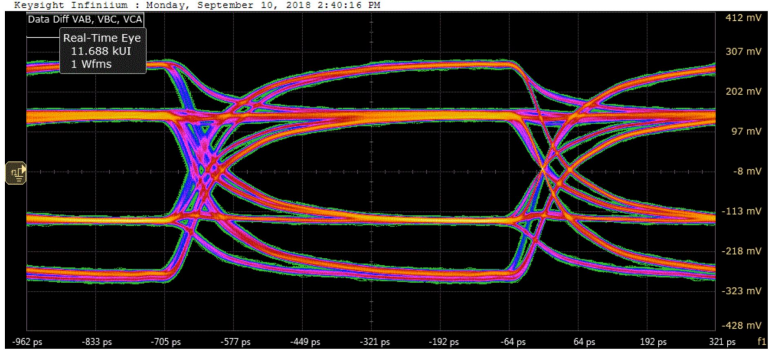
Silicon Results of VXR7200 MIPI Interfaces

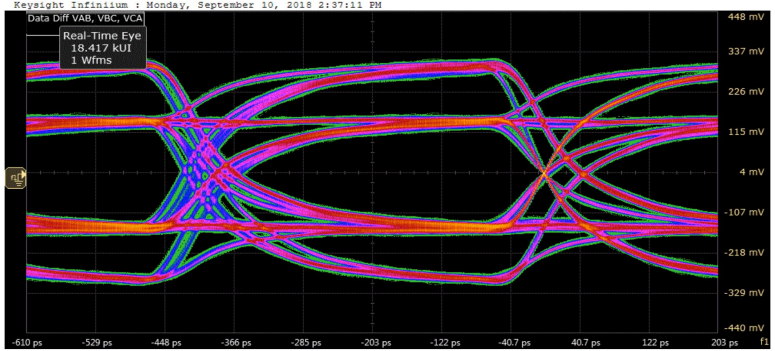
Test Bench Setups

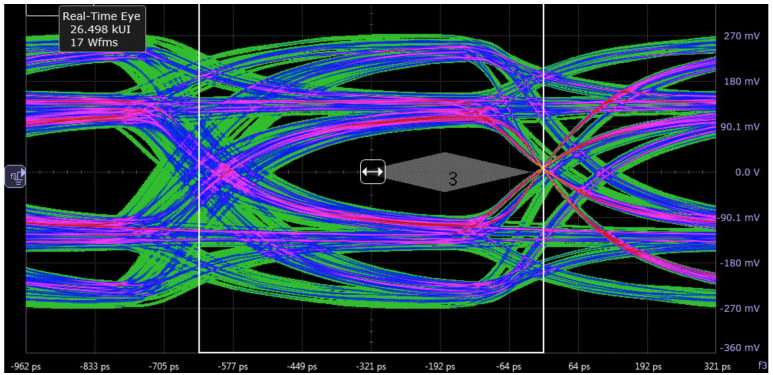


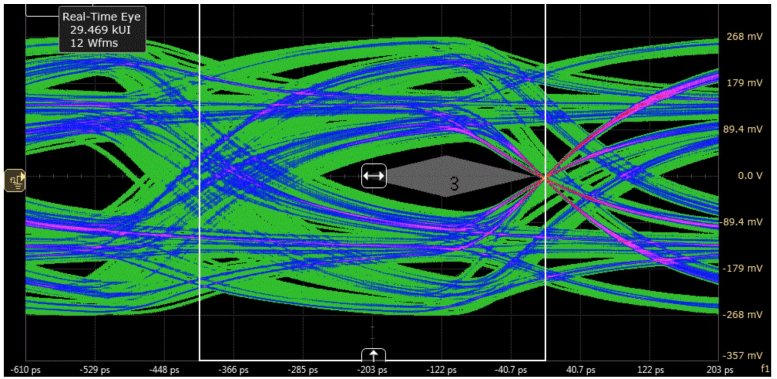


Silicon Results of VXR7200 C-PHY℠ Interface



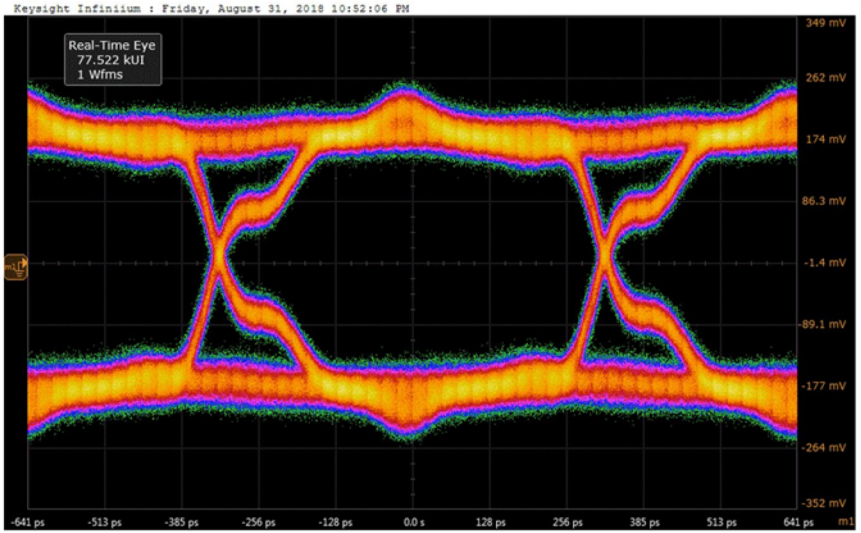




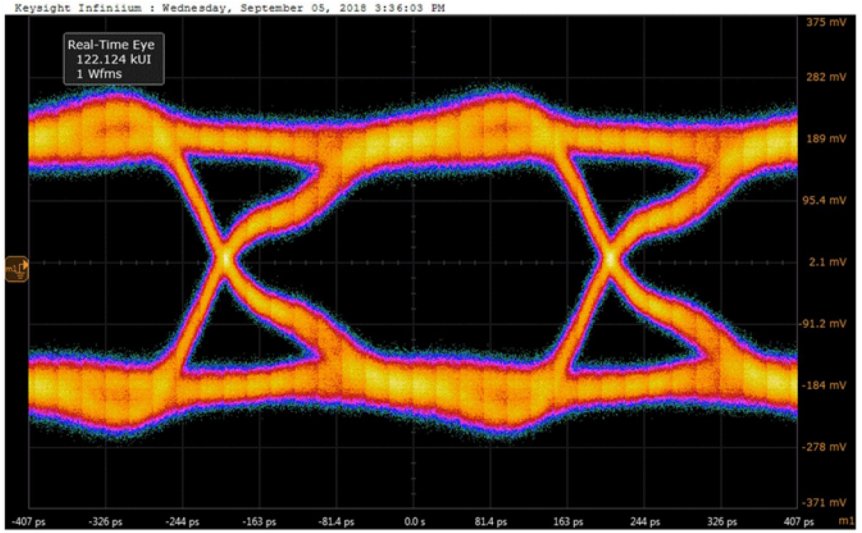


1.5Gsps **2.5Gsps**

Silicon Results of VXR7200 D-PHY℠ Interface



1.5Gbps



2.5Gbps

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Mixel's IP MIPI solution in XR

- C-PHY℠/D-PHY℠ Combo
- D-PHY℠ v1.1
- D-PHY℠ v1.2
- CSI-2℠
- DSI℠
- DSI-2℠

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Summary

- Combo C-PHY℠/D-PHY℠ offers a flexible and versatile solution for both system bring-up and application usage
- Mixel's C-PHY/D-PHY link speed makes it ideal for most display applications
- The Combo IP has been integrated into many end products by tier-one SOC, Display and Sensor vendors, several in XR applications
- Mixel's C-PHY/D-PHY are available in multiple configurations and Silicon proven in multiple nodes and foundries
- Synaptics achieved first time silicon success integrating Mixel's C-PHY/D-PHY into VXR7200

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Q&A

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ADDITIONAL RESOURCES

- Demystifying MIPI C-PHY / D-PHY Subsystem - Tradeoffs, Challenges, and Adoption
  https://www.chipestimate.com/Demystifying-MIPI-C-PHY--DPHY-Subsystem-Tradeoffs-Challenges-and-Adoption-/Mixel/Technical-Article/2018/04/24
- Synaptics' New Virtual Reality Display Driver and VR Bridge Provide Ultimate User Experience for Emerging Head-Mounted Displays
  https://globenewswire.com/news-release/2018/08/28/1557502/0/en/Synaptics-New-Virtual-Reality-Display-Driver-and-VR-Bridge-Provide-Ultimate-User-Experience-for-Emerging-Head-Mounted-Displays.html
- Synaptics chip paves the way for dual 2K VR headsets with 1,000 PPI
  https://venturebeat.com/2018/08/28/synaptics-chip-paves-the-way-for-dual-2k-vr-headsets-with-1000-ppi/
- MIPI DevCon 2016: Implementing MIPI C-PHY
  https://www.slideshare.net/MIPI-Alliance/mipi-devcon-2016-implementing-mipi-cphy

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