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Troubleshooting MIPI M-PHY® Link and Protocol Issues

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Objective

- This presentation is intended to help MIPI UniPro®/UFS developers to find the root cause of problems more quickly by providing tips for debugging MIPI M-PHY® based devices.

Welcome in Korean

MIPI Technologies

Physical Layer Interconnects

- High Speed Interconnects
  - MIPI M-PHY®
    - MIPI UniPro®/UniPort
      - Camera (Unipro), Storage (UniPro), Modem, Interchip
  - MIPI D-PHY(SM)
  - MIPI C-PHY(SM)
    - Camera, Display
  - MIPI A-PHY(SM)
    - Automotive applications
- Low Speed Interconnects
  - SLIMBus®
    - Audio
  - SoundWire®
    - Audio
  - CMOS I/O
    - Chip to Chip

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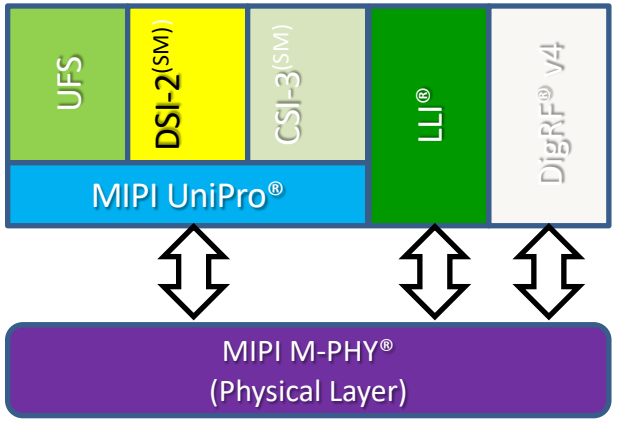
MIPI M-PHY® Protocols

- M-PHY® protocols are used based on interface used in each application.
- Multiple protocols can be used in a single device.



Why MIPI M-PHY®?

From the MIPI M-PHY® Specification V4.0:

"Mobile devices face increasing bandwidth demands for each of its functions as well as an increase of the number of functions integrated into the system. This requires wide bandwidth, low-pin count (serial) and highly power-efficient (network) interfaces that provides sufficient flexibility to be attractive for multiple applications, but which can also be covered with one physical layer technology. MIPI M-PHY® is the successor of MIPI D-PHY(SM), requiring less pins and providing more bandwidth per pin (pair) with improved power efficiency."

MIPI M-PHY® Data Rates

- LS-MODE
  - Gears 0-7
- HS-MODE
  - Gears 1-4
- All Modules (Host and Device) must support LS
  - Default for PWM is Gear1 3-9Mbs
  - Each Gear supports 2x higher speeds
  - one GEAR below the default speed range (PWM-G0)
- HS-Mode is Optional
  - HS-MODE includes a default GEAR (HS-G1)
  - Optional High Speed GEARs (HS-G2 , HS-G3, HS-G4) at incremental 2x higher rates
  - Each GEAR includes two data rates for EMI mitigation reasons
    - E.g. HS-G1 supports 1.25 Gbps and 1.45 Gbps
  - These two data rates are known as A & B
- Support for a LS or a HS GEAR requires support for all GEARs below

MIPI M-PHY® HS Gear 4

- Doubling of the Data Rate from HS-Gear3 to HS-Gear4

Table 11 HS-BURST: RATE Series and GEARs

RATE A-series (Mbps)	RATE B-series[1] (Mbps)	High-Speed GEARs
1248	1457.6	HS-G1 (A/B)
2496	2915.2	HS-G2 (A/B)
4992	5830.4	HS-G3 (A/B)
9984	11660.8	HS-G4 (A/B)

1. *The B-series rates shown are not integer multiples of common reference frequencies 19.20 MHz or 26.00 MHz, but are within the tolerance range of 2000 ppm.*

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MIPI UniPro®

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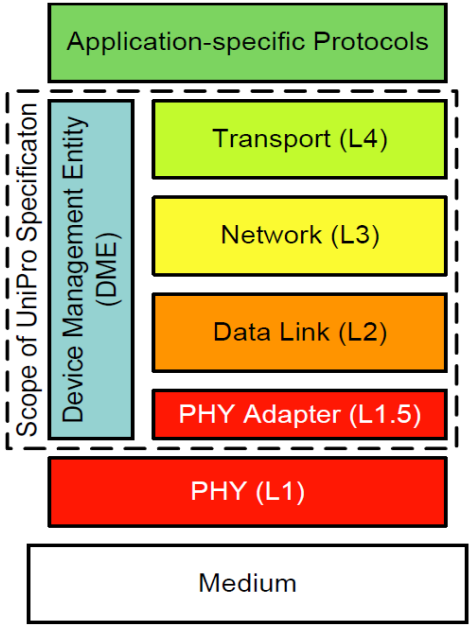
MIPI UniPro®

- MIPI specification to the define protoc
  between Devices that implement the
- This includes definitions of data struct
  Frames, used to convey information a
- Flow control, error handling, power ar
  connection services are also defined i
- UniPro version 1.61, the use of M-PHY
  chip interconnections



MIPI UniPro® L1.5 Protocol

- The L1.5 for MIPI M-PHY® automates a significant part of the required steps used for Power Modes control, utilizing an L1.5-to-L1.5 communication protocol known as PACP (PHY Adapter Control Protocol).
- PDUs (“PACP frames”) generated by L1.5 are multiplexed with the symbol stream received from L2 and can be recognized by a unique header pattern.

MIPI UniPro® L1.5 Power States and Power Modes

- The difference between Power States and Power Modes are as follows:
- An Application can set only a Power Mode, but cannot set a Power State
- An Application can get a Power Mode and get a Power State
  - the gettable value of a Power Mode simply reflects the value that was set
  - the gettable value of a Power State may change spontaneously when in FastAuto_Mode or SlowAuto_Mode

MIPI UniPro® PACP Capability Exchange

832	Sublink0	5.111370...	PACP_CAP_EXT1_ind		PWM-G1 x1
833	Sublink0	5.111398...	PACP_CAP_ind		PWM-G1 x1
840	Sublink1	5.111968...		PACP_CAP_EXT1_ind	PWM-G1 x1
842	Sublink1	5.112047...		PACP_CAP_ind	PWM-G1 x1

0	ESC_PA MK1	EscParm_PA 0x01	
2	PACP_FunctionId 0x0309		
4	THibern8 0x01	TMinActivate 0x6	Status 0xF
6	TAdvHibern8 0x01	TAdvMinActivate 0xA	RxAdvGranularity 0x4
8	MinRxTrailingClocks 0x2E	RxPwmBurstClosureLength 0x1F	
10	RxLsPrepareLength 0x0D	RxPwmG6G7SyncLength 0x00	
12	RxHsG1PrepareLength 0x0F	RxHsG1SyncLength 0x48	
14	RxHsG2PrepareLength 0x0F	RxHsG2SyncLength 0x49	
16	RxHsG3PrepareLength 0x0F	RxHsG3SyncLength 0x4A	
18	Reserved [31:16] 0xffff		
20	Reserved [15:0] 0xffff		
22	CCITT CRC-16 0xDB44		

MIPI UniPro® Layer 1.5 Example – PACP_PWR_REQ

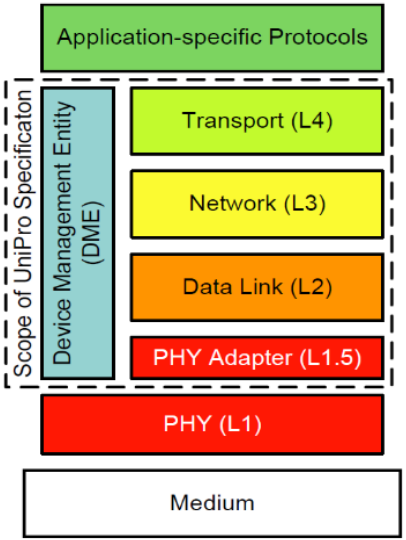
Used for power mode changes

▷ FRAME 696	3.947_976_272 s	0.000_203_592 s	LS		1	0	PACP	PACP_PWR_REQ		
▷ FRAME 706	3.948_213_046 s	0.000_219_178 s	LS		1	0			PACP	PACP_PWR_CNF

EscParam_PA	0x01
PACP_FunctionId	0x010E : PACP_PWR_REQ
DevId	0x00
▽ Flags	0x36
Scrambling request	0x0 : Not requested
UserDataValid	0x1 : Valid
HS Series	0x1 : Series B
LINE-RESET request	0x0 : Not requested
PA_TxTermination	0x1 : Enable
PA_RxTermination	0x1 : Enable
TxMode	0x1 : Fast_Mode
TxLane	0x1 : 1 Lane
TxGear	0x1
RxMode	0x1 : Fast_Mode
RxLane	0x1 : 1 Lane
RxGear	0x1
PAPowerModeUserData	0x00000000 00000000 00000000 FFFFFFFF FFFFFFFF FFFFFFFF
CRC-16	0x7A4E

MIPI UniPro® Layers

- L2 - The Data Link Layer provides reliable Links between a transmitter and a directly attached receiver
- L3 - Network Layer is to allow data to be routed to the proper destination in a networked environment.
- L4 - Transport Layer mechanisms allow a single physical Packet stream between two Devices to support multiple, independent, logical Packet streams or “Connections”.



16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	ESC_DL								SOF			TC		Reserved		
0	L3s=1	DestDeviceID_Enc							L4s=1	DestCPortID_Enc					FCT	EOM
0	L4 Payload								L4 Payload							
0	L4 Payload								L4 Payload							
1	ESC_DL								EOF_EVEN			Frame Seq. Number				
0	CCITT CRC-16															

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Universal Flash Storage (UFS)
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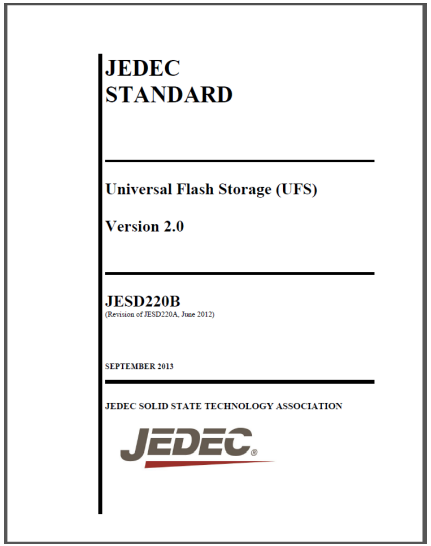
UFS – Universal Flash Storage

- Universal Flash Storage – JEDEC Standard JESD220B
- Universal Flash Storage (UFS) is a simple, high performance, mass storage device with a serial interface.
- It is primarily used in mobile systems, between host processing and mass storage memory devices.
- MIPI M-PHY® and MIPI UniPro® make up the interconnect for UFS
- UFS is architected on SCSI SAM
- UFS uses the command layers from SCSI SPC and SBC


JEDEC
STANDARD

Universal Flash Storage (UFS)

Version 2.0

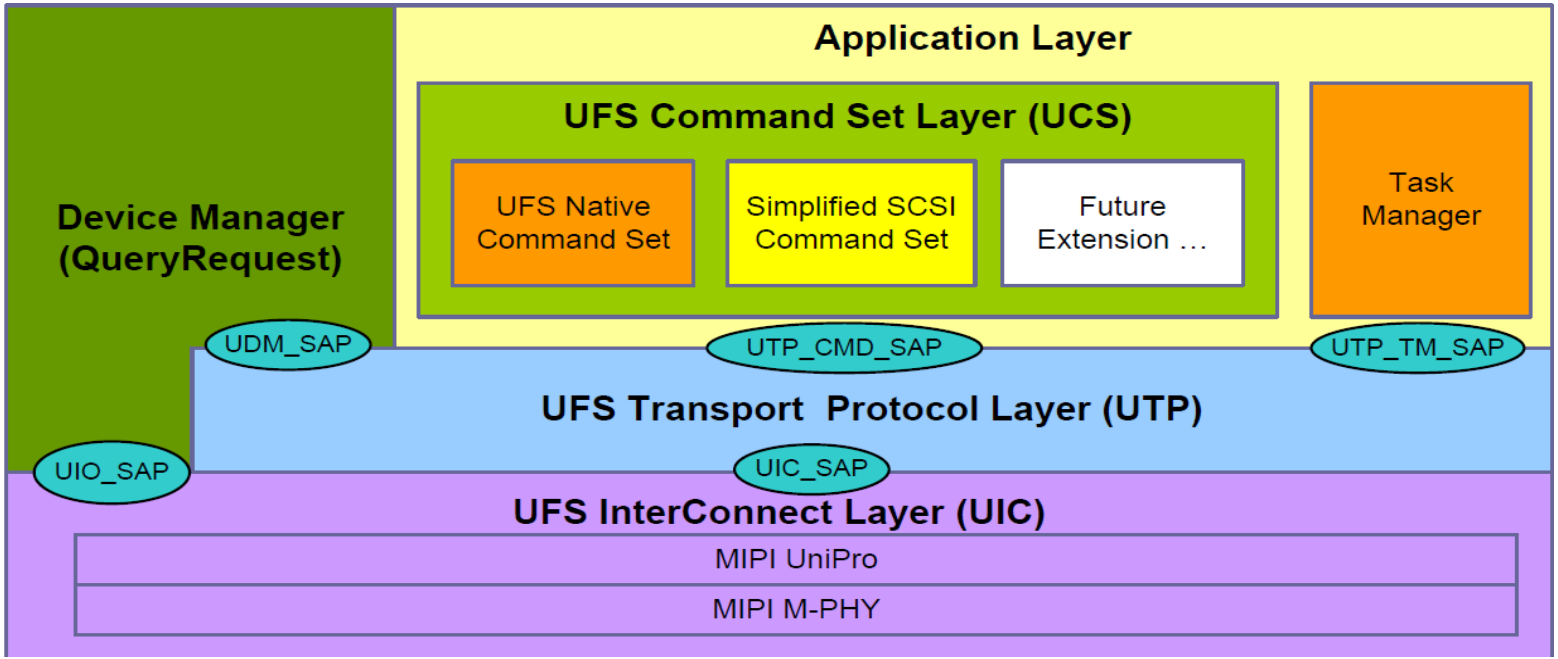
JESD220B
(Revision of JESD220A, June 2012)

SEPTEMBER 2013

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

JEDEC

UFS Architecture

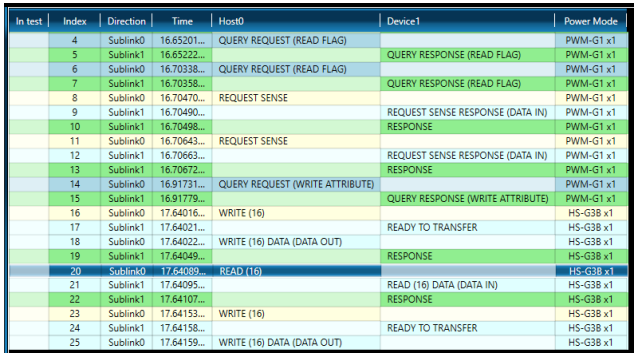


UFS Physical Layer Requirements

- UFS interface can support multiple lanes.
- Each lane consists of a differential pair.
- Basic configuration is based on one transmit lane and one receive lane.
- Optionally, a UFS device may support two downstream lanes and two upstream lanes. An equal number of downstream and upstream lanes shall be provided in each link.
  - Links must be symmetrical

Application Specific Protocol - UFS

- The application layer consists of the UFS Command Set layer (UCS), the device manager and the Task Manager
- The UCS will handle the normal commands like read, write, and so on.
- UFS may support multiple command sets.
- UFS is designed to be protocol agnostic. This version UFS standard uses SCSI as the baseline protocol layer.
- A simplified SCSI command set was selected for UFS.
- UFS Native command set can be supported when it is needed to extend the UFS functionalities.
- The Task Manager handles commands meant for command queue control.
- The Device Manager will provide device level control like Query Request and lower level link-layer control.



In test	Index	Direction	Time	Host0	Device1	Power Mode
	4	Sublink0	16.65201...	QUERY REQUEST (READ FLAG)		PWM-G1 x1
	5	Sublink1	16.65222...		QUERY RESPONSE (READ FLAG)	PWM-G1 x1
	6	Sublink0	16.70338...	QUERY REQUEST (READ FLAG)		PWM-G1 x1
	7	Sublink1	16.70358...		QUERY RESPONSE (READ FLAG)	PWM-G1 x1
	8	Sublink0	16.70470...	REQUEST SENSE		PWM-G1 x1
	9	Sublink1	16.70490...		REQUEST SENSE RESPONSE (DATA IN)	PWM-G1 x1
	10	Sublink1	16.70498...		RESPONSE	PWM-G1 x1
	11	Sublink0	16.70643...	REQUEST SENSE		PWM-G1 x1
	12	Sublink1	16.70663...		REQUEST SENSE RESPONSE (DATA IN)	PWM-G1 x1
	13	Sublink1	16.70672...		RESPONSE	PWM-G1 x1
	14	Sublink0	16.91731...	QUERY REQUEST (WRITE ATTRIBUTE)		PWM-G1 x1
	15	Sublink1	16.91779...		QUERY RESPONSE (WRITE ATTRIBUTE)	PWM-G1 x1
	16	Sublink0	17.64016...	WRITE (16)		HS-G3B x1
	17	Sublink1	17.64021...		READ TO TRANSFER	HS-G3B x1
	18	Sublink0	17.64022...	WRITE (16) DATA (DATA OUT)		HS-G3B x1
	19	Sublink1	17.64049...		RESPONSE	HS-G3B x1
	20	Sublink0	17.64089...	READ (16)		HS-G3B x1
	21	Sublink1	17.64095...		READ (16) DATA (DATA IN)	HS-G3B x1
	22	Sublink1	17.64107...		RESPONSE	HS-G3B x1
	23	Sublink0	17.64153...	WRITE (16)		HS-G3B x1
	24	Sublink1	17.64158...		READ TO TRANSFER	HS-G3B x1
	25	Sublink0	17.64159...	WRITE (16) DATA (DATA OUT)		HS-G3B x1

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SCSI Read Command

In test	Index	Direction	Time	Host0	Device1	
	4	Sublink0	16.65201...	QUERY REQUEST (READ FLAG)		
	5	Sublink1	16.65222...		QUERY F	
	6	Sublink0	16.70338...	QUERY REQUEST (READ FLAG)		
	7	Sublink1	16.70358...		QUERY F	
	8	Sublink0	16.70470...	REQUEST SENSE		
	9	Sublink1	16.70490...		REQUES	
	10	Sublink1	16.70498...		RESPON	
	11	Sublink0	16.70643...	REQUEST SENSE		
	12	Sublink1	16.70663...		REQUES	
	13	Sublink1	16.70672...		RESPON	
	14	Sublink0	16.91731...	QUERY REQUEST (WRITE ATTRIBUTE)		
	15	Sublink1	16.91779...		QUERY F	
	16	Sublink0	17.64016...	WRITE (16)		
	17	Sublink1	17.64021...		READY T	
	18	Sublink0	17.64022...	WRITE (16) DATA (DATA OUT)		
	19	Sublink1	17.64049...		RESPON	
	20	Sublink0	17.64089...	READ (16)		
	21	Sublink1	17.64095...		READ (1	
	22	Sublink1	17.64107...		RESPON	
	23	Sublink0	17.64153...	WRITE (16)		HS-G3B x1
	24	Sublink1	17.64158...		READY TO TRANSFER	HS-G3B x1
	25	Sublink0	17.64159...	WRITE (16) DATA (DATA OUT)		HS-G3B x1

Packet Decode

Packet: 20, Host0, READ (16)

8 | 16 | 32

Byte	+0			+1						
0	HD 0x0	DD 0x0	Transaction Code 0x1	Re... 0x0	R... 0x1	W... 0x0	Reserve... 0x0	CP 0x0	ATTR 0x0	
2	LUN 0x00			Task Tag 0x00						
4	IID 0x0		Command Set Type 0x0	Reserved (byte 5) 0x00						
6	Reserved (byte 6) 0x00			Reserved (byte 7) 0x00						
8	EHS Length 0x00			Reserved (byte 9) 0x00						
10	Data Segment Length 0x0000									
12	Expected Data Transfer Length [31:16] 0x0000									
14	Expected Data Transfer Length [15:0] 0x1000									
16	Operation Code 0x88			RDPROTECT 0x0	DPO 0x0	FUA 0x0	RE... 0x0	FU... 0x0	O... 0x0	
18	LOGICAL BLOCK ADDRESS [63:48]									

SCSI Write Command

In test	Index	Direction	Time	Host0	Device1
	0	Sublink0	4.186909...	NOP OUT	
	1	Sublink1	4.187109...		NOP IN
	2	Sublink0	4.188010...	QUERY REQUEST (SET FLAG)	
	3	Sublink1	4.188210...		QUERY R
	4	Sublink0	4.189164...	QUERY REQUEST (READ FLAG)	
	5	Sublink1	4.189364...		QUERY R
	6	Sublink0	4.240711...	QUERY REQUEST (READ FLAG)	
	7	Sublink1	4.240910...		QUERY R
	8	Sublink0	4.242537...	REQUEST SENSE	
	9	Sublink1	4.242737...		REQUES
	10	Sublink1	4.242817...		RESPON
	11	Sublink0	4.244950...	REQUEST SENSE	
	12	Sublink1	4.245155...		REQUES
	13	Sublink1	4.245235...		RESPON
	14	Sublink0	4.457277...	QUERY REQUEST (WRITE ATTRIBUTE)	
	15	Sublink1	4.457761...		QUERY RESPONSE (WRITE ATTRIBUTE)
	16	Sublink0	5.176648...	WRITE (16)	

Packet Decode

Packet: 16, Host0, WRITE (16) — 8 | 16 | 32

Byte	+0	+1
0	H... 0... / D... 0... / Transaction Code 0x1	R... 0... / R... 0... / W... 0... / Rese... 0x0 / CP 0... / ATTR 0x0
2	LUN 0x00	Task Tag 0x00
4	IID 0x0 / Command... 0x0	Reserved (byte 5) 0x00
6	Reserved (byte 6) 0x00	Reserved (byte 7) 0x00
8	EHS Length 0x00	Reserved (byte 9) 0x00
10	Data Segment Length 0x0000	
12	Expected Data Transfer Length [31:16] 0x0000	
14	Expected Data Transfer Length [15:0]	

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Debugging MIPI M-PHY®

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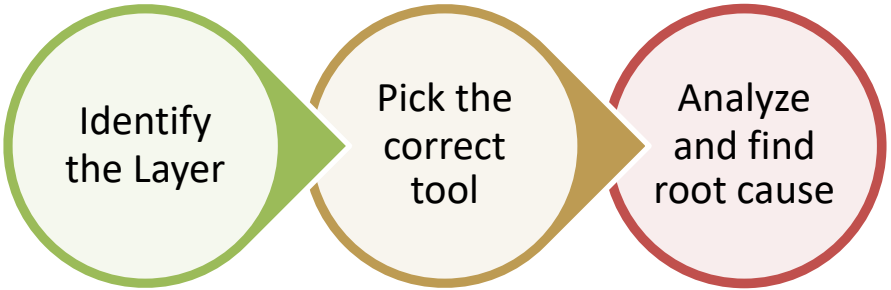
Debug process for Serial Protocols

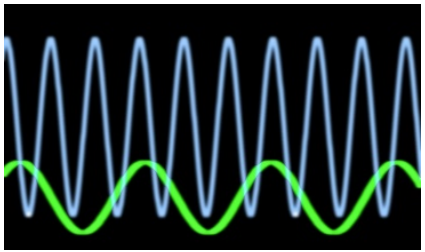


Debugging MIPI M-PHY®

- Typically MIPI M-PHY® production systems are chip to chip, no connector
- Development systems may have SMA connections between devices
- First challenge is to access link
- Probing Type:
  - SMA
  - Multi Lead
  - Midbus
- Check electrical first before debugging protocol problem

Using the correct tool

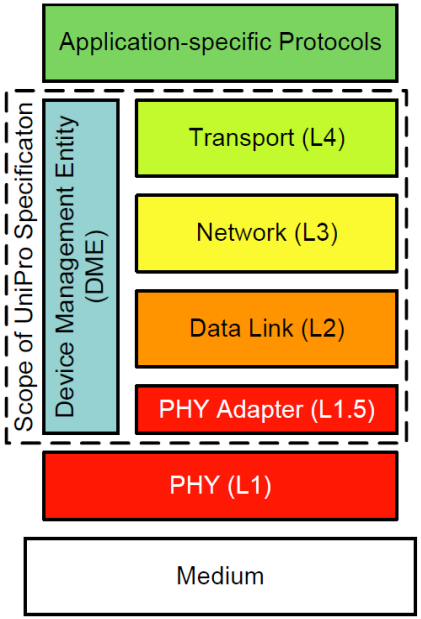
- Is problem related to Signal Integrity?
  - Are devices physically connected?
  - Are both devices providing MIPI M-PHY® compliant signaling?
  - Use an Oscilloscope to verify
- Is problem related to Connectivity
  - Is a link established between the 2 devices?
  - Is the data rate as expected?
  - Can software see the devices –
    - for UFS, can the storage be seen?
  - Use a Protocol analyzer to verify



SCSI		Request Sense
	CTRL	AFC
	UTP	DATA IN
CTRL		AFC
CTRL		AFC
	UTP	RESPONSE
CTRL		AFC
CTRL		AFC
SCSI		Read (10)

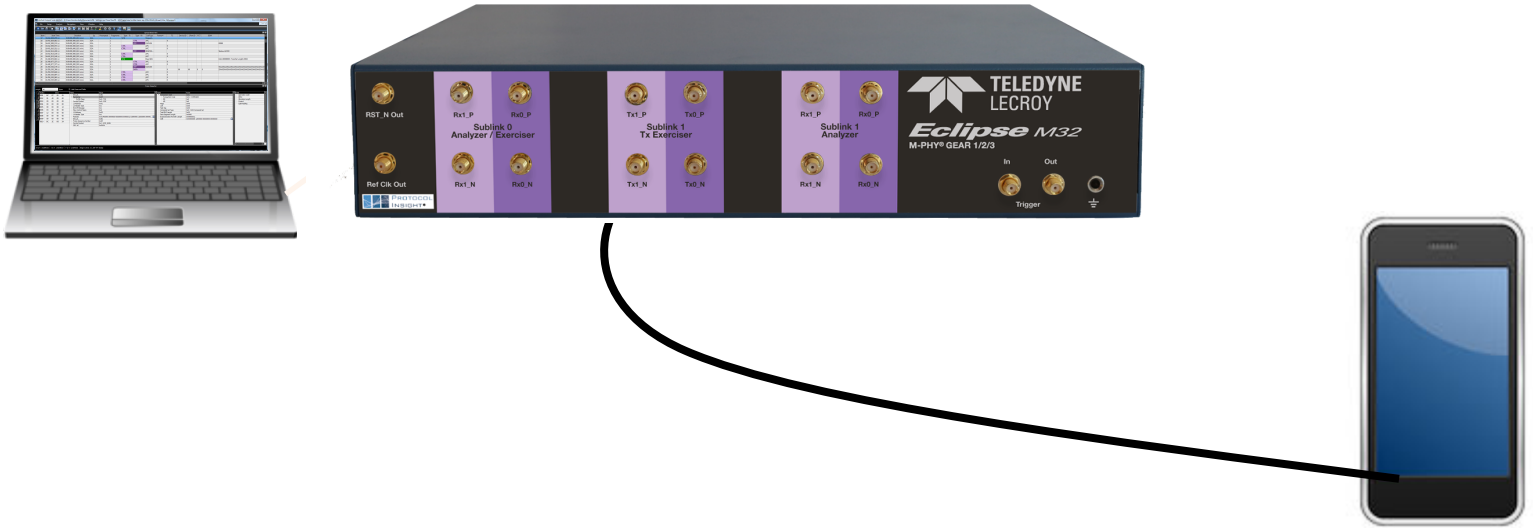
Which Layer is causing the problem?

- Same principle applies regardless of MIPI M-PHY® upper layer protocol
- Identify the layer
  - Performance?
  - Reliability?
  - Errors?



Protocol Analyzer sees nothing?

- Is there a signal present?
  - Connect the analyzer probe output to an Oscilloscope to verify.



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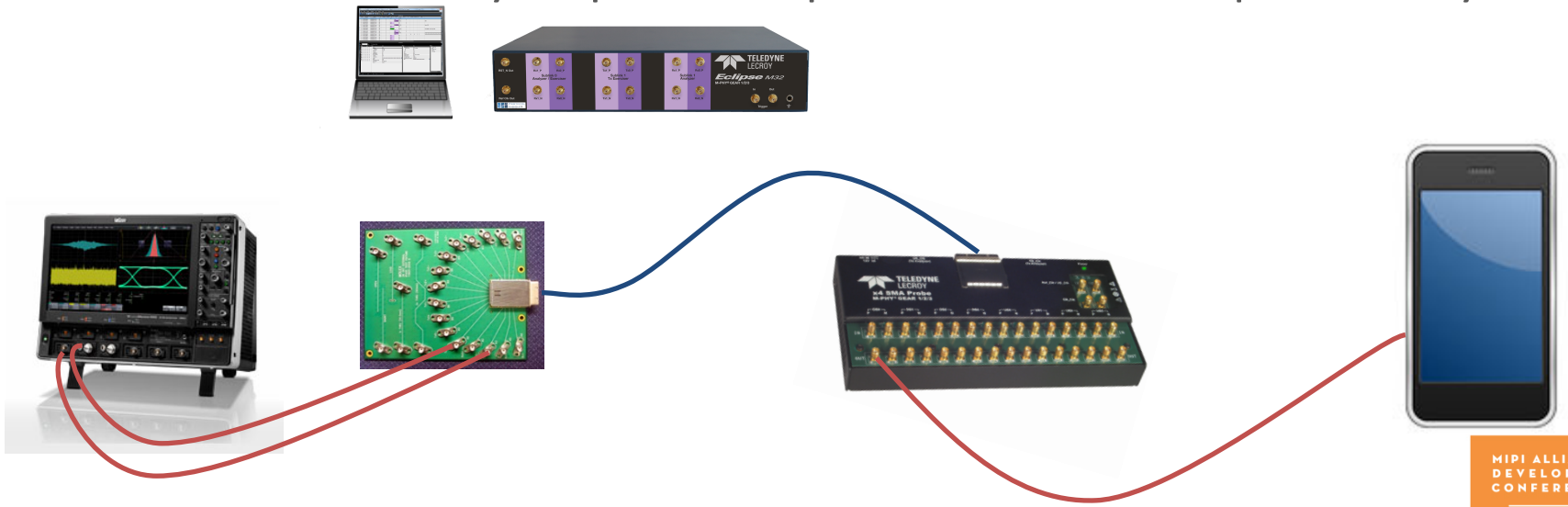


Protocol Issues – Look at upper layers

Index	Direction	Time	Host0	Device1	Power Mode	Error	MIBAttribute	Mibvalue
251	Sublink1	16.42751...		TRG_UPR2	PWM-G1 x1	NONE		
252	Sublink1	16.42751...		TRG_UPR2	PWM-G1 x1	NONE		
253	Sublink0	16.42751...	Filler		PWM-G1 x1	NONE		
254	Sublink1	16.42752...		TRG_UPR2	PWM-G1 x1	NONE		
255	Sublink0	16.42752...	TRG_UPR1		PWM-G1 x1	NONE		
256	Sublink1	16.42752...		TRG_UPR2	PWM-G1 x1	NONE		
257	Sublink0	16.42752...	Filler		PWM-G1 x1	NONE		
258	Sublink1	16.42752...		TRG_UPR2	PWM-G1 x1	NONE		
259	Sublink1	16.42752...		TRG_UPR2	PWM-G1 x1	NONE		
260	Sublink0	16.42752...	TRG_UPR1		PWM-G1 x1	NONE		
261	Sublink1	16.42753...		TRG_UPR2	PWM-G1 x1	NONE		
262	Sublink0	16.42753...	Filler		PWM-G1 x1	NONE		
263	Sublink1	16.42753...		TRG_UPR2	PWM-G1 x1	NONE		
264	Sublink1	16.42753...		TRG_UPR2	PWM-G1 x1	NONE		
265	Sublink0	16.42753...	TRG_UPR1		PWM-G1 x1	NONE		
266	Sublink1	16.42753...		TRG_UPR2	PWM-G1 x1	NONE		
267	Sublink0	16.42753...	Filler		PWM-G1 x1	NONE		
268	Sublink1	16.42753...		TRG_UPR2	PWM-G1 x1	NONE		
269	Sublink0	16.42754...	TRG_UPR1		PWM-G1 x1	NONE		
270	Sublink1	16.42754...		TRG_UPR2	PWM-G1 x1	NONE		
271	Sublink1	16.42754...		TRG_UPR2	PWM-G1 x1	NONE		
272	Sublink0	16.42754...	Filler		PWM-G1 x1	NONE		

In test	Index	Direction	Time	Host0	Device1	Power Mode
	4	Sublink0	16.65201...	QUERY REQUEST (READ FLAG)		PWM-G1 x1
	5	Sublink1	16.65222...		QUERY RESPONSE (READ FLAG)	PWM-G1 x1
	6	Sublink0	16.70338...	QUERY REQUEST (READ FLAG)		PWM-G1 x1
	7	Sublink1	16.70358...		QUERY RESPONSE (READ FLAG)	PWM-G1 x1
	8	Sublink0	16.70470...	REQUEST SENSE		PWM-G1 x1
	9	Sublink1	16.70490...		REQUEST SENSE RESPONSE (DATA IN)	PWM-G1 x1
	10	Sublink1	16.70498...		RESPONSE	PWM-G1 x1
	11	Sublink0	16.70643...	REQUEST SENSE		PWM-G1 x1
	12	Sublink1	16.70663...		REQUEST SENSE RESPONSE (DATA IN)	PWM-G1 x1
	13	Sublink1	16.70672...		RESPONSE	PWM-G1 x1
	14	Sublink0	16.91731...	QUERY REQUEST (WRITE ATTRIBUTE)		PWM-G1 x1
	15	Sublink1	16.91779...		QUERY RESPONSE (WRITE ATTRIBUTE)	PWM-G1 x1
	16	Sublink0	17.64016...	WRITE (16)		HS-G3B x1
	17	Sublink1	17.64021...		READY TO TRANSFER	HS-G3B x1
	18	Sublink0	17.64022...	WRITE (16) DATA (DATA OUT)		HS-G3B x1
	19	Sublink1	17.64049...		RESPONSE	HS-G3B x1
	20	Sublink0	17.64089...	READ (16)		HS-G3B x1
	21	Sublink1	17.64095...		READ (16) DATA (DATA IN)	HS-G3B x1
	22	Sublink1	17.64107...		RESPONSE	HS-G3B x1
	23	Sublink0	17.64153...	WRITE (16)		HS-G3B x1
	24	Sublink1	17.64158...		READY TO TRANSFER	HS-G3B x1
	25	Sublink0	17.64159...	WRITE (16) DATA (DATA OUT)		HS-G3B x1

MIPI UniPro® - Link Startup Sequence

- The Link Startup Sequence is a multi-phase handshake, which exchanges MIPI UniPro® trigger events to establish initial Link communication, in both directions, between two directly attached MIPI UniPro® Devices.

Link Startup Sequence

Table 13 Link Startup Sequence

Phase	PA Transmitter	PA Receiver
0	Continue to send TRG_UPR0 (all available Lanes)	Wait for TRG_UPR0 reception. Lane discovery (see ***Section 5.7.8.2)***
0b	Send two additional TRG_UPR0 (all available Lanes) Then proceed with phase 1	Ignore all data
1	Continue to send TRG_UPR1	Wait for TRG_UPR1 reception on all Lanes Re-align Lane numbering (***Section 5.7.8.3)***
2	Send two additional TRG_UPR1 Then proceed with phase 3	Ignore all data
3	Continue to send TRG_UPR2 on all Lanes	Wait for TRG_UPR2 reception on PHY RX Data Lane 0 • TRG_UPR2 (-> advance to phase 4) • TRG_UPR1 (-> ignore) • Others (-> ignore)
4	Send two additional TRG_UPR2 on all Lanes Then proceed with Phase 5	Ignore all data
5	Transfer Capabilities	Receive Capabilities and apply down grading
	Report to the DME using PA_LM_LINKSTARTUP.cnf_L that the Link Startup Sequence succeeded. Exit the Link Startup Sequence and enter SlowAuto_Mode.	

MIPI UniPro® - Link Startup Sequence

- Do both sides go through the Link Startup Sequence?

8104	Sublink1	57.83088...	Line-Reset		PWM-G1 x1	NONE
8107	Sublink1	58.22716...	TRG_UPR0		PWM-G1 x1	NONE
8115	Sublink1	58.22923...	TRG_UPR0		PWM-G1 x1	NONE
8119	Sublink0	58.23052...		Line-Reset	PWM-G1 x1	NONE
8123	Sublink1	58.23130...	TRG_UPR0		PWM-G1 x1	NONE
8129	Sublink0	58.23289...		TRG_UPR0	PWM-G1 x1	NONE
8137	Sublink1	58.23337...	TRG_UPR0		PWM-G1 x1	NONE
8144	Sublink0	58.23446...		TRG_UPR0	PWM-G1 x1	NONE
8152	Sublink1	58.23537...	TRG_UPR0		PWM-G1 x1	NONE
8159	Sublink0	58.23604...		TRG_UPR0	PWM-G1 x1	NONE
8160	Sublink0	58.23604...		TRG_UPR0	PWM-G1 x1	NONE
8161	Sublink0	58.23604...		TRG_UPR0	PWM-G1 x1	NONE
8162	Sublink0	58.23604...		TRG_UPR1	PWM-G1 x1	NONE
8163	Sublink0	58.23605...		TRG_UPR1	PWM-G1 x1	NONE
8164	Sublink0	58.23605...		TRG_UPR1	PWM-G1 x1	NONE

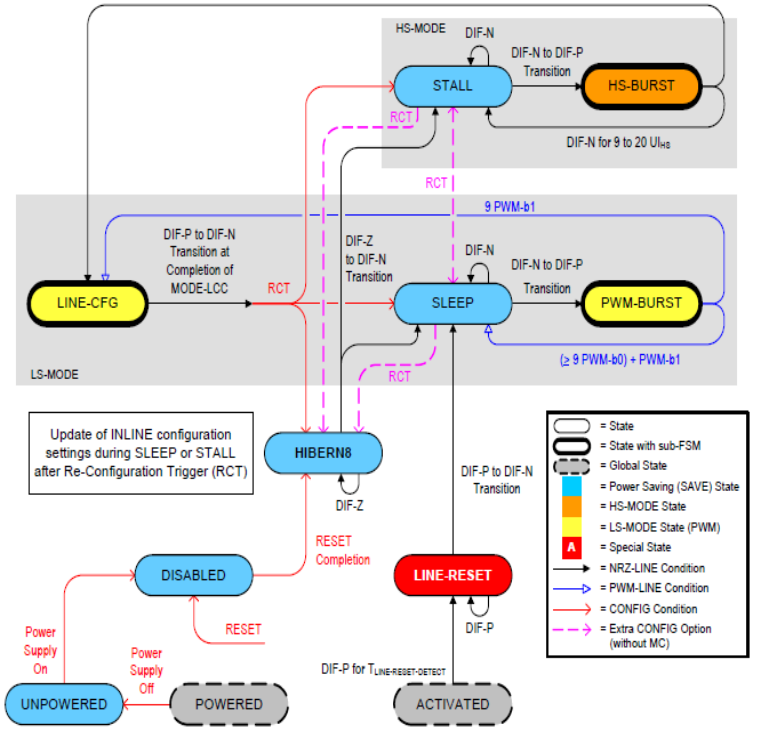
MIPI UniPro® – Link Startup Sequence

- Does the Link Startup Sequence Complete?

8925	Sublink1	58.23783...	TRG_UPR2		PWM-G1 x1	NONE
8926	Sublink1	58.23783...	TRG_UPR2		PWM-G1 x1	NONE
8927	Sublink1	58.23784...	TRG_UPR2		PWM-G1 x1	NONE
8928	Sublink1	58.23784...	TRG_UPR2		PWM-G1 x1	NONE
8929	Sublink1	58.23784...	TRG_UPR2		PWM-G1 x1	NONE
8930	Sublink1	58.23785...	TRG_UPR2		PWM-G1 x1	NONE
8939	Sublink0	58.23807...		PACP_CAP_EXT1_ind	PWM-G1 x1	NONE
8940	Sublink0	58.23810...		PACP_CAP_ind	PWM-G1 x1	NONE
8947	Sublink1	58.23867...	PACP_CAP_EXT1_ind		PWM-G1 x1	NONE
8949	Sublink1	58.23875...	PACP_CAP_ind		PWM-G1 x1	NONE
8960	Sublink0	58.23948...		AFC TC1	PWM-G1 x1	NONE
8961	Sublink0	58.23948...		AFC TC0	PWM-G1 x1	NONE
8970	Sublink1	58.24024...	AFC TC1		PWM-G1 x1	NONE
8972	Sublink1	58.24029...	AFC TC0		PWM-G1 x1	NONE

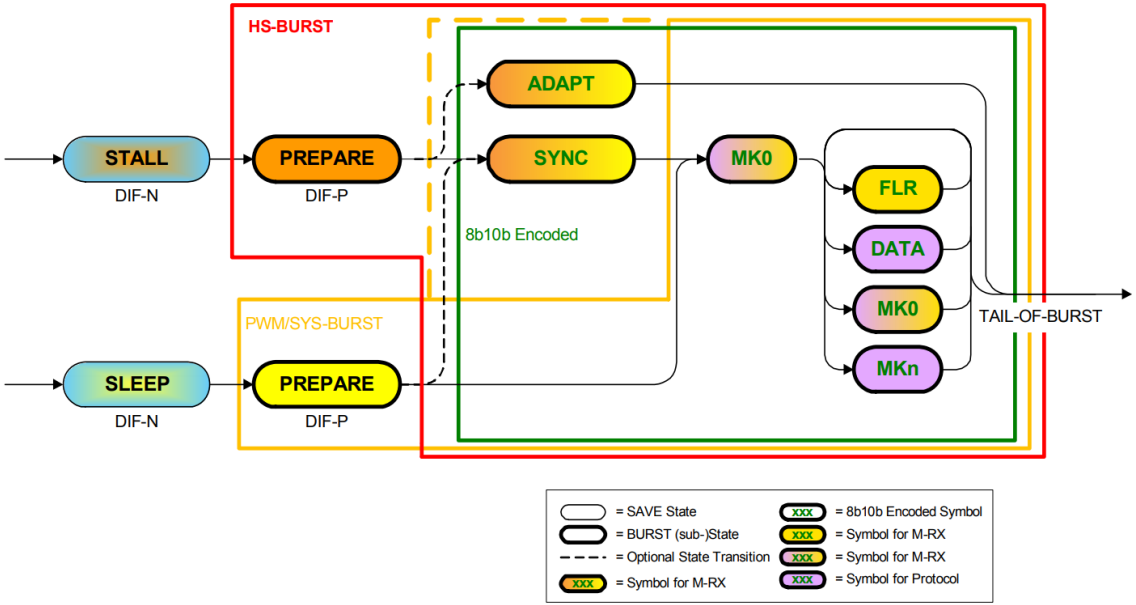
State Machine

- Two operating modes,
  - HS-MODE
  - LS-MODE
- A data transmission (BURST) state and a MODE-specific power saving (SAVE) state
- STALL is the SAVE state of HS-MODE
- SLEEP is the SAVE state of LS-MODE
  - HS-MODE: STALL, HS-BURST
  - LS-MODE (Type-I MODULE): SLEEP, PWM-BURST, LINE-CFG
  - LS-MODE (Type-II MODULE): SLEEP, SYS-BURST



Bursts

- HSG4 includes ADAPT state



Power Mode Change

- Are the Power Mode Changes happening as expected?
- Did the Link Startup Sequence Complete?
- Trigger on PACP_PWR_REQ to track Power mode changes

Index	Direction	Time	Host	Device	Power Mode	Error	RxGear	RxLane	RxMode	TxGear	TxLane	TxMode
1150	Sublink1	6.169753...	PACP_PWR_req		PWM-G1 x1	NONE	0x1	0x1	FastAuto_Mode (0x4)	0x1	0x1	FastAuto_Mode (0x4)
1156	Sublink0	6.170045...		PACP_PWR_cnf	PWM-G1 x1	NONE	0x1	0x1	FastAuto_Mode (0x4)	0x1	0x1	FastAuto_Mode (0x4)

UFS Initialization

- MIPI UniPro® Link Startup Sequence must complete before any UFS traffic can commence.

In test	Index	Direction	Time	Host	Device	Power Mode
	0	Sublink1	5.316020794000 s		NOP OUT	PWM-G1 x1
	1	Sublink0	5.316397266000 s	NOP IN		PWM-G1 x1
	2	Sublink1	5.383056086000 s		QUERY REQUEST (SET FLAG)	PWM-G1 x1
	3	Sublink0	5.383427540000 s	QUERY RESPONSE (SET FLAG)		PWM-G1 x1
	4	Sublink1	5.449256130000 s		QUERY REQUEST (READ FLAG)	PWM-G1 x1
	5	Sublink0	5.449674915000 s	QUERY RESPONSE (READ FLAG)		PWM-G1 x1

Summary

- Although device is a UFS controller you are dependent on MIPI UniPro® Link Startup Sequence
- Knowing this process will help you understand how to bring up the device
- Identify Lower Layer issues first, otherwise nothing else will work

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ADDITIONAL RESOURCES

- MIPI M-PHY® Specification v4.0
- MIPI MIPI UniPro® Specification v1.8
- JEDEC Spec JESD220C (UFS)

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