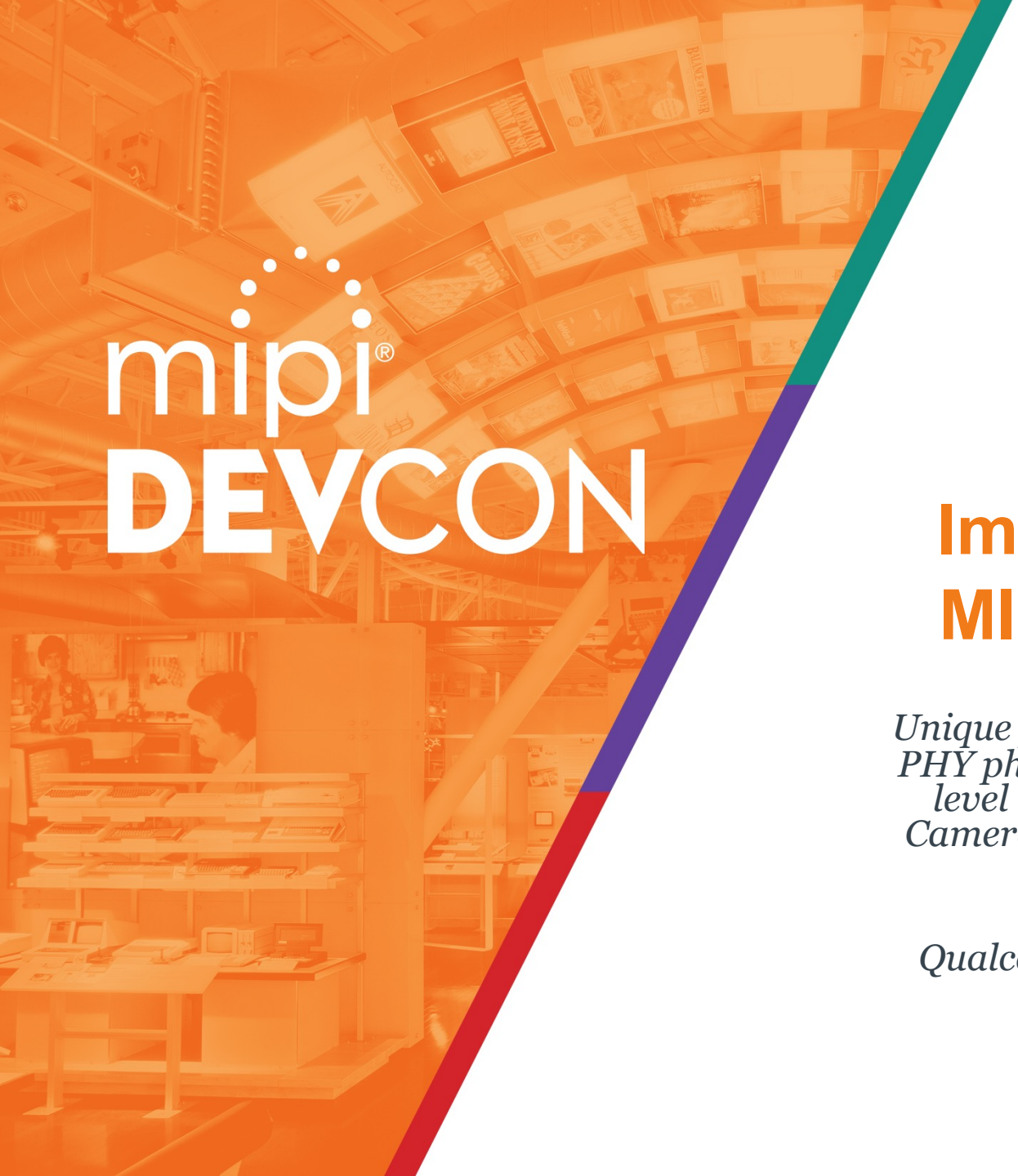


Implementing MIPI C-PHY℠

Unique properties of the MIPI C-PHY physical layer and system-level benefits and values for Camera and Display interfaces

George Wiley
Qualcomm Technologies, Inc.

MIPI C-PHY

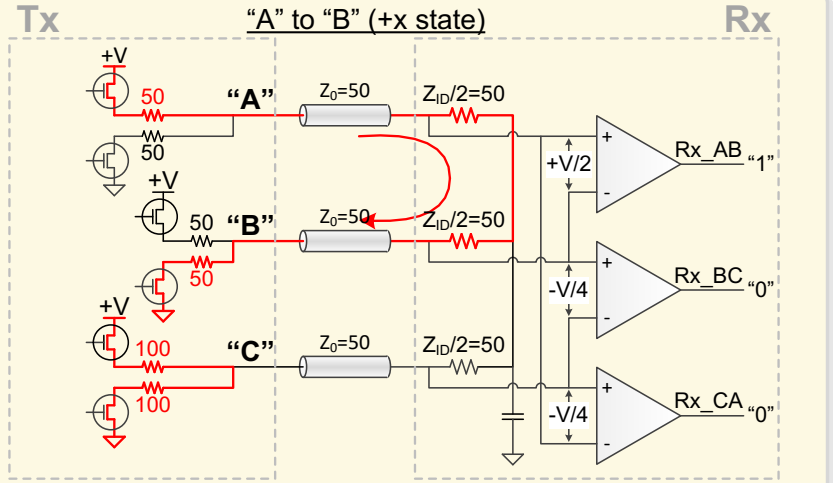
- At first glance it seems a bit… unusual!

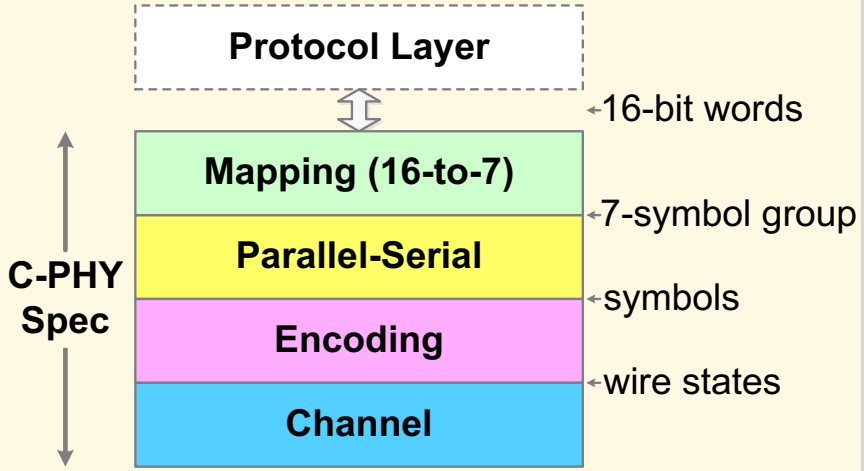
Summary

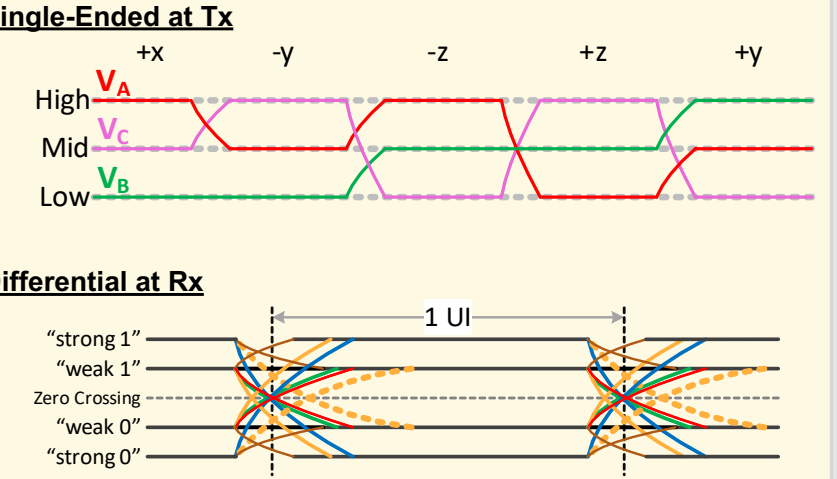
- MIPI C-PHY, Brief Overview.
- Unique properties of the physical layer
  - Some random but interesting tidbits about C-PHY
  - Why things are the way they are (beyond the scope of the specs)
  - (a little bit of “secret sauce”).
- MIPI C-PHY Benefits and Value for Camera and Display.
- Applications.
- Roadmap.

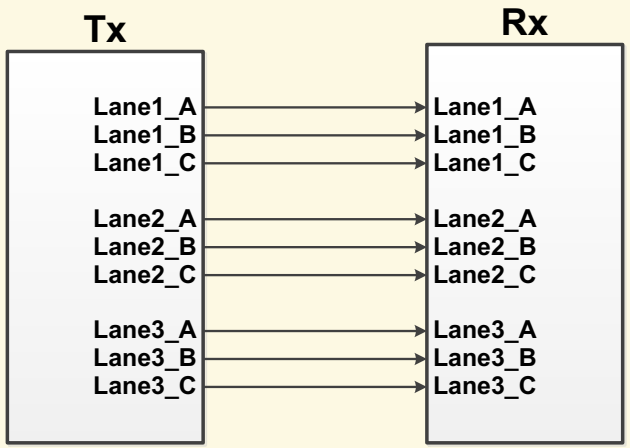
MIPI C-PHY Brief Overview

MIPI C-PHY Overview



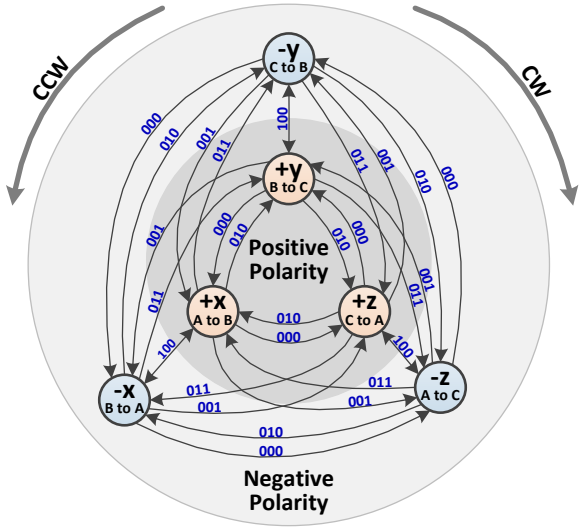






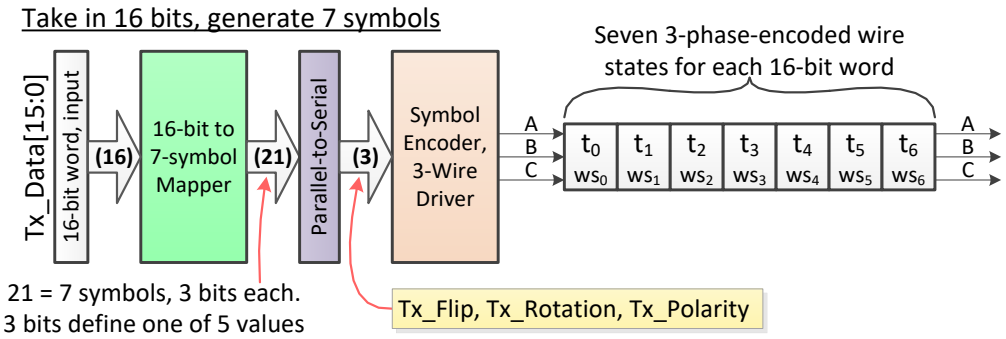
Encoding & Mapping

- 6 Wire States; 5 possible transitions from each.
- $\log_2(5) \cong 2.3219$ bits/symbol are possible, C-PHY uses $16 \div 7 \cong 2.2857$ bits/symbol

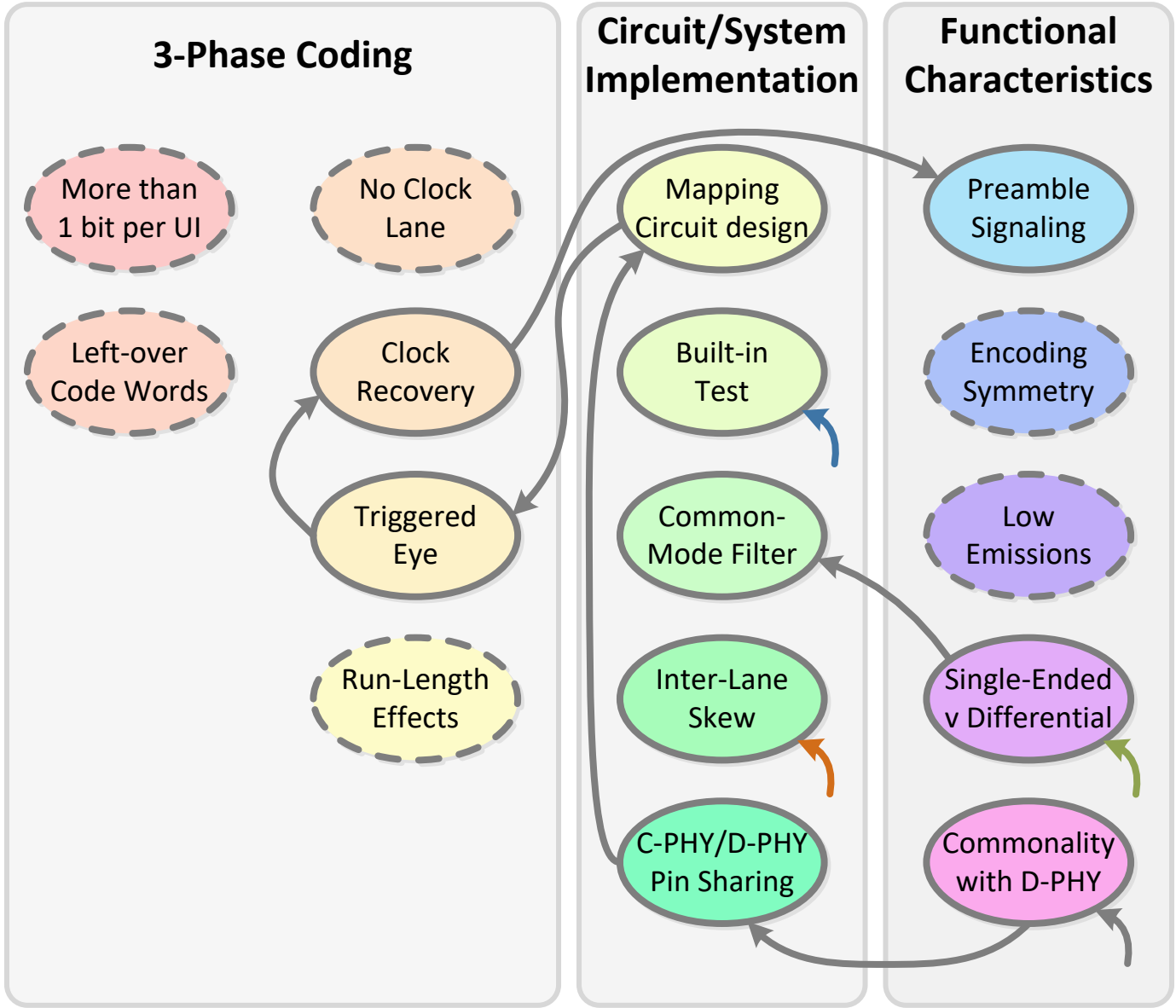


[Flip, Rotation, Polarity]

- Mapping converts 16-bit word to 7 symbols.
  - 16 bits $\Rightarrow 2^{16} = 65{,}535$ states, 7 symbols $\Rightarrow 5^7 = 78{,}125$ states.
  - 12,589 states left over; ≅0.0362 bits/symbol are wasted!
    - Actually, what's left over goes to good use! Will explain later.



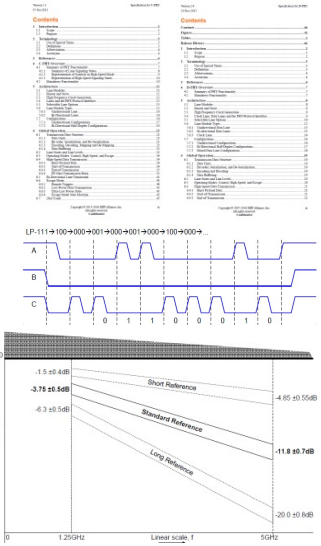
Unique Properties of the Physical Layer



MIPI C-PHY & MIPI D-PHY Similarities

Commonality with D-PHY

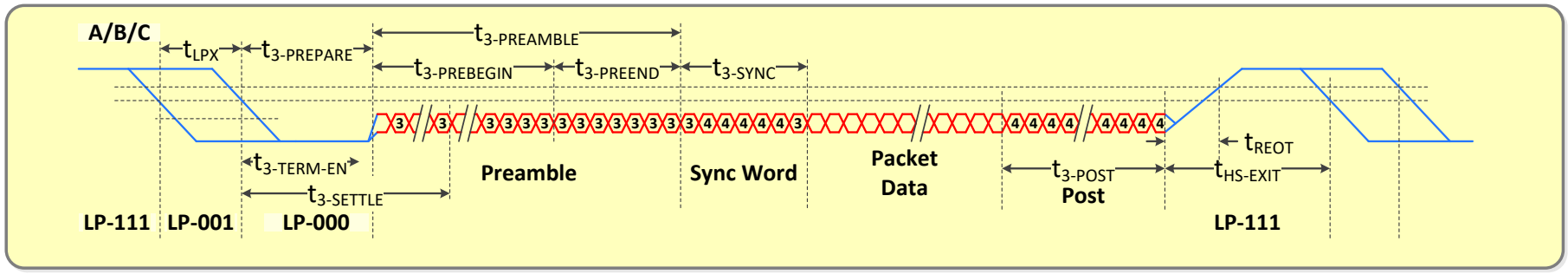
- Close cousins, there are a lot of similarities, and some differences.
- Things that are the same (or almost the same):
  - Document section #'s correspond to the same type of parameters/items.
    - The D-PHY spec was used as a template for the first C-PHY spec!
  - LP (Low-Power) Mode is identical, functional definition & electrical specs.
    - (C-PHY LP Mode has a 3rd wire, but it doesn't do much.)
  - Channel models are common between the specs
    - (Interconnect and Lane Configuration specs are nearly the same.)
  - PHY-Protocol Interface definition has a lot in-common.
    - (Many signals are defined using common language.)
  - Similar High-Speed Mode voltage levels.
    - A dual-mode C/D-PHY driver or receiver can be built to share the same pins.
- Things that are different:
  - High-Speed Data encoding is completely different.
  - High-Speed timing specs are unique to C-PHY encoding.

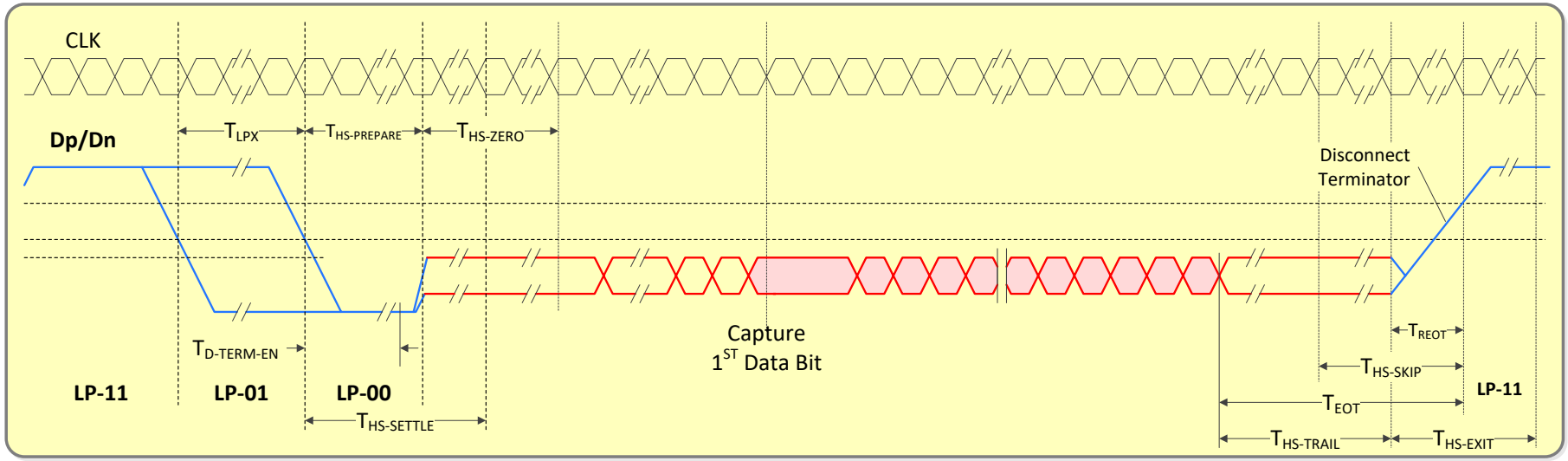


C-PHY & D-PHY Global Timing

Commonality with D-PHY

- Similar signaling going into and out of HS Mode.





C-PHY/D-PHY Pin Sharing

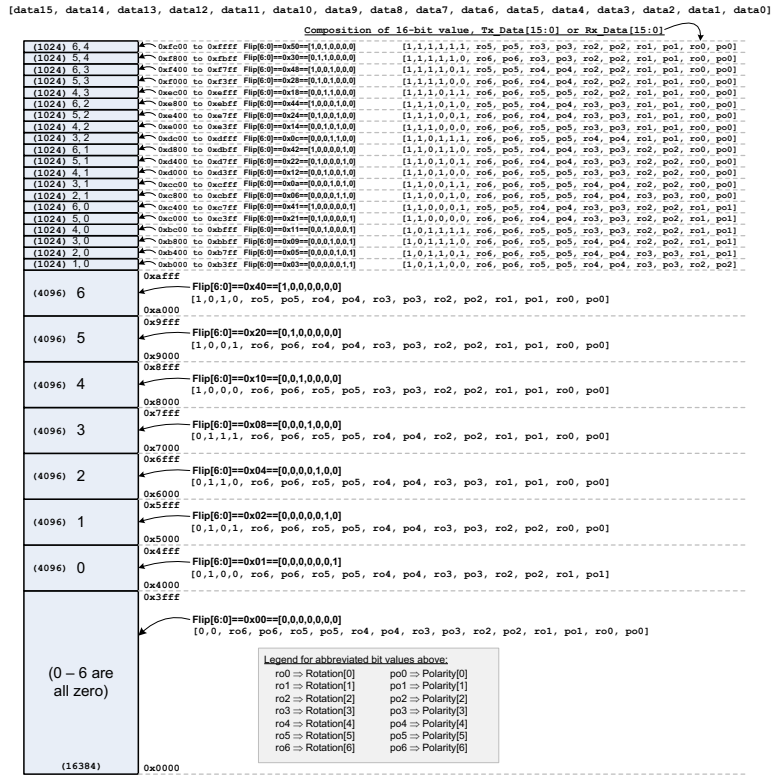
C-PHY/D-PHY Pin Sharing

- C-PHY & D-PHY can co-exist on the same AP pins.
  - Mode bit at system boot configures as either C-PHY or D-PHY mode.
- Electrical Specs are similar.
- Timing/encoding is completely different.
- Low-Power Modes in C-PHY & D-PHY are identical.

Mapping Function

Mapping Circuit design

- Looks really complicated, but it's not.
  - For a human: it's complicated. For a circuit implementation: it's easy.
- For human understanding, an intuitive mapping could have been:
  - A base-5 number representation. (But base-5 would be a more complex circuit.)
- The C-PHY Mapper implementation:
  - Has no arithmetic operations, no carry or look-ahead.
  - Reduces to simple combinatorial logic, no states.
  - Can be pipelined easily.
  - The spacing of unused code words is convenient for other functions. (a topic for another day)
  - A complete implementation using 4-to-1 muxes and small look-up table is provided in the spec.
  - Or just plug the diagram on the right into logic synthesis to create the RTL.



Why the Mapper?

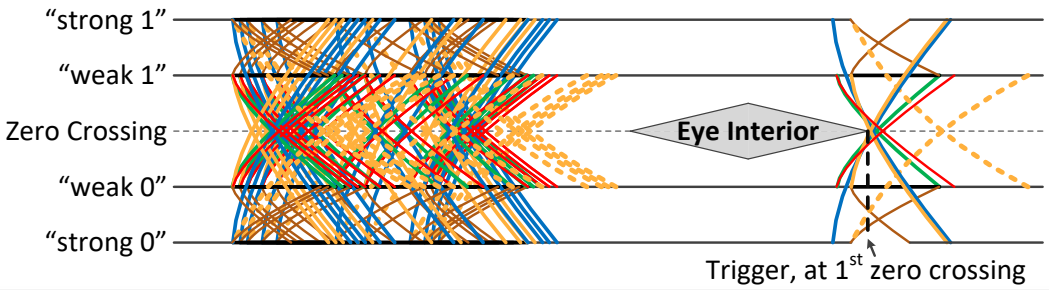
Mapping Circuit design

- Hypothetically, let's explore this…
- Assume we had used only 4 states per symbol instead of 5.
- Translation of symbols to words becomes trivial.
- Each symbol would encode 2 bits ⇒ 8 symbols represent 16 bits
  - Hypothetical case would be 8 symbols that represent 16 bits
  - Instead of 7 symbols that represent 16 bits
- Would have many more unused states & wasted capacity
  - $Log_2(5) – 2 \cong 0.3219$ bits/symbol would be lost;
  - Instead of $Log_2(5) - (16/7) \cong 0.0362$ bits/symbol currently unused.
- Increase link capacity by more than 14%, at the cost of:
  - Some digital circuits that perform the mapping function. A good tradeoff!

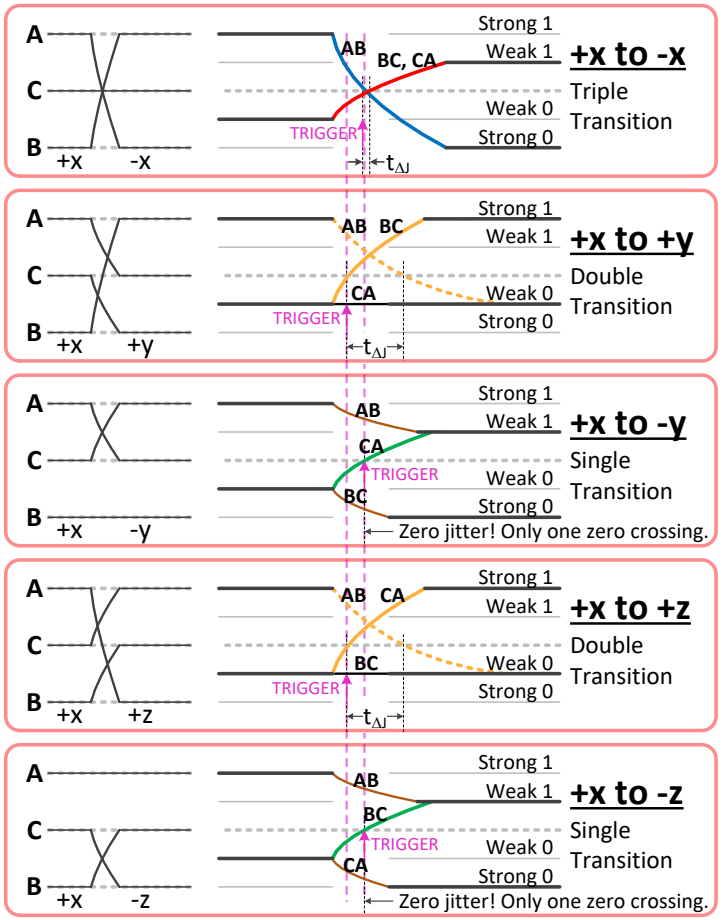
C-PHY Triggered Eye Concept

Triggered Eye

- Trigger at first zero-crossing of AB, BC or CA.
  - The right-most point of the eye interior aligned with the first zero crossing trigger point. (First Transition)
  - Capture the received data in the Rx just prior to the trigger point.
- 1, 2 or 3 Transitions at each UI boundary.
- When 2 or 3 Transitions, they are often staggered in time. Caused by:
  - 2-Transition case: Weak-to-Strong & Strong-to-Weak.
  - Slight differences in rise and fall times between the three signals of the lane (DCD), and ISI.
  - Slight differences in signal propagation times between the combinations of signal pairs received (e.g. A-B, B-C, and C-A).



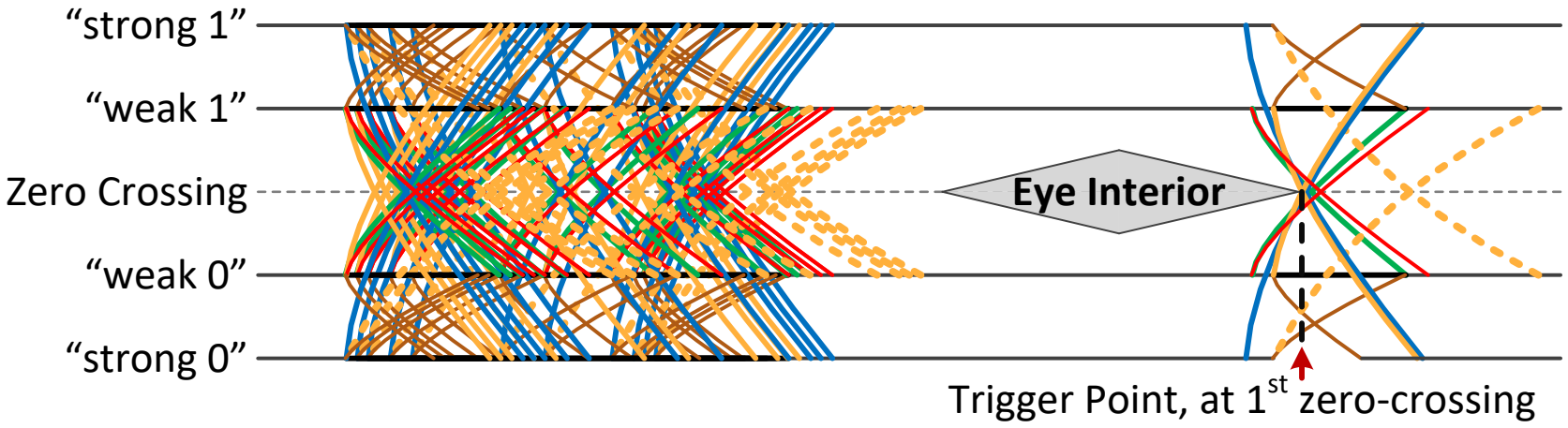
An "ideal" view: without ISI or DCD.



Symbol Clock Recovery

Clock Recovery

- Clock edge is at the first zero-crossing (the Trigger Point).
- Ignore subsequent edges in the same UI.
  - Zero-crossings following the first zero-crossing are ignored.
  - (For 2 or 3 Transition symbols, only the 1st transition is used for clock recovery.)
- Data is sampled just prior to the Trigger Point.

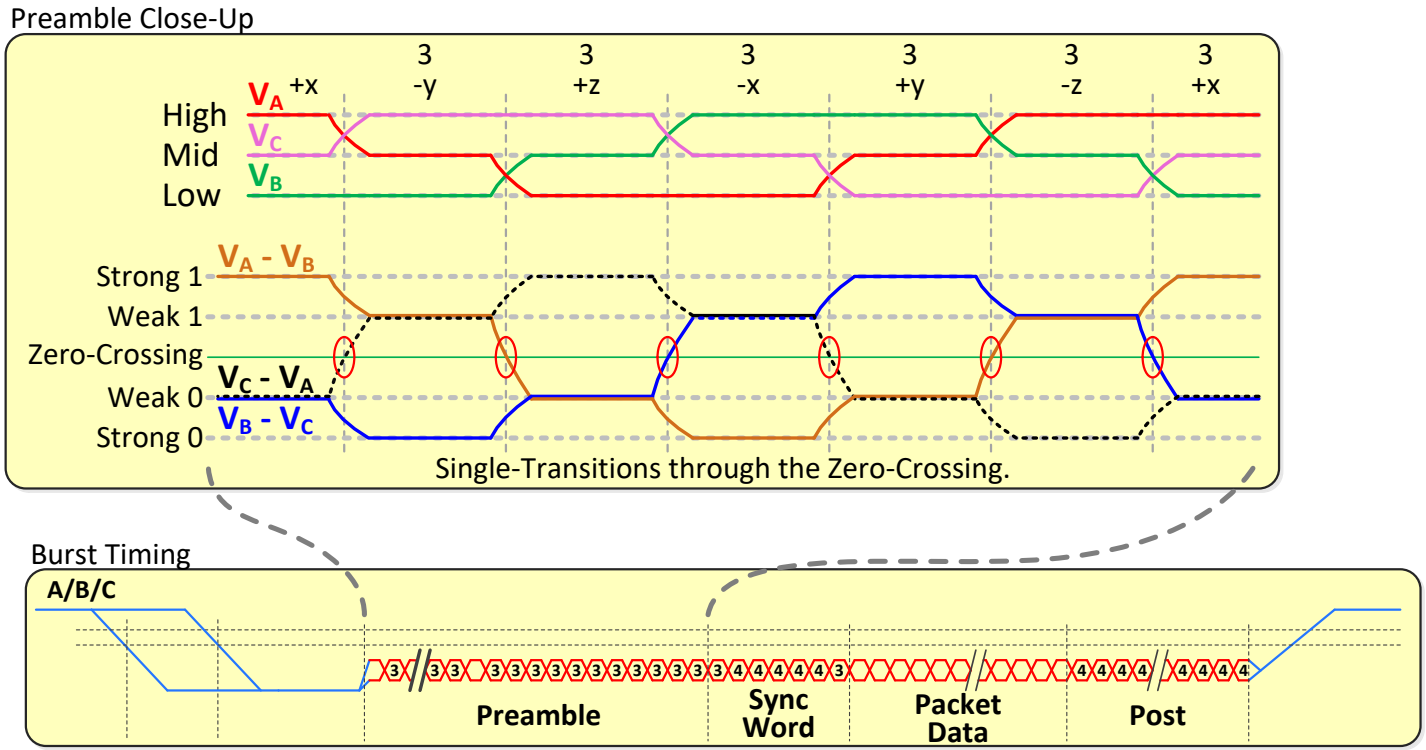


Recovered clock edge is at this Trigger Point.
Data is sampled just prior to the Trigger Point.

Preamble Signaling

Properties of the Preamble

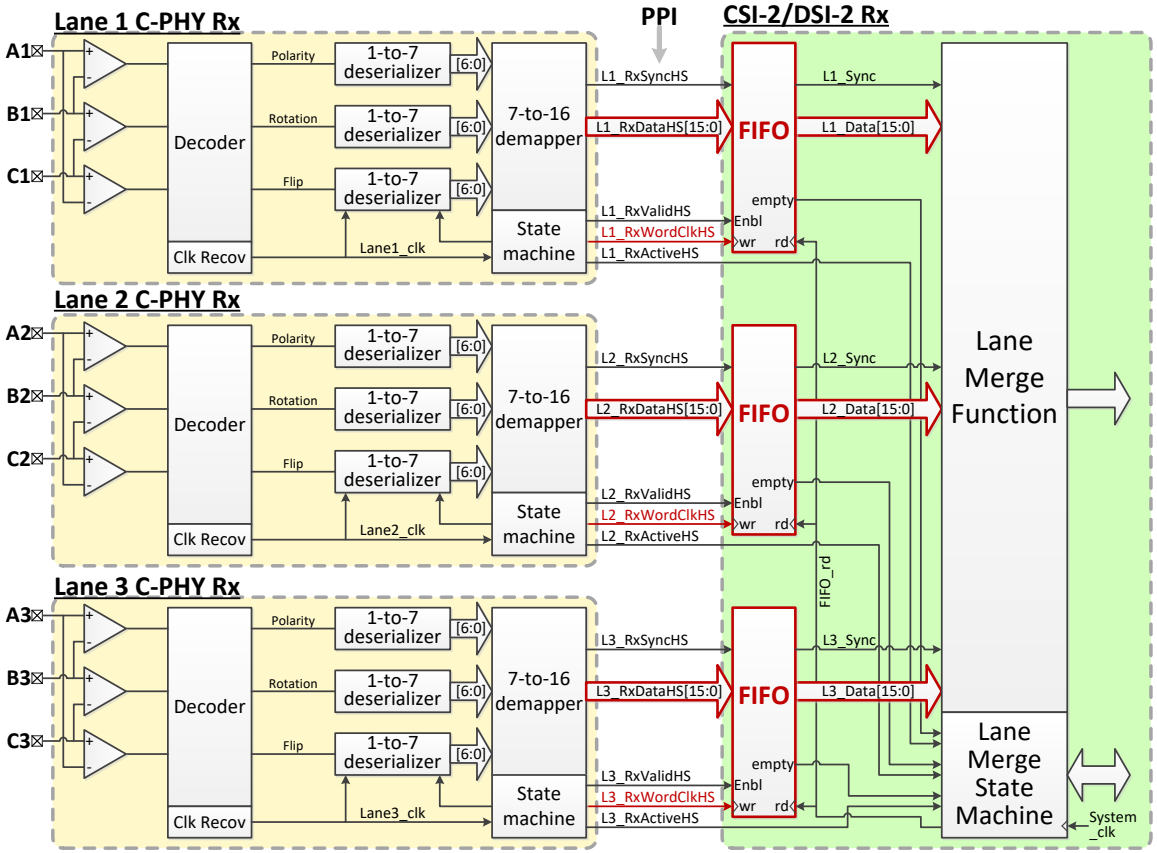
- The first field of the burst.
- All 3's. Single-transition symbols.
- Simplifies Clock Recovery start-up.



Inter-Lane Skew

Inter-Lane Skew Impact

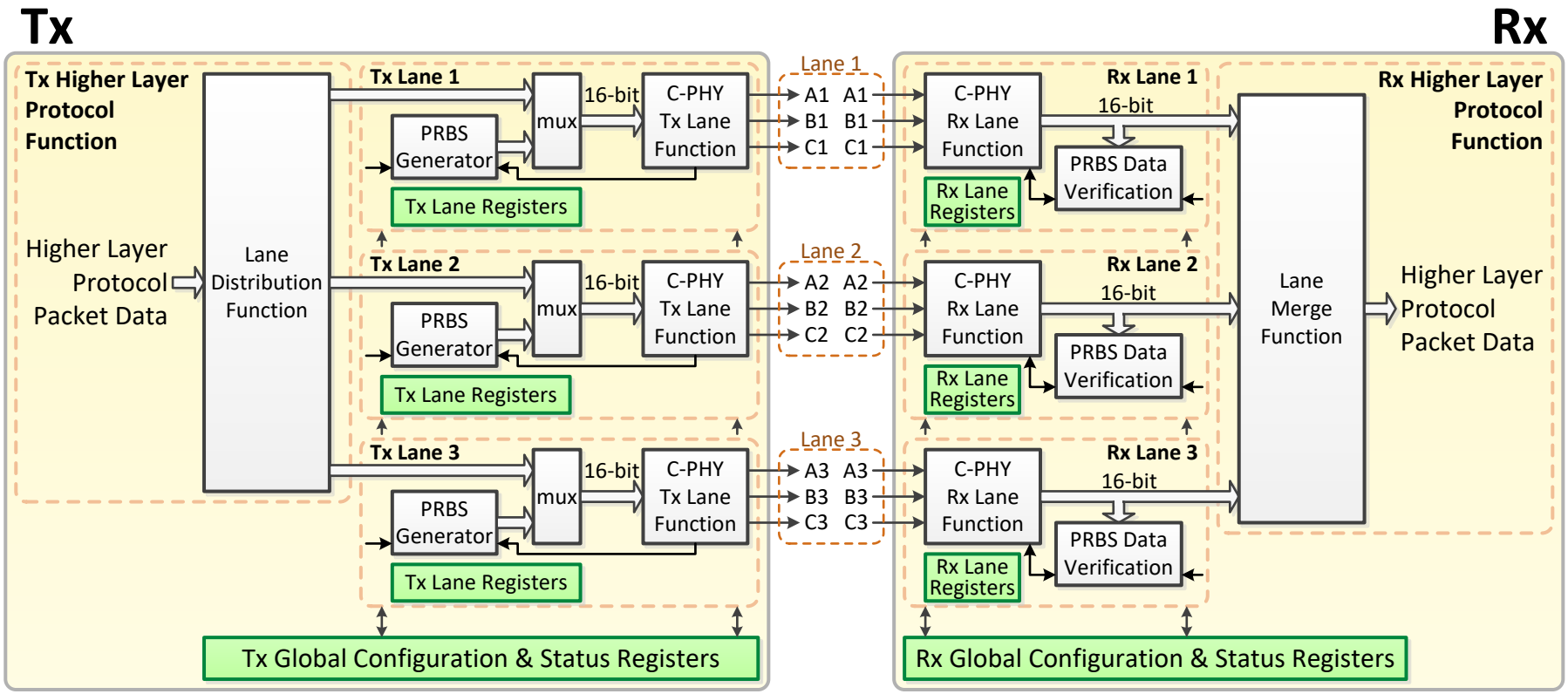
- Clock timing embedded in each Lane. Tolerant of Inter-Lane skew.
  - Small elastic buffer facilitates data alignment.
- Important characteristic for Lane grouping flexibility.



Built-in Test Capability

Built-in Test

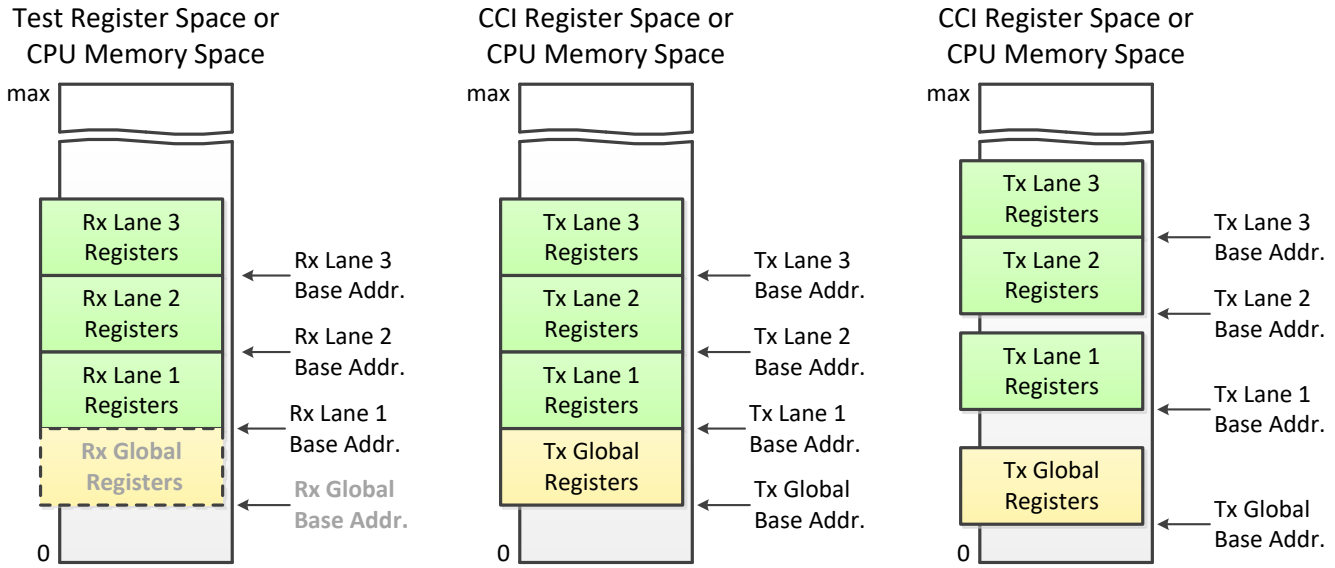
- 19 pages in the C-PHY spec dedicated to built-in test (of 140p total)
- Control/status register definitions, PRBS definitions, test data sequence definitions and examples.



Built-in Test Registers

Built-in Test

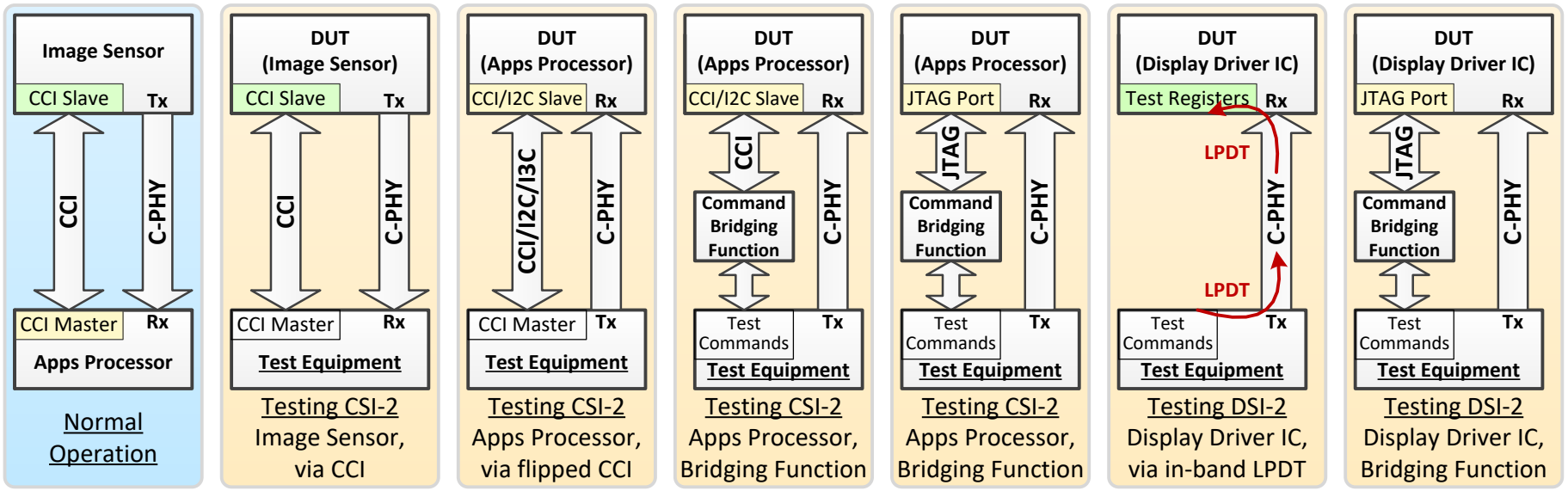
- Detailed Register Definitions, per-Lane and Global Registers
  - But physical access to registers is the system designer's choice.
  - Register functions are standardized, but layer to access the registers can be defined based on product requirements/convenience.
- Control: Select test or normal operation, select PRBS & starting seed, define debug pattern.
- Read: burst status, word or symbol error count, first error location.



Example, Test Configurations

Built-in Test

- Showing a variety of different methods to access the test registers.

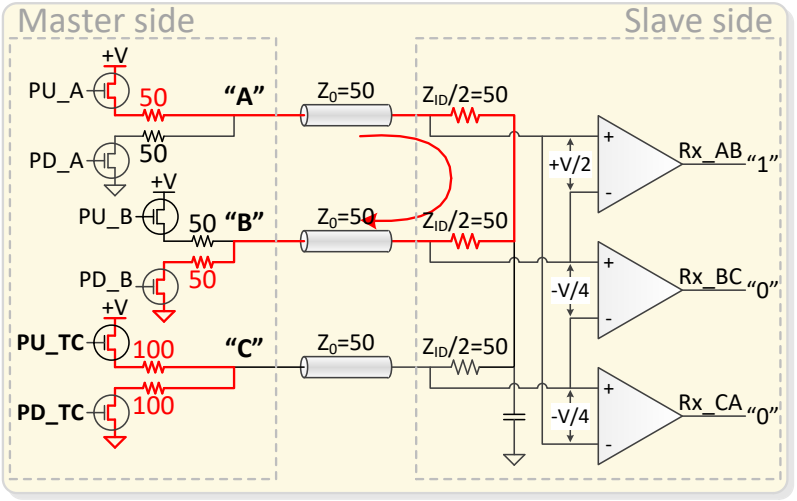


Differential or Single-Ended?

Single-Ended v Differential

- We've had many arguments about this. ☺
- The driver has the appearance of being single-ended
  - It's clearly different than a classic differential driver, however:
  - The average of the three outputs is the midpoint voltage: $\left(\frac{V_A+V_B+V_C}{3}\right) = V_{CPTX}$
- The sum of current through all three wires = zero.
- Differential Receivers are used to receive the signal at the Rx side.
- System has low emissions from any common-mode signal component.

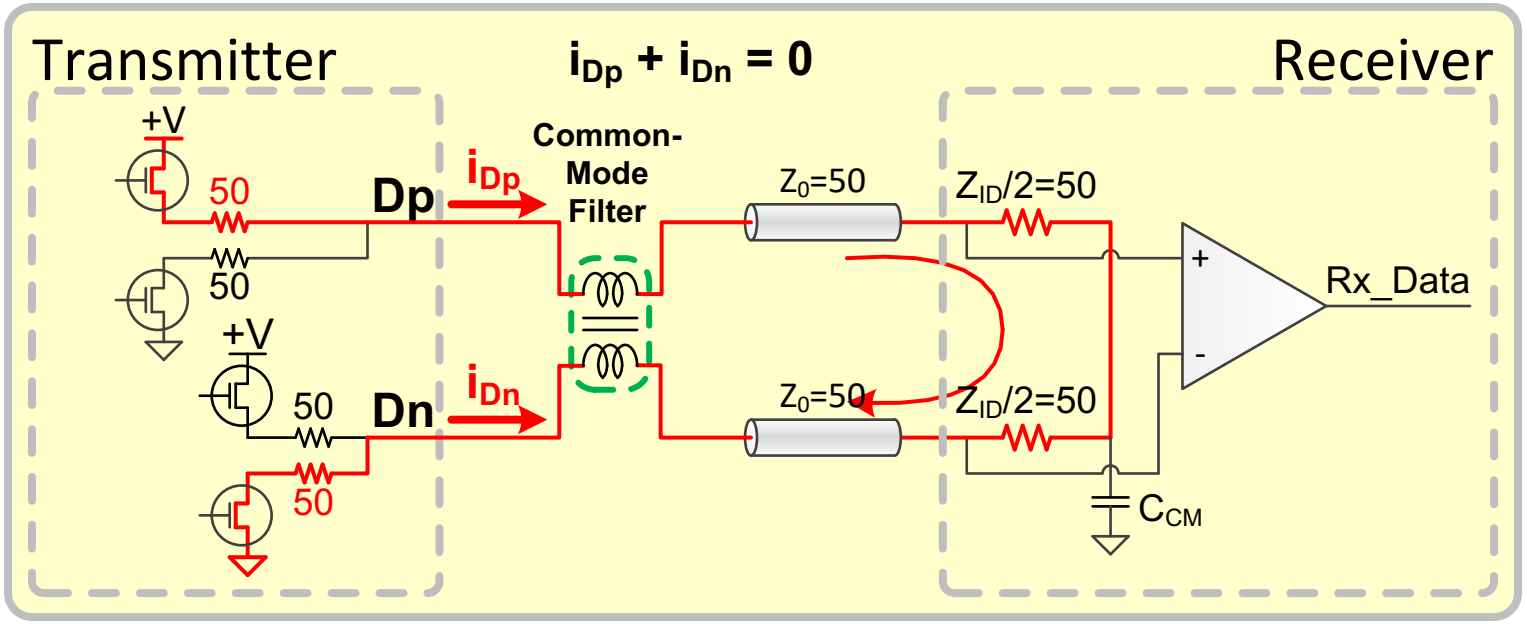
It's a wall, it's a rope,
it's a snake, it's a tree trunk...



D-PHY Common-Mode Filter

Common-Mode Filter

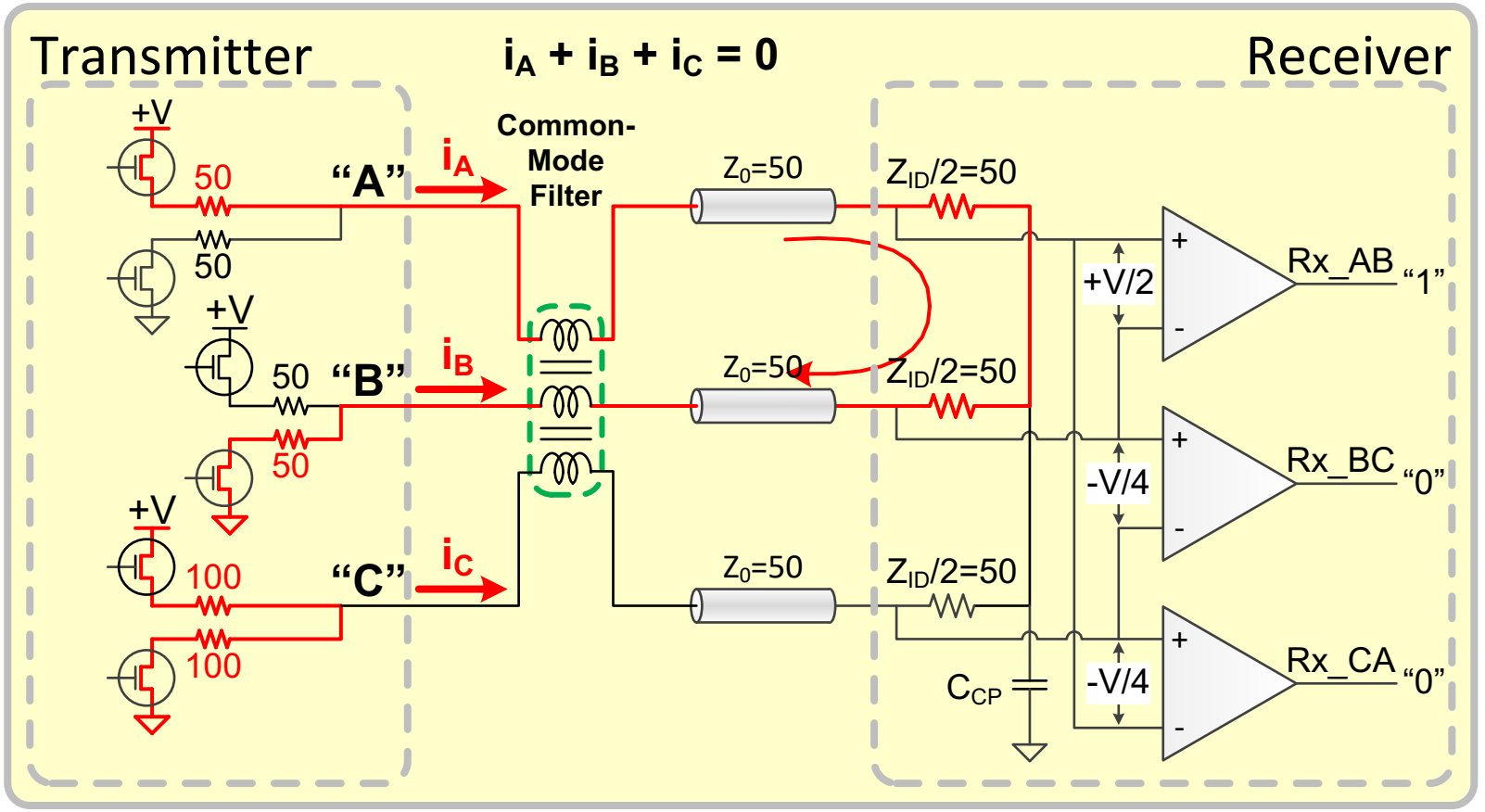
- Differential filter, shown for comparison purposes.
- Filter attenuates common-mode noise, but not the differential signal.



C-PHY Common-Mode Filter

Common-Mode Filter

- Similar general concept as the differential common-mode filter, but magnetics are different.

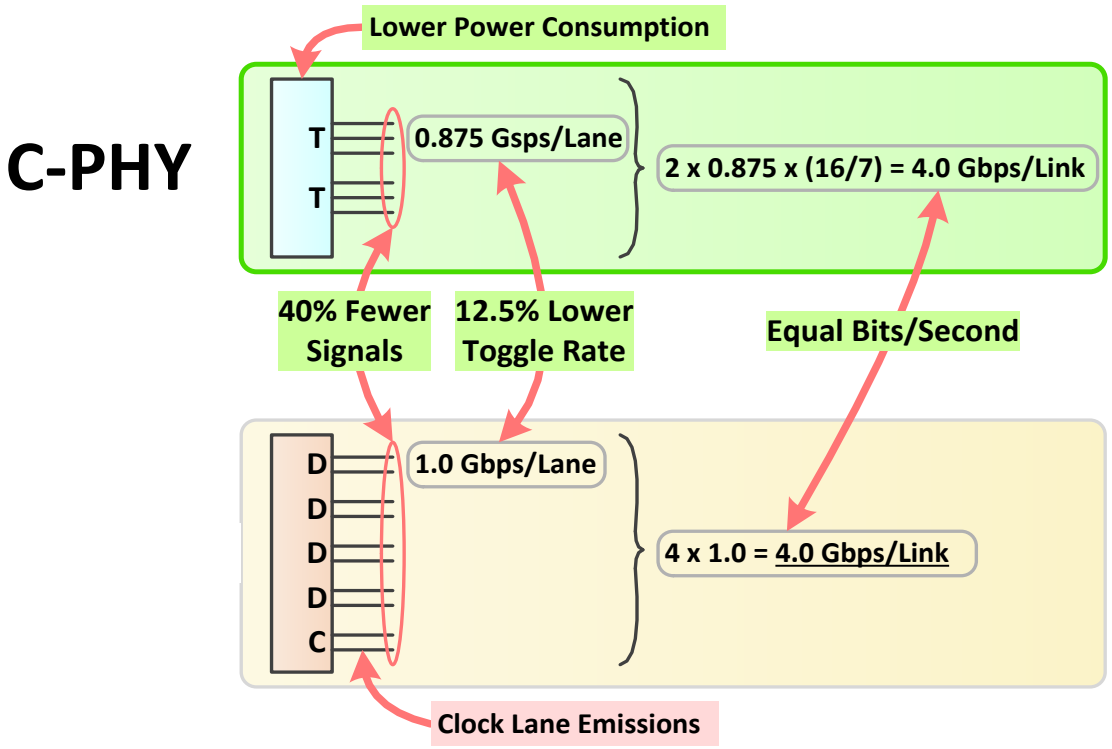


MIPI C-PHY Benefits & Value

MIPI C-PHY Benefits

- Performance (bit rate 2.28x the signaling rate, e.g. 1Gsym/s = 2.28Gbps)
- Pins
  - Enables fewer pins/balls on AP (due to higher performance and flexibility)
  - Coexists on same pins with existing D-PHY.
- Flexibility
  - Embedded clock enables assigning lanes to any port on the AP (flexible Lane (trio) to camera ISP mapping and display link mapping.
- Power
  - Qualcomm simulations/measurements show about a 20-50% power reduction for Tx+Rx, depending on configuration.
- Interference (Low Emissions)
  - Embedded clock eliminates clock spur emissions.
- Built-in Test
  - Extensive built-in test capability.

C-PHY System Benefits, Display Example

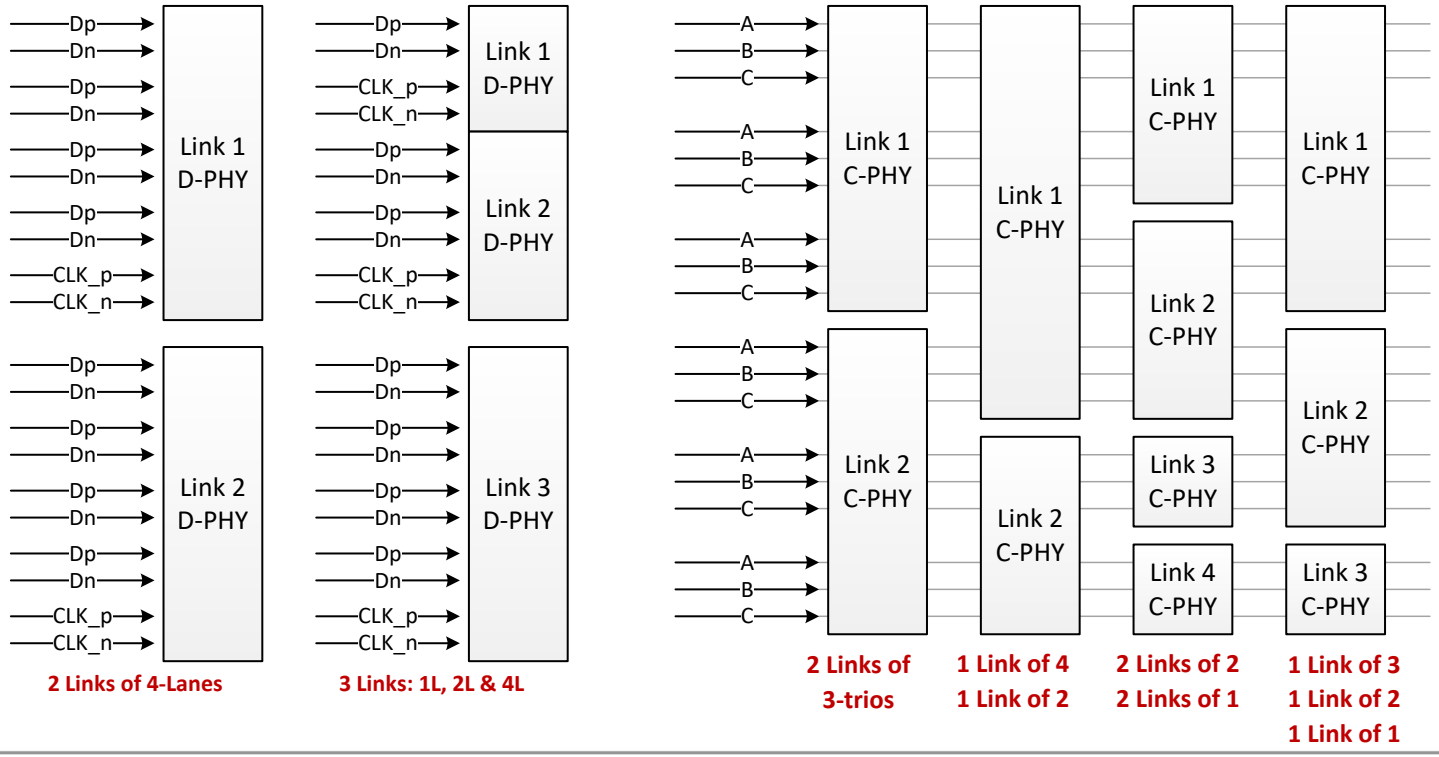


At the Same Link Rate, C-PHY has:

- 40% fewer connections
- 12.5% Lower Toggle Rate/Lane
- Lower Power Consumption
- No Emissions from a Clock Lane

Flexibility to Reassign Lanes

- C-PHY Lanes (Trios) easily reconfigured to different AP Links.
- Since C-PHY has embedded clock, there's no limitation to associate data lanes with a clock lane.
  - Easy to mux PHY Lanes (Trios) to Lane Merge/Distribution functions in Protocol Layer.
  - Can choose allocation of Lanes (Trios) to Links via register configuration.



Camera Example - Pins, Power & Speed

- C-PHY v1.0, D-PHY v1.2.
- Savings of pins, power, or link rate reduction.

Current savings is Tx & Rx combined.

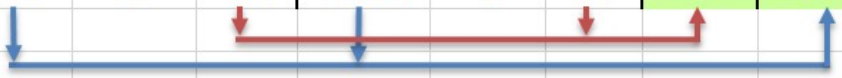
	Mpix	bpp	fps	OH	Sensor Gbps	D-PHY per lane Gbps	D-PHY Data Lanes	# of Pins /Link	C-PHY per lane Gsps	C-PHY Lanes	# of Pins /Link	C-PHY Pin Savings	C-PHY Speed Reduction	C-PHY Current Savings	C-PHY Savings T1 Driver
1	2	10	30	10%	0.66	0.66	1	4	0.29	1	3	1	56.3%	9%	36%
2	5	10	30	10%	1.65	1.65	1	4	0.72	1	3	1	56.3%	26%	46%
3	8	10	30	10%	2.64	1.32	2	6	1.16	1	3	3	12.5%	39%	n/a
4	13	10	30	10%	4.29	2.15	2	6	1.88	1	3	3	12.5%	43%	n/a
5	16	10	30	20%	5.76	1.92	3	8	1.26	2	6	2	34.4%	21%	n/a
6	21	10	30	20%	7.56	1.89	4	10	1.65	2	6	4	12.5%	30%	n/a
7	24	10	30	20%	8.64	2.16	4	10	1.89	2	6	4	12.5%	32%	n/a
8	32	10	30	20%	11.52	2.30	5	12	1.68	3	9	3	27.1%	21%	n/a
9	40	10	30	20%	14.40	2.40	6	14	2.10	3	9	5	12.5%	28%	n/a

Camera Example - Pins, Power & Speed

- C-PHY v1.1, D-PHY v2.0.
- Savings of pins, power, or link rate reduction.

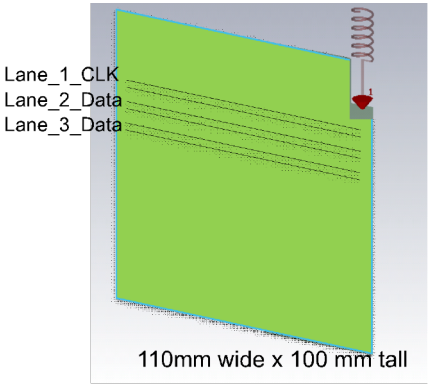
Current savings is Tx & Rx combined.

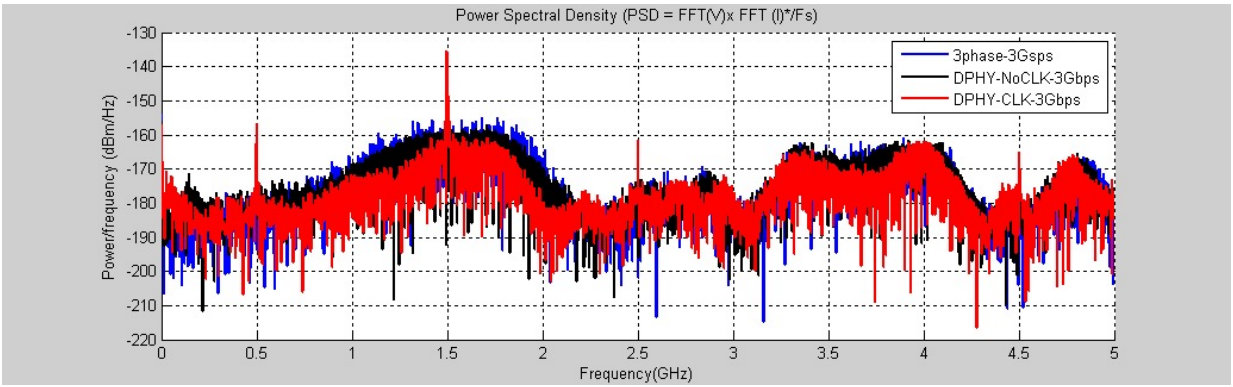
	Mpix	bpp	fps	OH	Sensor Gbps	D-PHY per lane Gbps	D-PHY Data Lanes	# of Pins /Link	C-PHY per lane Gsps	C-PHY Lanes	# of Pins /Link	C-PHY Pin Savings	C-PHY Speed Reduction	C-PHY Current Savings	C-PHY Savings T1 Driver
1	2	10	30	10%	0.66	0.66	1	4	0.29	1	3	1	56.3%	9%	36%
2	5	10	30	10%	1.65	1.65	1	4	0.72	1	3	1	56.3%	26%	46%
3	8	10	30	10%	2.64	2.64	1	4	1.16	1	3	1	56.3%	36%	n/a
4	13	10	30	10%	4.29	4.29	1	4	1.88	1	3	1	56.3%	45%	n/a
5	16	10	30	20%	5.76	2.88	2	6	2.52	1	3	3	12.5%	45%	n/a
6	21	10	30	20%	7.56	3.78	2	6	1.65	2	6	0	56.3%	23%	n/a
7	24	10	30	20%	8.64	4.32	2	6	1.89	2	6	0	56.3%	27%	n/a
8	32	10	30	20%	11.52	3.84	3	8	2.52	2	6	2	34.4%	32%	n/a
9	40	10	30	20%	14.40	3.60	4	10	2.10	3	9	1	41.7%	22%	n/a



C-PHY Low Emissions

- No clock interference due to embedded clock
- No observable emissions/EMI due to non-differential signaling
- A few simple configurations of D-PHY and C-PHY were evaluated for emissions
  - Lanes routed on a board, in close proximity to WWAN Antenna
  - For comparison purposes only, as Absolute levels depend on many complex conditions in a real device
  - Higher emissions from the D-PHY clock lane correlates with real-world designs

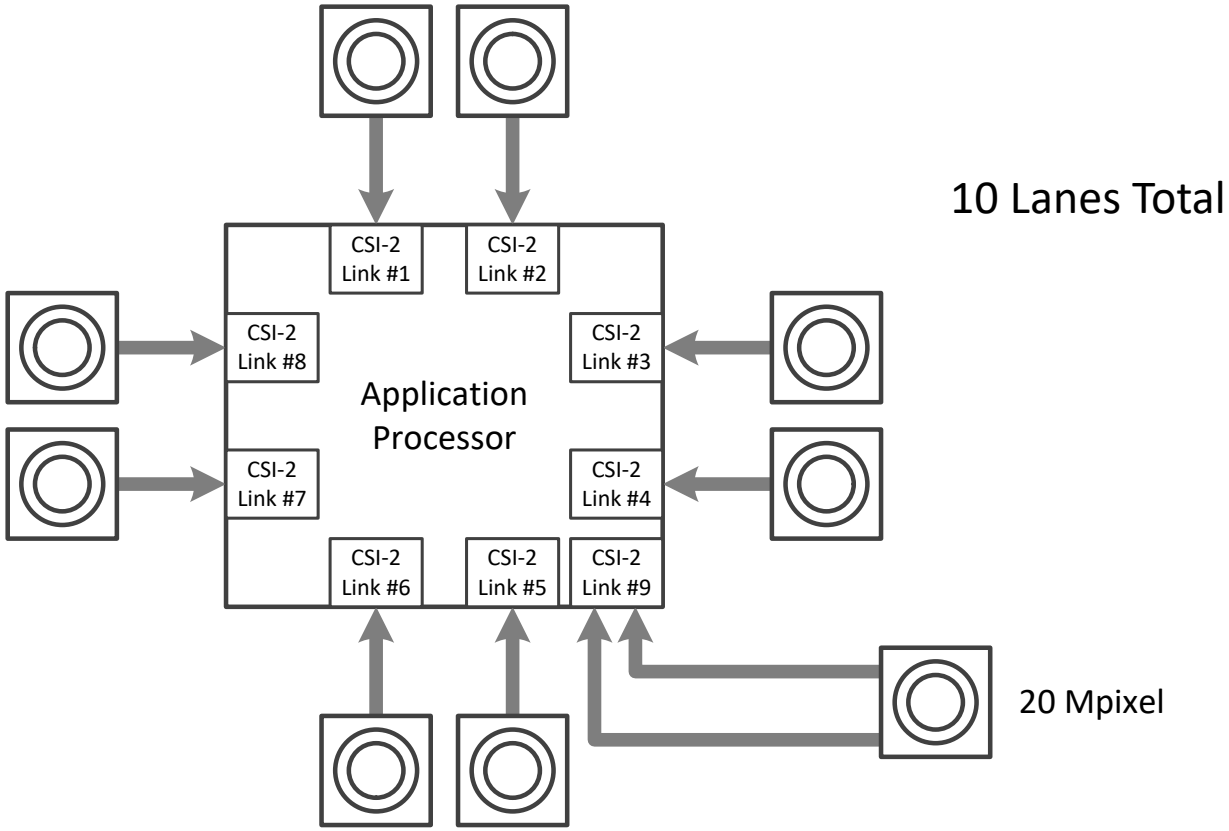




MIPI C-PHY Applications

Drone Camera Connection Example

- One 20 Mpixel main camera (2 Lanes, 6 wires).
- 8 navigation cameras (1 Lane each, 3 wires each).



The Trend to Fewer Pins

- The conventional MIPI D-PHY Link configuration has been 4 Data + 1 Clock.
  - 10 pins total.
- Reduction to 6 pins
  - A majority of 10 to 20 Mpixel image sensors can be supported using 1 or 2 C-PHY Lanes.
  - Low-res image sensors that have sensitivity to high channel rates can be supported using 2 Lanes.

MIPI C-PHY Roadmap

C-PHY Feature Roadmap

Category	Feature	v1.0	v1.1	v1.2	next
	Board Adoption	4Q14	1Q16	**~4Q16 Target**	
Speed	Symbol Rate (Gsps/Lane) *	2.5	2.8	**~3.5**	
Symbol Rate	C-PHY/D-PHY Unified Channel Models		✓	✓	✓
	Tx Timing by Tx Eye Diagram		✓	✓	✓
	Basic Pre-emphasis		✓	✓	✓
	PVT Calibration for Rx			✓	✓
	Additional UI Jitter (RCLK jitter) specs			✓	✓
	Pre-emphasis/De-emphasis, Gen 2			✓	✓
	Technology Enhancements to Increase the Symbol Rate				✓
Power Reduction	Unterminated Mode		✓	✓	✓
	Reduced Amplitude HS Mode option (same V_{OD} as D-PHY)			✓	✓
LP Mode	**Alternate Low-Power Mode**			✓	✓
Enhanced Function	Co-exists with D-PHY on same device pins	✓	✓	✓	✓
	Track D-PHY SG Activity to Keep C/D-PHY Specs In-Sync	✓	✓	✓	✓
	16-bit/32-bit PPI		✓	✓	✓
	Optical Interconnect		✓	✓	✓
	HS Reverse Mode			✓	✓
	Low Latency Delimiter (LLPD), for Camera			✓	✓
	Various Functional Enhancements Planned				✓

* The stated Symbol Rate is with the Standard Channel except v1.0 which is the rate with the Legacy Channel

Summary

C-PHY Ecosystem

- Application Processor companies
  - Qualcomm, others in development
- Image Sensors
  - OmniVision, Sony, others in development
- Display Driver ICs
  - In development
- Test equipment companies
  - Introspect, Keysight, Tektronix, The Moving Pixel Company, others in development
- Silicon IP
  - In development
- System components
  - Common-mode filters: Murata, Panasonic, TDK
  - C-PHY switches

Summary

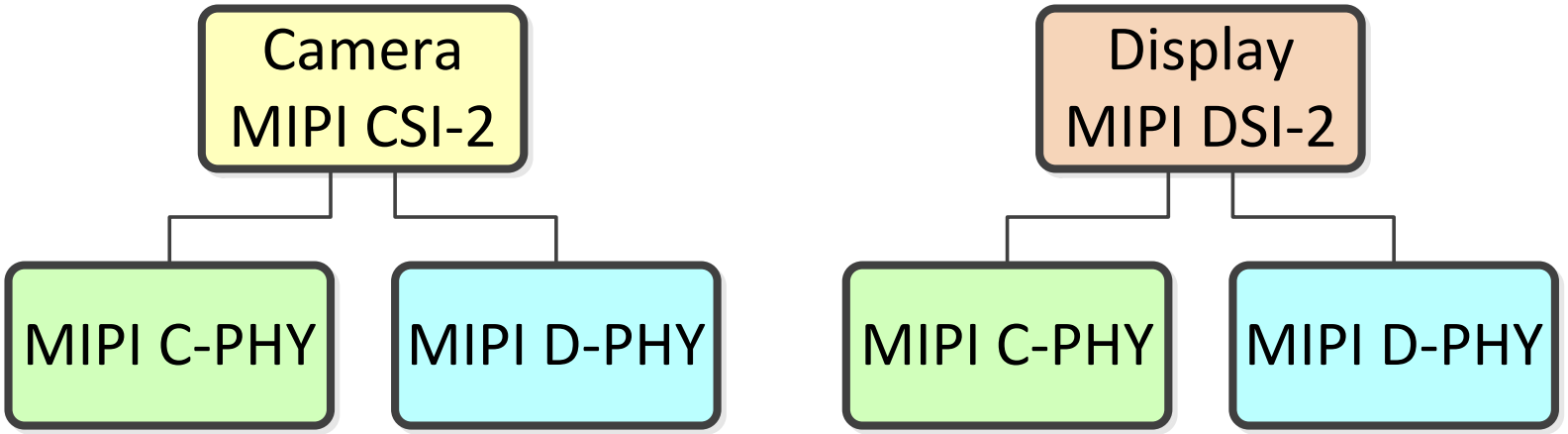
- Satisfies all KPI's…
  - Pins (Cost), Architectural Flexibility, Performance, Power, Low Emissions
- Suitable for all product tiers
  - C/D-PHY combo into high tier products first, now migrating to mid and low-tiers.

Thank You

Backup Material

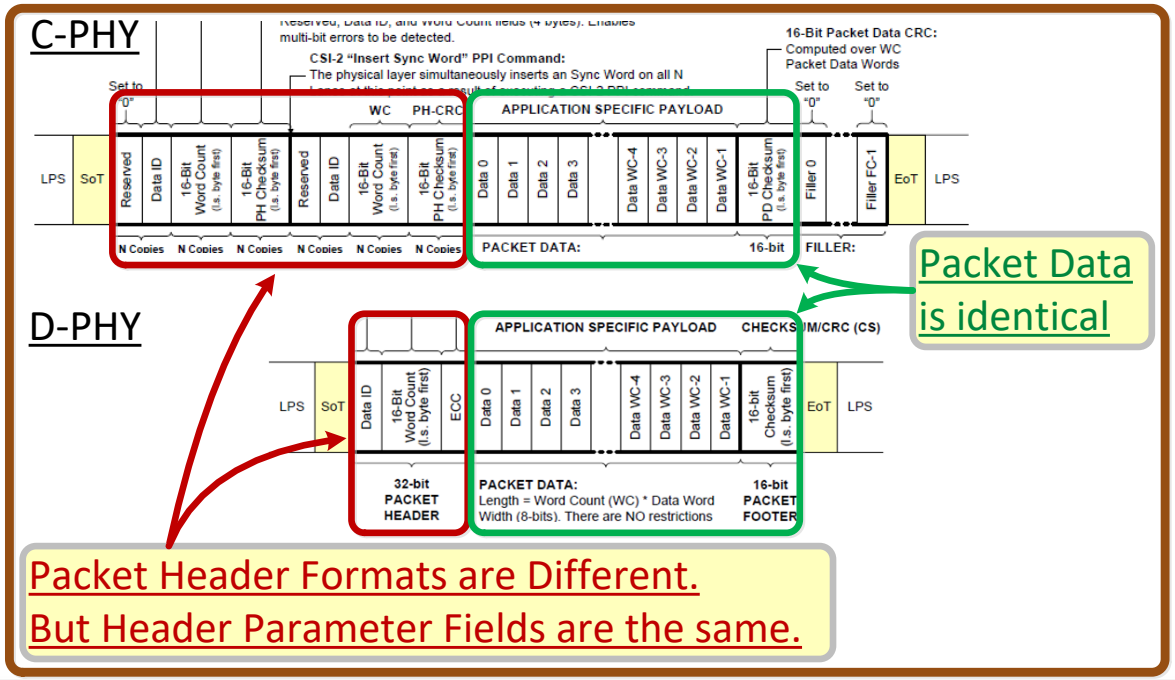
CSI-2 and DSI/DSI-2 Ecosystems

- Protocol specs, CSI-2 and DSI (now DSI-2) reference C-PHY & D-PHY.
  - Huge existing ecosystems for Camera and Display are preserved.
- Camera & Display protocol specs have been updated to include C-PHY.



CSI-2 and DSI-2 Details

- How Camera & Display protocol specs reference both PHY's.
  - Low-Level packet header formats are a little different for C-PHY vs. D-PHY.
  - Application-Specific Payloads of the Packets are identical.

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