



TECHNOLOGY BRIEF

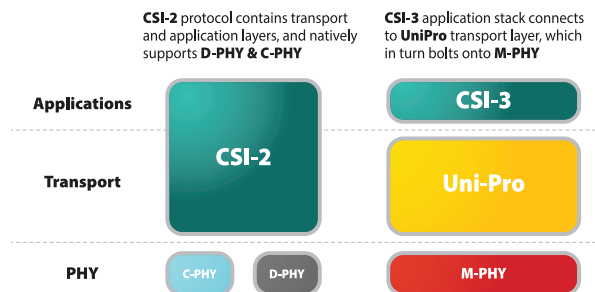
Evolving CSI-2 Specification

The bandwidths of today's host processor-to-camera sensor interfaces are being pushed to their limits by the demand for higher image resolution, greater color depth and faster frame rates. But more bandwidth is simply not enough for designers with performance targets that span multiple product generations.

The mobile industry needs a standard, robust, scalable, low-power, high-speed, cost effective camera interface that supports a wide range of imaging solutions for mobile devices.

The MIPI® Alliance Camera Working Group has created a clear design path that is sufficiently flexible to resolve not just today's bandwidth challenge but "features and functionality" challenges of an industry that manufactures more than a billion handsets each year for a wide spectrum of users, applications and cost points.

MIPI CSI-2 and MIPI CSI-3 are the successors of the original MIPI camera interface standard, and both standards continue to evolve. Both are highly capable architectures that give designers, manufacturers – and ultimately consumers – more options and greater value while maintaining the advantages of standard interfaces.



Technical Summary

The latest Camera Serial Interface 2 Specification (CSI-2 v1.3) offers higher interface bandwidth and greater channel layout flexibility than its predecessor. It introduces C-PHYSM 1.0, a new PHY that MIPI Alliance released in September 2014, as well as support for the previous version's D-PHYSM 1.2 interface.

Both PHY options improve skew tolerance and provide higher data rates. Both are serial interfaces that address many of the problems of parallel interfaces, which consume relatively large amounts of power, are difficult to expand and can be proprietary.

Sensor fusion and shutter lag

- Compatible with I2C interface widely used in camera subsystems.
- Sensor flexibility: Design into systems with ALS, IR, Gyro, Presence, Accelerometer and MEMS sensors.
- Real-time sensor configuration and adjustment.
- Fast AF: Real-time feedback allows quick lens configuration. Never miss a shot.

Richer and subtler colors

- Improved data transfer rate (up to 4X) enables increased color depth (up to 1.6 factor) and higher resolutions for crisper images.

Longer battery life

- Lowest energy per bit allows most efficient operation in the industry.
- Robust operation minimizes processor overhead.

Higher video resolution

- Higher bandwidth enables frame resolutions of 1080p, 4k, 8k and beyond and more stable images including 240 FPS and higher.

Lower system cost

- Lower pin count.
- Longer wires allow more flexible system integration.
- Low EMI facilitates routing across the screen.
- C-PHY solution provides embedded clock and data enabling about 2.3X effective bandwidth increase over channel toggle rate that reduces the number of PHY pins.



TECHNOLOGY BRIEF

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Using D-PHY maintains compatibility with earlier versions of the specification and lets vendors leverage their existing product development infrastructure. C-PHY requires a minimum of three pins instead of four and provides pin-wise backwards compatibility with D-PHY. Designers can implement standalone C-PHY, D-PHY or combo C/D-PHY options to ensure longer-term design viability.

The CSI-2 protocol contains transport and application layers and natively supports C-PHY, D-PHY, or combo C/D-PHY. The camera control interface for both physical layer options is bi-directional and compatible with the I2C standard. The CSI-2 Specification defines standard data transmission and control interfaces between the camera as a peripheral device and a host processor, which is typically a baseband, application engine. The table below illustrates optimal MIPI CSI and PHY configurations for popular 4K imaging format:

4K @ 30 FPS AND 12 BPP

REQUIRED MIPI SPECS (IPs)	PHY PINS	CHANNEL RATE	REQUIRED BW	VARIABLE LINK RATE	CONTROL INTERFACE
[CSI-2] [D-PHY]	6	1.78 Gbps	3.56 Gbps	Yes	I2C
[CSI-2] [C-PHY]	3	1.55 Gbps	3.56 Gbps	Yes	I2C

Gbps = Giga bits per second | Gsps = Giga symbols per second

CSI-2 over D-PHY and C-PHY

D-PHY as used in CSI-2 is a unidirectional differential interface with one 2-wire forwarded clock lane and one or more 2-wire data lanes. The updated D-PHY specification, v1.2, introduces lane-based data skew control in the receiver to achieve a peak transmission rate of 2.5 Gbps/lane or 10 Gbps over 4 lanes, compared to the v1.1 peak transmission rate of 1.5 Gbps/lane or 6 Gbps over 4 lanes.

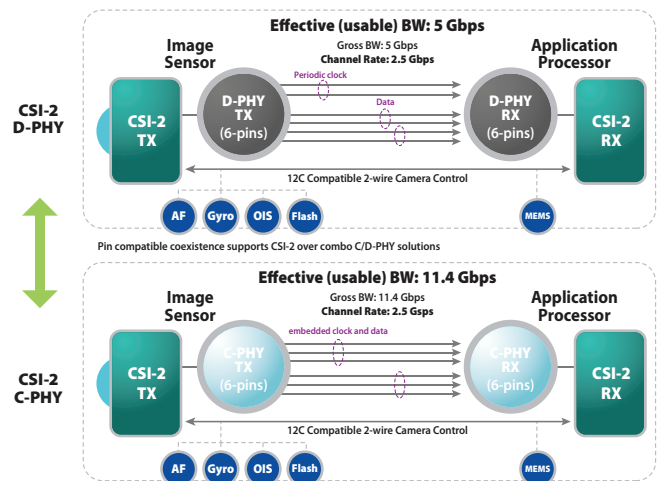
C-PHY consists of one or more unidirectional 3-wire serial data lanes or "trios", each with its own embedded clock. The physical layer of C-PHY interface is defined by the MIPI Alliance Specification for C-PHY. MIPI C-PHY uses 3-phase symbol encoding of about 2.28 bits per symbol on a trio where each trio operating at 2.5 Gsps provides an equivalent of 5.7 Gbps per lane. Three trios operating at the C-PHY v1.0 rate of 2.5 Gsps provides 17.1 Gbps over a 9-wire interface that can be shared, if desired, with the MIPI D-PHY interface.

CSI-2 over C/D-PHY imaging interface does not limit the number of lanes per link. Transmission rate linearly scales with the number of lanes for both C-PHY and D-PHY. The Figure below illustrates the connections between a CSI-2 Image Sensor transmitter and an Application Processor receiver using 6-pin C/D-PHYs, which are typically used on Mobile Platforms.

MIPI's CSI-2 is currently the most widely adopted camera interface in mobile devices.

CSI-2 v1.3 At-a-Glance

- C-PHY 1.0, D-PHY v1.2 or "combo C/D-PHY" possible
- 4 Virtual Channels, 64 Data Types
- RGB, YUV, RAW, JPEG Formats
- Embedded Data
- Line based transmission
 - Easy implementation
 - Low gate count
 - Matched data rates for sensor and link
- CRC/ECC for payload and header protection

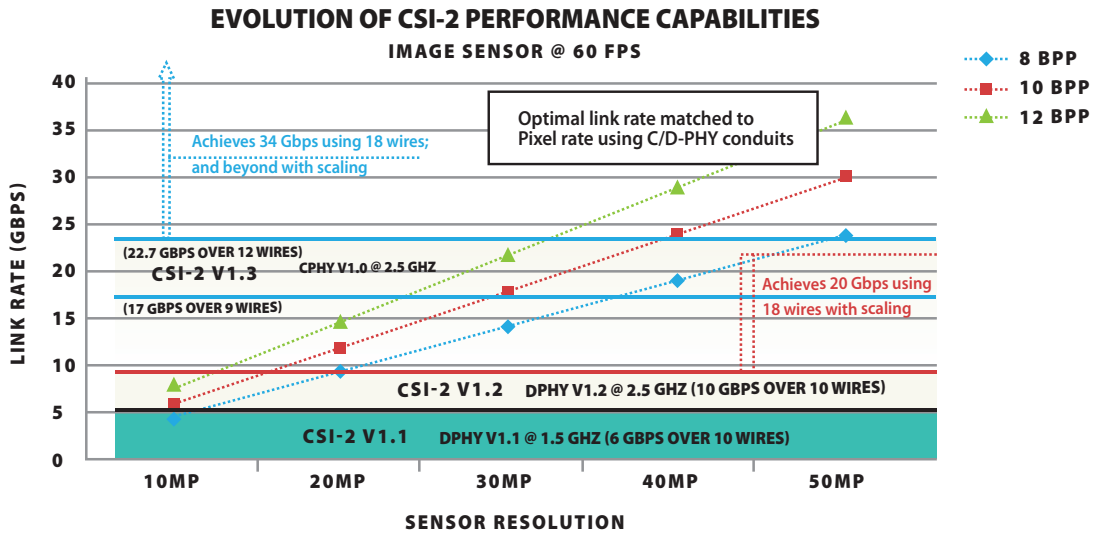




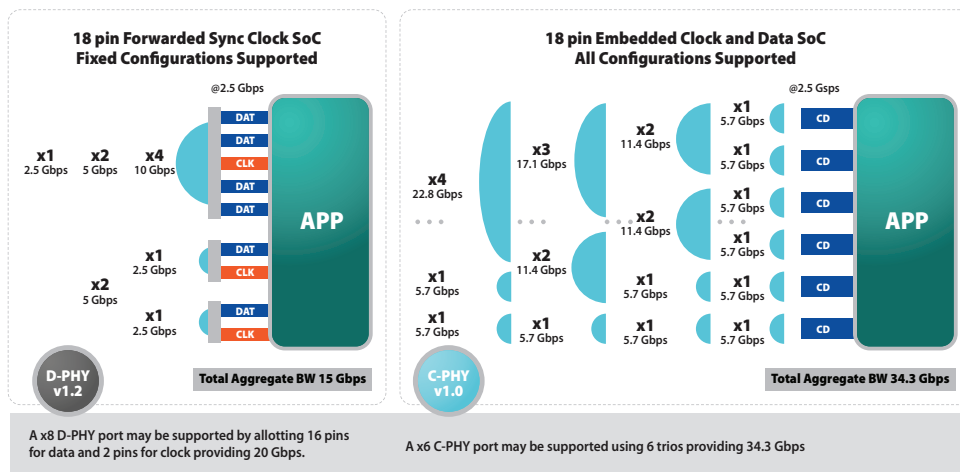
TECHNOLOGY BRIEF

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The following graph illustrates the evolution of CSI-2 over C/D-PHY interface performance for broad range of mobile and beyond imaging applications.



The following figure illustrates the benefits of CSI-2 logical port configurations with embedded clock and data. A myriad of imaging use cases can be mapped on multiple port configurations. Embedded clock and data (CD) lanes provide configurable logical port realizations on CSI-2 platforms.



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