Leveraging Video Compression within MIPI DSI-2^{SM} for High-Performance Displays

IF IT'S NOT MIPI, IT'S NOT MOBILE

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26 May 2021

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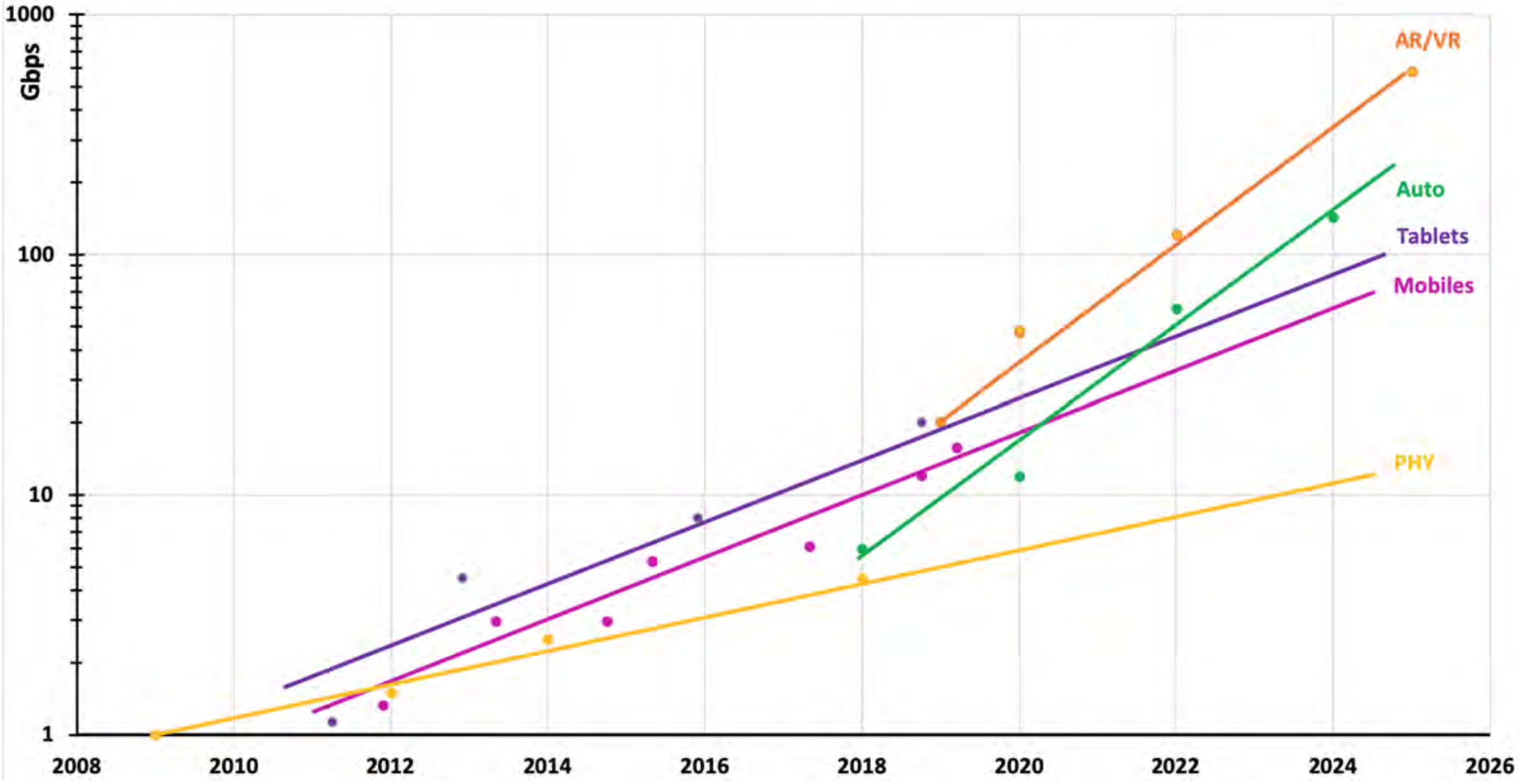
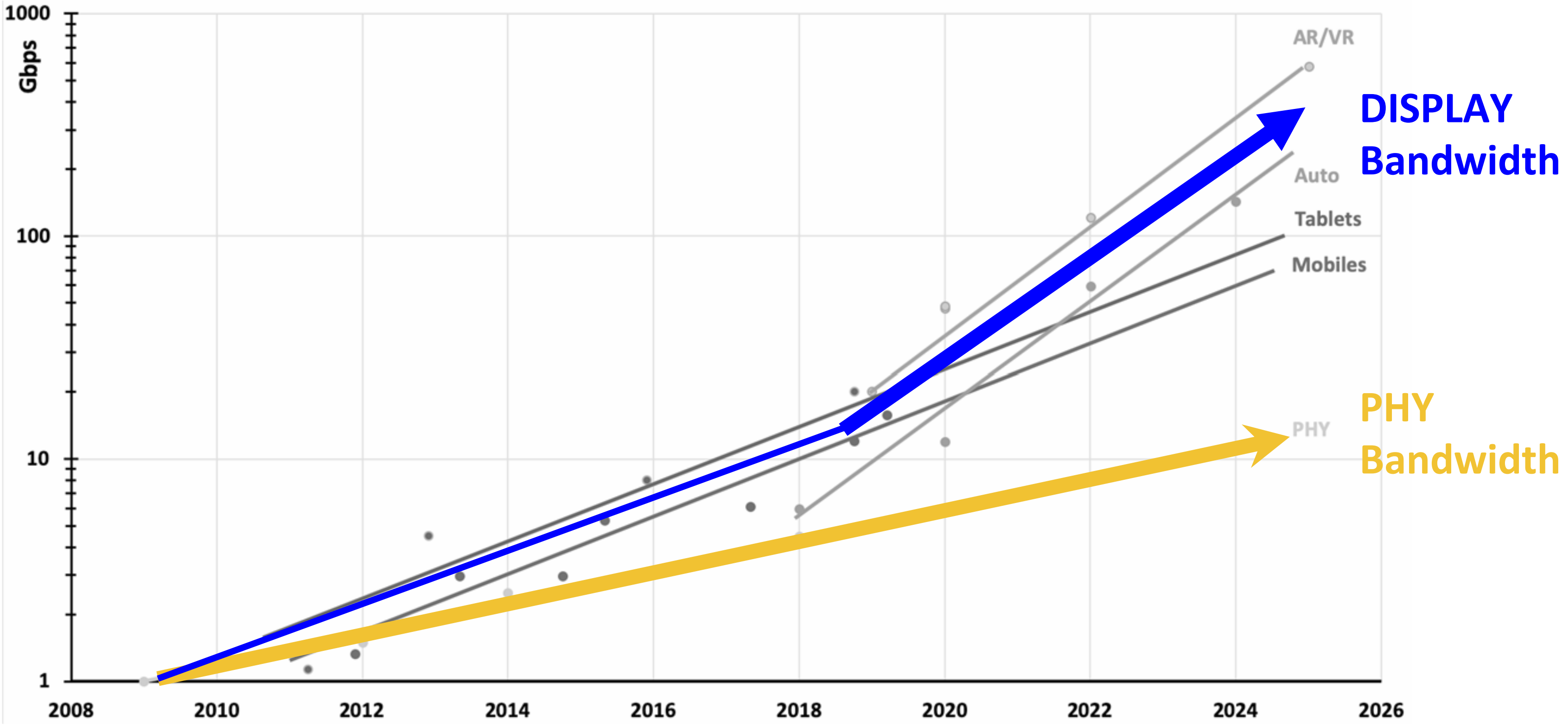
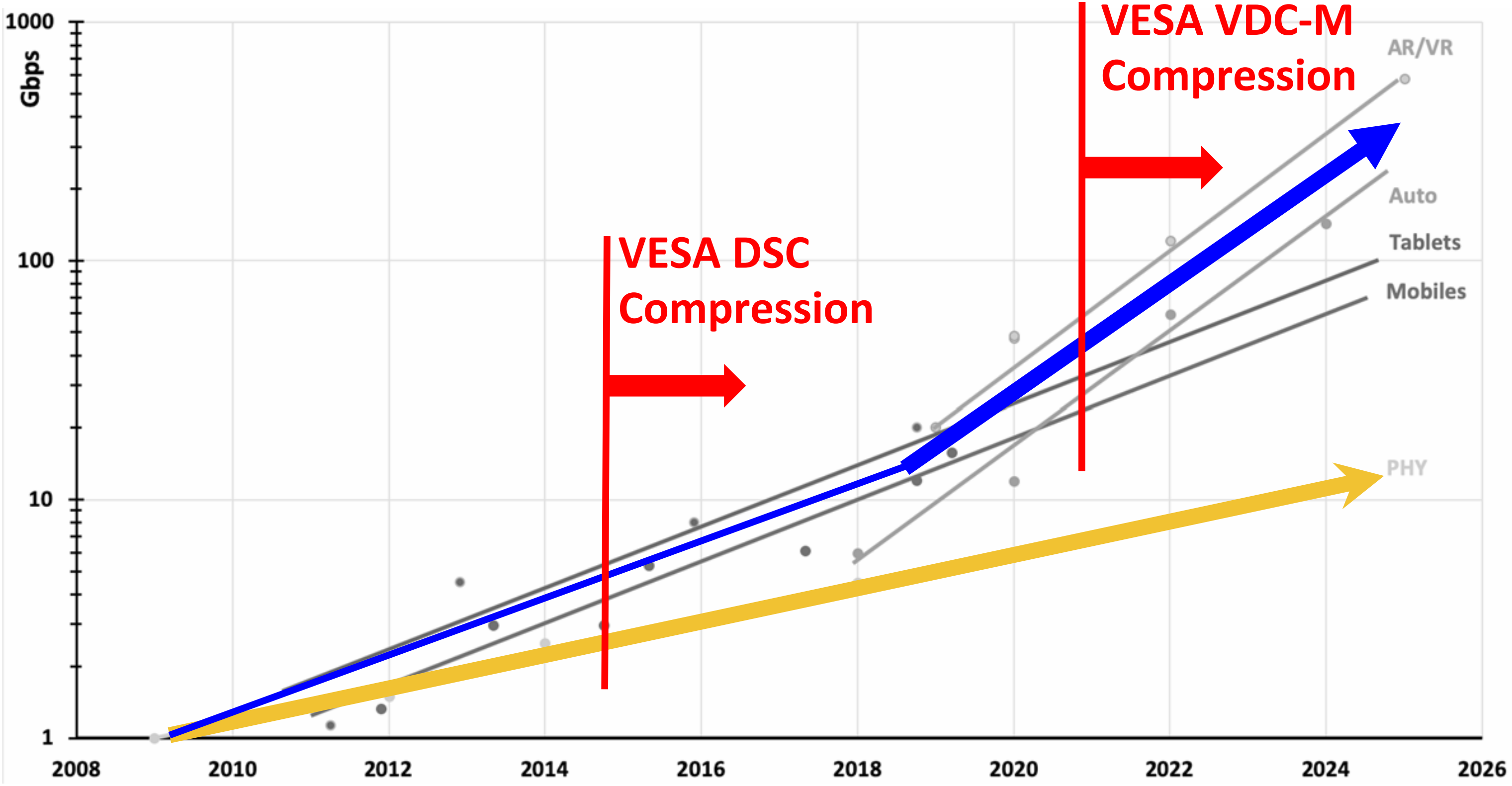
Product Display Bandwidth Trends



Product Display Bandwidth Trends



Product Display Bandwidth Trends



VESA Video Compression Codecs

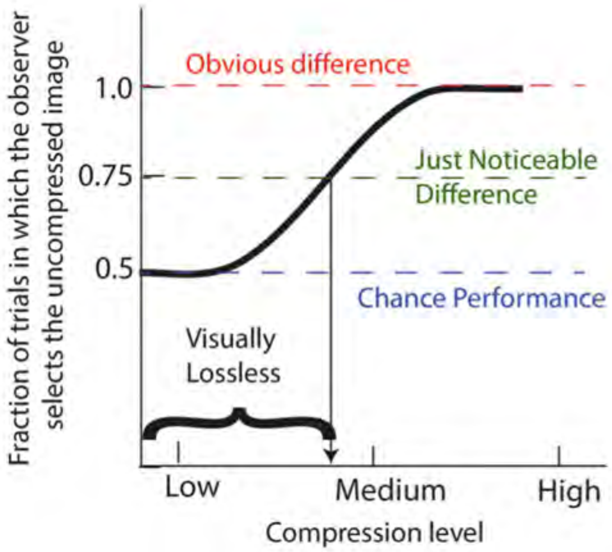
- Incorporated in the MIPI Display Serial Interface (MIPI DSI-2^{SM})
- Guaranteed low-latency performance
- Visually lossless quality for all images and video

Which specification should you use?

It depends on your target application & desired display features!

Image Quality Testing

- **Visually lossless subjective testing method:**
  - Expert analysis with image interleaving on high quality monitors
  - Non-expert random evaluation using the ISO/IEC CD 29170-2 procedure
    - Based on a "flicker test" and forced paradigm
  - All types of images tested
- **Test results:**
  - DSC at 8bpp vs. VDC-M at 6bpp: both are visually lossless
  - The two codecs have been tested with HDR content
  - Stereoscopic testing is also being done



Source: Hoffman & Stolitzka, 2015

Resources

Find out more about VESA's image quality testing:

- VESA Display Stream Compression Whitepaper, 2014
- *A new standard method of subjective assessment of barely visible image artifacts and a new public database: Subjective analysis of image quality* by David M Hoffman and Dale Stolitzka, 2015
- VESA DSC test results available for download: vesa.org/displayport-developer/presentations/

DSC & VDC-M: Comparison of Key Features

	DSC	VDC-M
Encoding Block Structure	**3x1 pixels**	**8x2 pixels**
Encoding Tools	• Mid Point (MPP) • Block Predictor (BP) • Modified Median Adaptive Predictor (MMAP) • Indexed Color History (ICH)	• Mid Point (MPP) • **Enhanced Block Predictor (BP)** • **Transform (DCT & Hadamard)** • Enhanced Quantization
IC Complexity	**Low**	**Medium**
Visually Lossless Performance	**8 bpp (bits per pixel)**	**5-6 bpp (bits per pixel)**
RAM Usage	Single line	2.5 lines
Latency (end-to-end) **Example: UHD 3840 x 2160**	**<0.5us** <2H line	**<1.2us** <5H line
Pixels/Clock Architecture		
Encoder	1	2
Decoder	3	4

Source: VESA Website

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Applications Using VESA Compression Codecs

- Mobiles
- Tablets
- Test equipment
- GPUs
- AR/VR devices
- Automotive video systems
- Video transport
- 8K TVs
- DTV set top boxes
- High-resolution monitors

Video Compression: Application-Specific Benefits

Market Trends	Compression Benefits
• Multiple or foldable displays • Ultra-high display resolutions • Ultra-high pixel density • High dynamic range (HDR) content • Higher frame rates	• Lower power consumption • Smaller footprint • Lower cost • Less pins • Lower switching frequencies
• Increased number of displays • Higher display resolutions • Multiple video sources in parallel	• Reduced number of cables • Lower weight & labor costs • Lower EMI • Lower power consumption • More reliable

Market Focus

Mobile

Mobile Market Trends

- Mobile devices need to be XR-ready
- Movement from LCD to OLED displays with sub-pixel rendering
  - Ultra-high resolutions and pixel density (up to 1500 ppi)
  - High dynamic range (HDR)
  - Higher frame rate
  - Optical compensation
  - Foldable, rollable displays
  - Lower power consumption
  - Non-uniformity compensation
- DDIC frame buffer going from 10 to 100 Mbits
- 5G increases EMI challenges

	2010	2020
Display Resolution	1280 x 720 HD	3840 x 2160 4K
Frame Rate	60 fps	120 fps
Pixel Depth	24 bits	30 bits
Interface	0.5 Gbps / lane	2.0 Gbps / lane With DSC
Display Bandwidth	1.3 Gbps	29.9 Gbps

23x

VDC-M Allows Higher Resolutions

Standard Resolution Bpp/Rate	FHD 1080x1920 24bpp/60fps	WQXGA 1600x2560 24bpp/60fps	UHD 2160x3840 24bpp/60fps	WQUXGA 2400x3840 24bpp/60fps	5K 2880x5120 24bpp/60fps	UHD 2160x3840 30bpp/120fps	5K 2880x5120 30bpp/120fps	VR 4kx4K 4096x4096 30bpp/120fps	8K 4320x8192 30bpp/120fps
Bandwidth	3.58Gbps	7.08Gbps	14.33Gbps	15.93Gbps	25.48Gbps	35.83Gbps	63.7Gbps	72.48Gbps	152.88Gbps
D-PHY v1.1 1.5Gbps / lane									
3x compression	1	2	4	4	6	8	N/A	N/A	N/A
4x compression	1	2	3	3	5	6	N/A	N/A	N/A
5x compression	N/A	N/A	N/A	N/A	N/A	5	N/A	N/A	N/A
D-PHY v1.2 2.5Gbps / lane									
3x compression	1	1	2	3	4	5	N/A	N/A	N/A
4x compression	1	1	2	2	3	4	7	8	N/A
5x compression	N/A	N/A	N/A	N/A	N/A	3	6	6	N/A
D-PHY v2.0 4.5Gbps / lane									
3x compression	1	1	2	2	2	3	5	6	N/A
4x compression	1	1	1	1	2	2	4	5	N/A
5x compression	N/A	N/A	N/A	N/A	N/A	2	3	4	7
D-PHY v2.1 6.5Gbps / lane short channel									
3x compression	1	1	1	1	2	2	4	4	8
4x compression	1	1	1	1	1	2	3	3	6
5x compression	N/A	N/A	N/A	N/A	N/A	2	2	3	5

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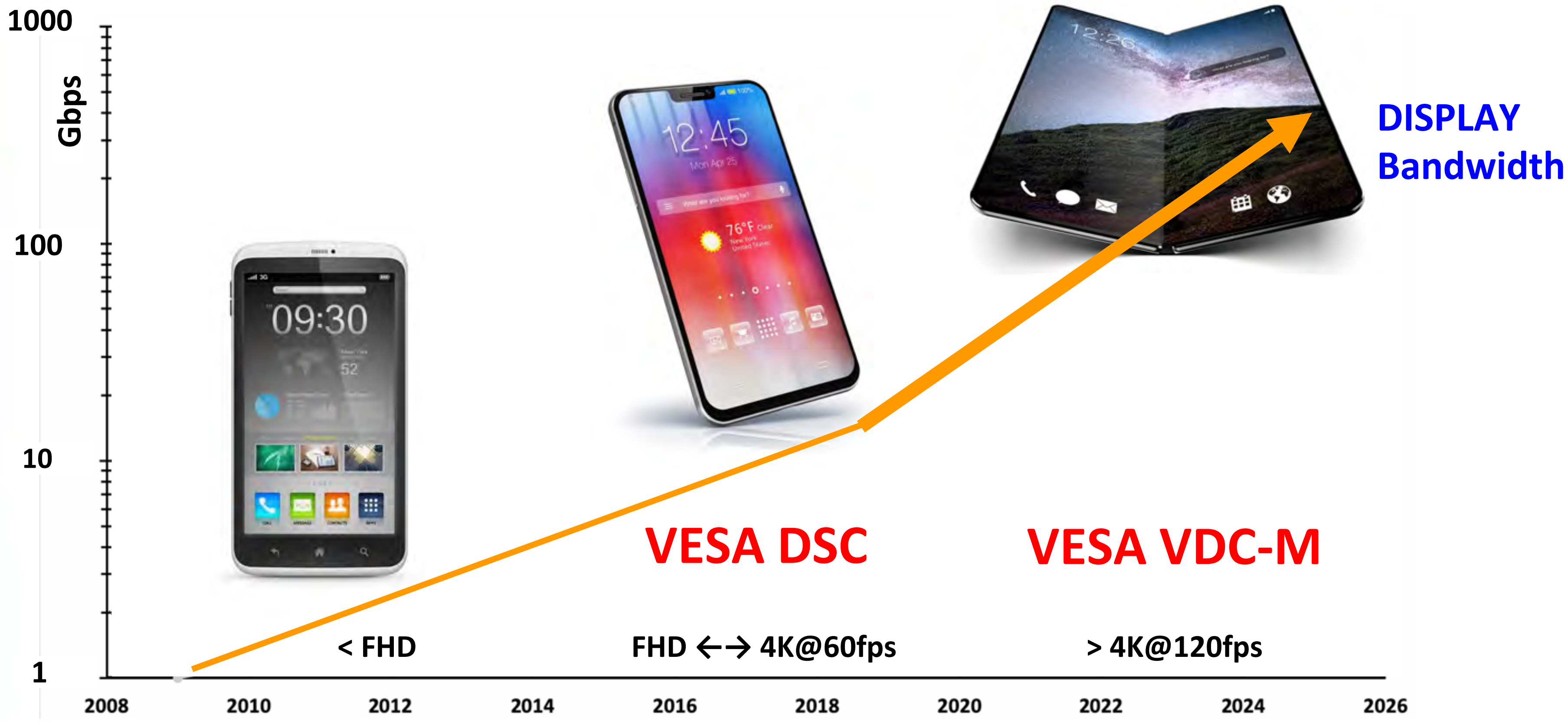
Display Resolution vs. Compression Technology



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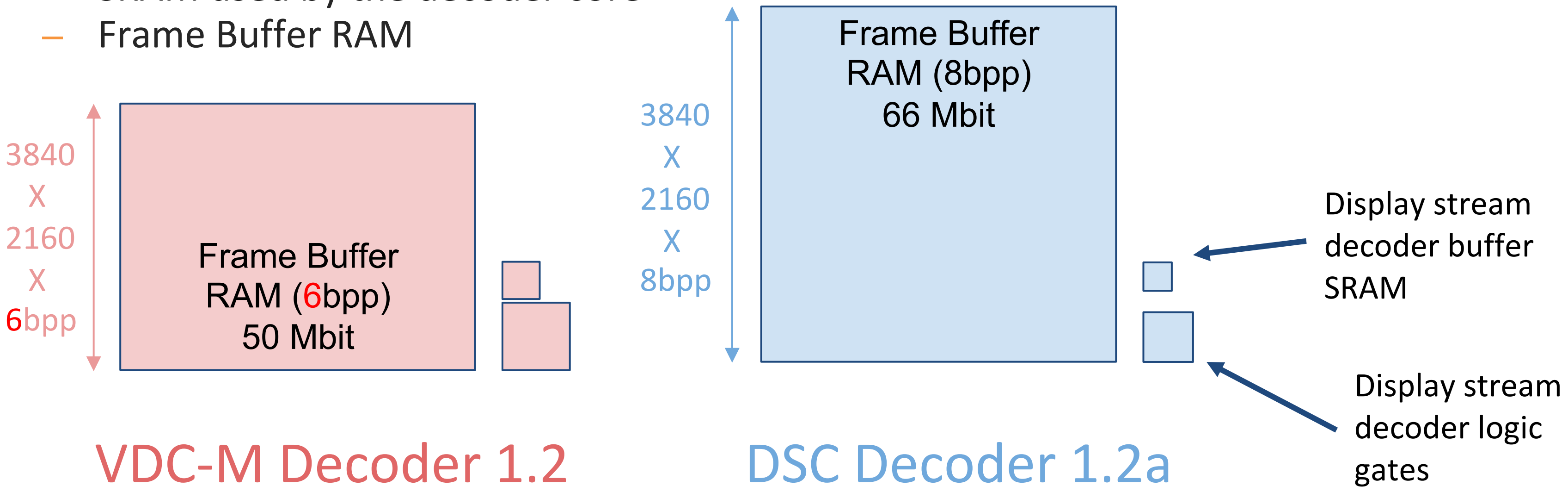
DDIC Frame Buffer Subsystem: UHD/4K Resolution 10bpc Use Case

- **DDIC frame buffer subsystem includes the following three main components:**
  - Display stream decoder core
  - SRAM used by the decoder core
  - Frame Buffer RAM



Drawn to scale

VDC-M vs. DSC for DDIC

- **VDC-M offers attractive PPA (Power, Performance, Area) when compared to DSC:**
  - Larger core gate count and internal SRAM is offset by a significant reduction in Frame Buffer RAM
  - Higher clock gating efficiency yields lower power
  - 4 pixels/clock decoder architecture allows for lower clock rates for the same throughput (Results in lower LVT usage)
- **Overall VDC-M-based DDIC design will be:**
  - 77% the area
  - 75-80% the power
  - Same throughput
- **Additional savings will be obtained by the reduction in number or speed of MIPI PHY lanes**

Market Focus

AR & VR

AR/VR Market

- **Challenges**
  - Requires two displays at higher resolution, higher ppi, higher refresh rates
  - Tethered Head-Mounted Display:
    - Cables are running out of bandwidth
  - Wireless Head-Mounted Display:
    - Bandwidth, power management, and miniaturization are huge obstacles

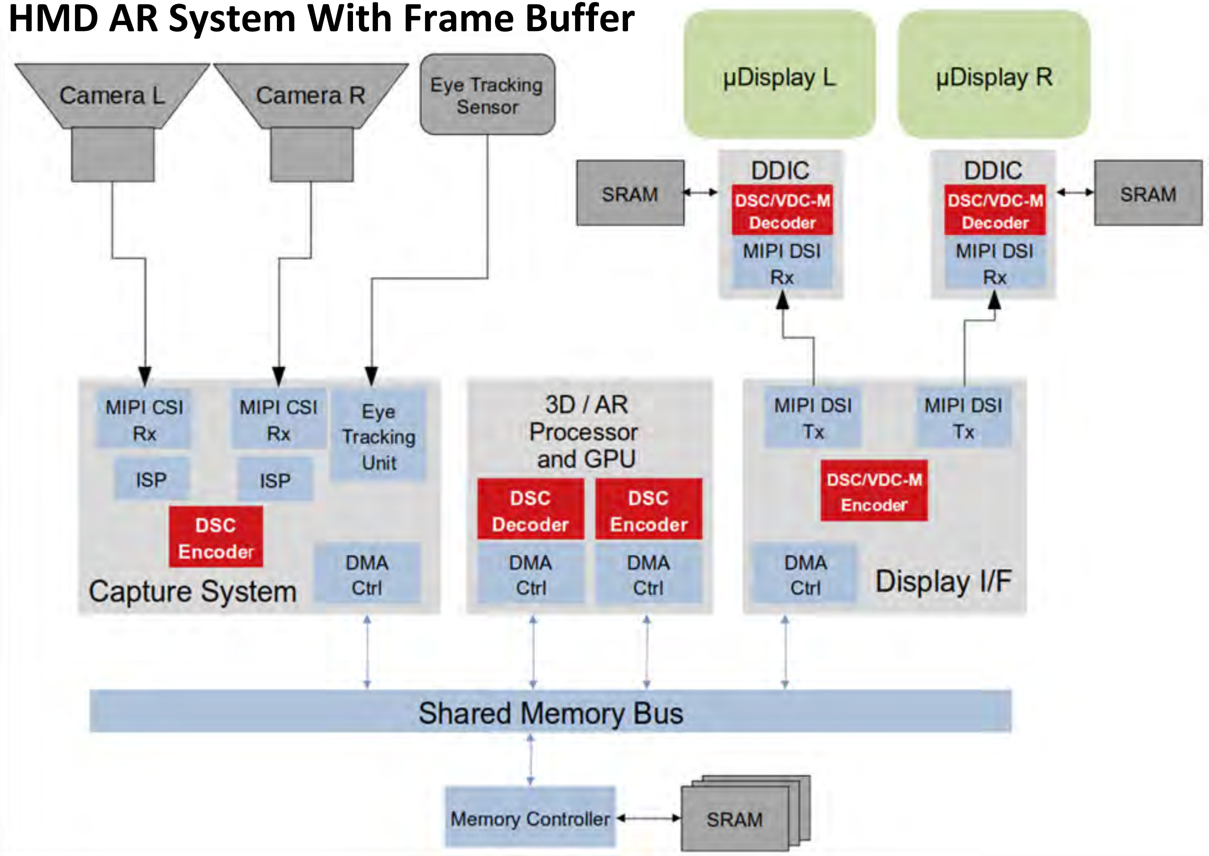
VDC-M to Fulfill Future AR/VR Requirements

Predicted industry trends:

1. Resolutions per eye will increase over time from 2k x 2k in 2019 to **8K x 8K in 2025**
2. It is believed that very few people see a difference beyond 8K x 8K per eye:
    - This is about **60 pixels per degree** for 273 degrees horizontally
    - It allows 220 degrees plus 25 degrees of overlap between the eyes
3. Refresh rates required is between 120 to 240Hz to meet human perception limits
4. Pixel resolution of 12bpc will be required by 2025

Use Case: AR Head-Mounted Display (HMD)

HMD AR System With Frame Buffer



Compression could be applied to:

- Images captured by 3D camera
- Video and graphics processed by AR processor and GPU
- L/R video streams sent to micro-displays (DSI-2 Link)
- Video stored inside micro-display driver IC (Frame Buffer)

Benefits

- Lower bandwidth & EMI
- Smaller RAM buffers
- Power saving, longer battery life
- Low latency

Market Focus

Automotive

Modern Automotive Cockpit Displays

Display Type	Example Size (Inches)	Example Resolution
Left and Right-Side Mirror Displays	7”	1280x800
Driver Instrument Display	12.3”	3840x1440
Center Information Display	12.3”	3840x2160
Extended Co-Driver display	12.3”	3840x2160
Lower Control Display	12.4”	3840x2160

Modern Automotive Cockpit Displays

Digital Side View Mirror

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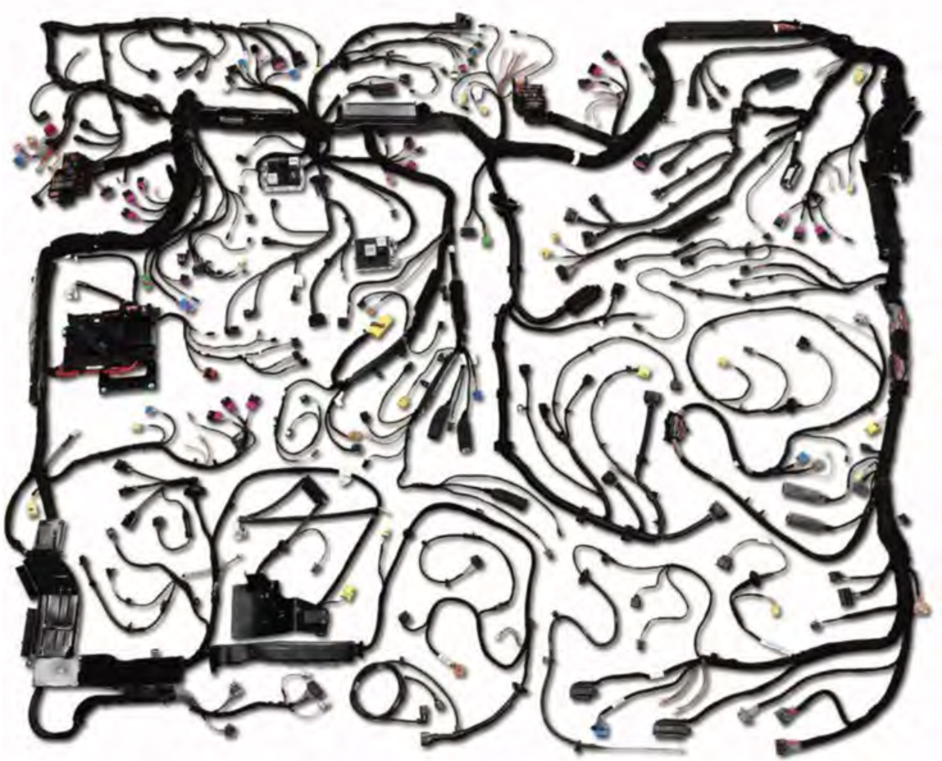
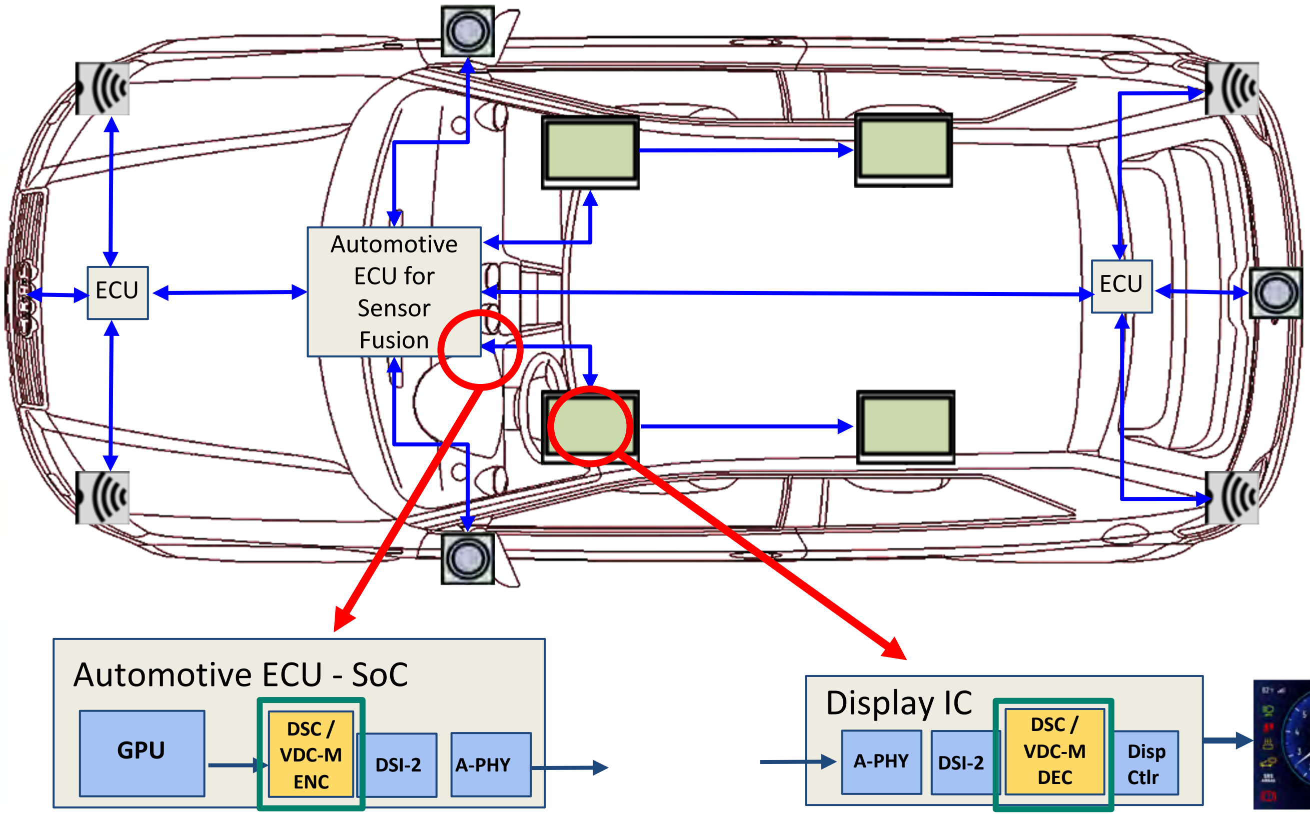
More Displays Yes...
But More Cables Is NOT The Solution



- Wiring harness is the 3rd highest cost component in a car (behind engine and chassis) comprising 50% of the cost of labor for the entire car
- 3rd heaviest component (after the chassis and engine)*
- Reliability, EMI, and signal integrity are major challenges
- On electric only vehicles, power consumption of video links must be minimized
- LESS cables reduces problems!

* Source: Delphi, Inc.

Car Display Systems Using Video Compression

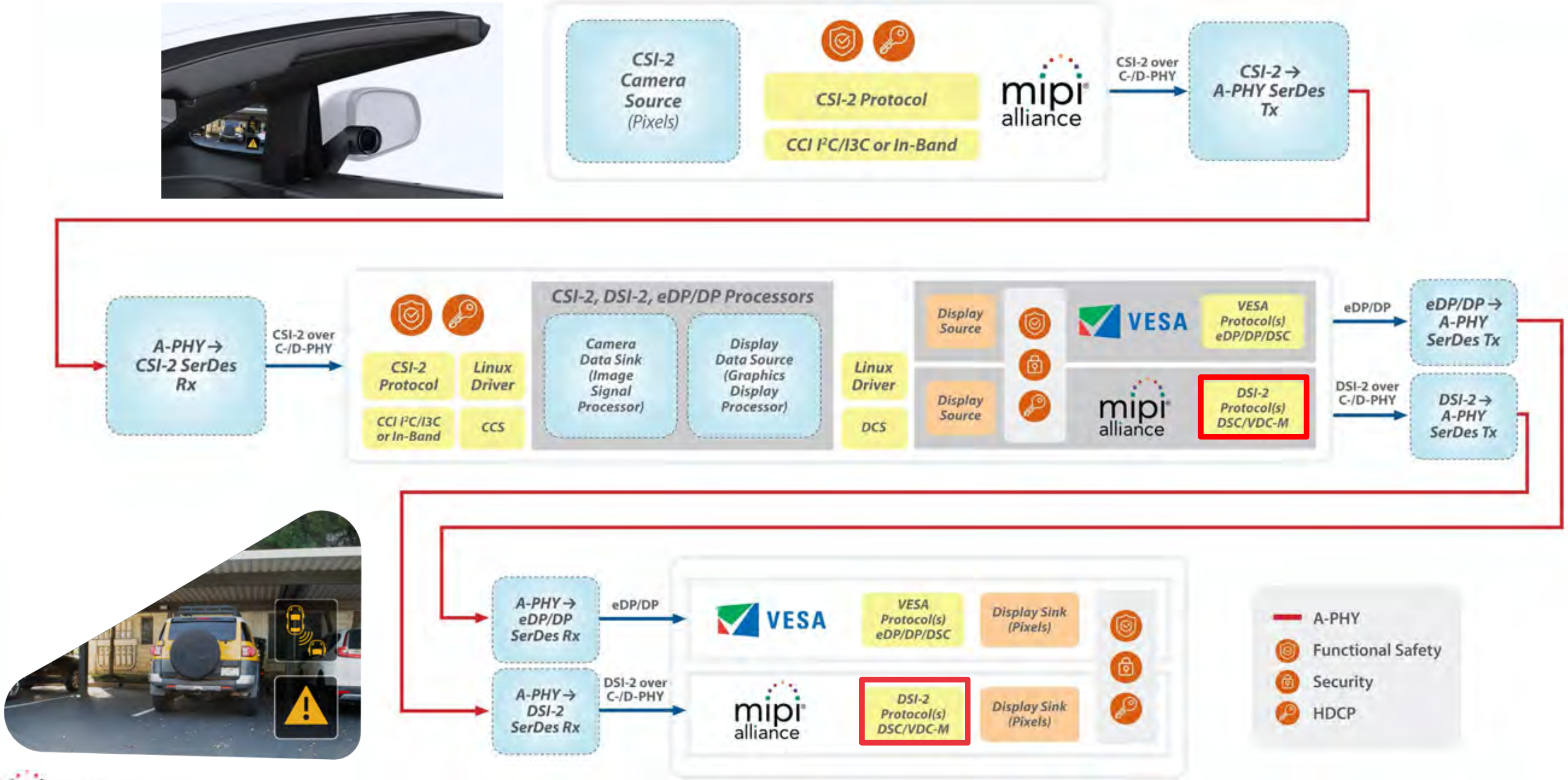


Benefits of using video compression:

- Reduced bandwidth for multiple feeds
- Enhance image quality (enabling HDR with same bandwidth)
- Savings on expensive cabling
- Lower EMI
- Reduce power

MASS: MIPI Automotive SerDes Solutions

A Vision for End-to-End Systems



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MASS Display Use-Cases and Architecture

- **MASS: MIPI Automotive SerDes Solutions**
  - Foundation is the next generation MIPI Automotive-PHY specification (MIPI A-PHY^{SM})
    - 5 speed gears (2, 4, 8, 12 and 16 Gbps) with roadmap to 48 Gbps and beyond
  - Leverages MIPI low-power, low EMI display and camera protocols
  - Includes new end-to-end functional safety and security improvements
  - **Includes and promotes standardized visually lossless compression (DSC/VDC-M) for displays**
    - **Low latency, low footprint & high visual quality**
- **MIPI whitepaper "Validating the Use of Compression for Automotive Displays"**
  - A study verifying VDC-M's visually lossless compression properties demonstrates that MIPI DSI-2 offers a solution to the growing bandwidth challenges in next-generation vehicles
  - For automotive applications, VDC-M 6x compression is visually lossless
  - Download: https://resources.mipi.org/download-mipi-whitepaper-automotive-display-compression

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Automotive Display Bandwidth Requirements

Display Parameters							Total Bandwidth (Gbps)			
Display Config	Driver Instrument Display (DID) 12"	Centre Information Display (CID) 10.2"	Lower Control Display (CLD) 10.2"	CoDriver Display (CDD) 12"	Left Side Mirror 3.6"	Right Side Mirror 3.6"	Src 24-Bit	Src 30-bit	VDC-M Comp 24-bit (6:1)	VDC-M Comp 30-bit (6:1)
1	1280x720	1280x720	None	None	None	None	2.846	3.558	0.474	0.593
2	1920x720	1920x720	1920x720	None	None	None	6.405	8.007	1.068	1.335
3	3840x1440	3840x1440	3840x1440	3840x1440	None	None	33.46	41.824	5.577	6.971
4	3840x2160	3840x2160	3840x2160	3840x2160	640x390	640x390	50.97	63.694	8.495	10.616
5	5120x2160	3840x2160	3840x2160	5120x2160	640x390	640x390	59.156	74.136	9.859	12.356
6	5120x2160	7680x2800	3840x2160	5120x2160	None	None	78.954	98.89	13.159	16.482
7	7680x2800	7680x2800	7680x2800	7680x2800	640x390	640x390	133.242	166.558	22.207	27.760

Uncompressed Rates

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4	3840x2160	3840x2160	3840x2160	3840x2160	640x390	640x390	50.97	63.694	8.495	10.616
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Compressed Rates

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Compression For Automotive Displays

Is it Safe?

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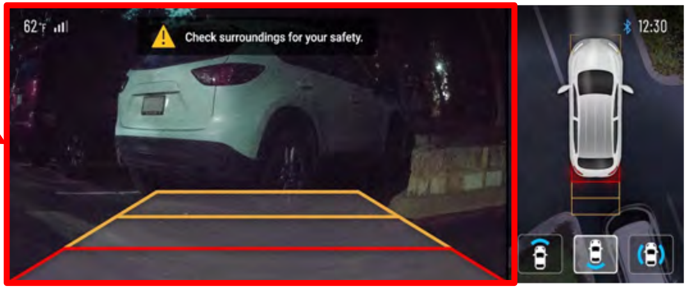
Functional Safety in Display Applications

- Display systems, when involved in ADAS, are required to meet ASIL and ISO 26262 requirements

Safety Critical Information!



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Functional Safety in Display Applications

- **Safety Goals must be clearly defined**
- **There is no standardized definition of a display failure in a vehicle…**
  - “Is a single pixel “glitch” ok?”
  - “Is a small portion of a frame corrupted for a second ok?”
  - “Is a complete frame corrupted for 1/60 sec ok?”
  - “Is a image showing darker than expected ok ?”
  - “Is it an issue if the video is frozen for ½ second?”
- **For displays that contain safety critical information, no compromises are acceptable!**

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Functional Safety Assessment In a Nutshell

- **Failure Modes & Effects** are identified (how and where a failure occurs)
- **Diagnostic** mechanisms are added to detect when a failure happens
- For each failure mode, each diagnostic performance (fault coverage score in %) is determined for various types of fault: **Single Point Faults**, **Transient Faults, Latent Faults,** etc.
- This whole assessment is done through a complete **FMEDA (Failure Mode, Effects, and Diagnostics Analysis)**
- Required overall performance (for each type of fault) depends on the safety level required (ASIL A to ASIL D)

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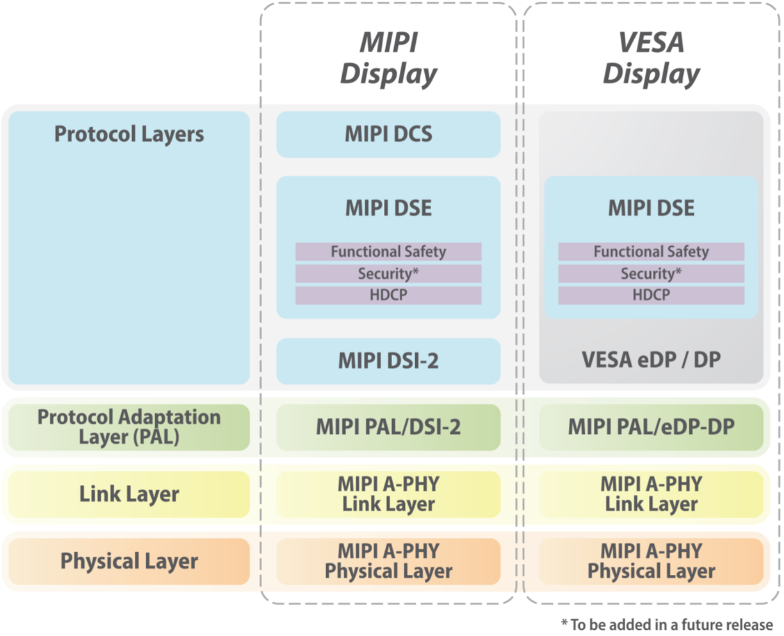
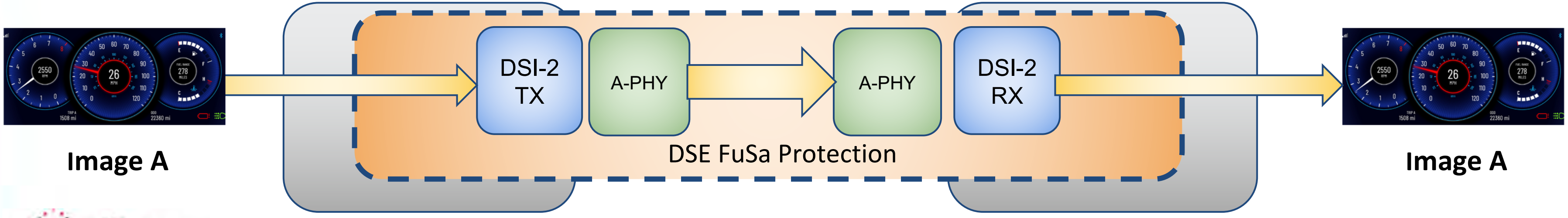
MIPI DSE - Display Service Extensions

MIPI DSE℠ protocol adds Functional Safety (FuSa) features for displays:

- SEP
- Message Counters
- CRCs





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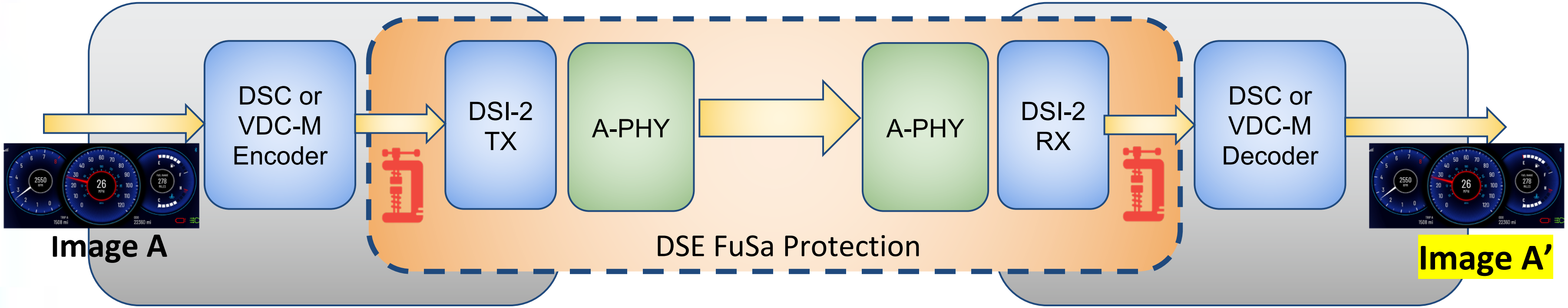
Additional Challenge with Video Compression

- When compression is used, the compressed image payload and DSI-2 packets are protected by DSE FuSa, but not the image content itself
- However...
  - Failures could occur during the encoding or decoding process
  - Even when there is no failure, the decoded image is NOT identical to the original image (it is visually lossless but not bit exact)



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FuSa with DSC & VDC-M Video Compression

- For DSC and VDC-M, the decoded image is generated during the encoding process

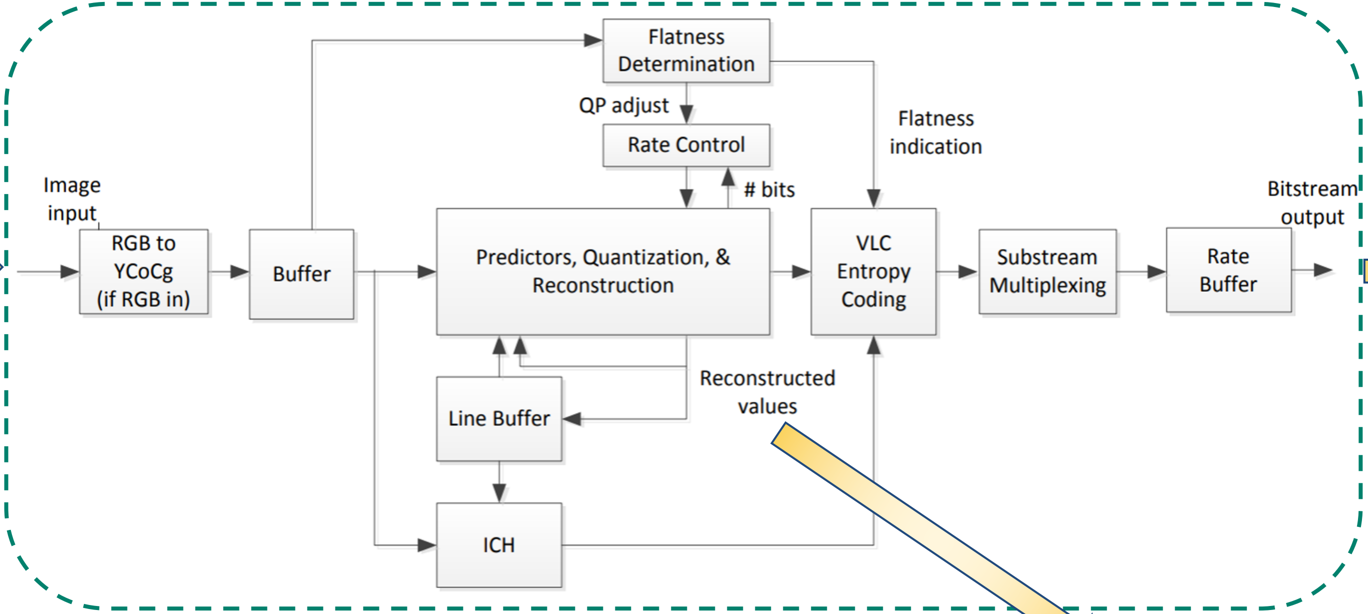


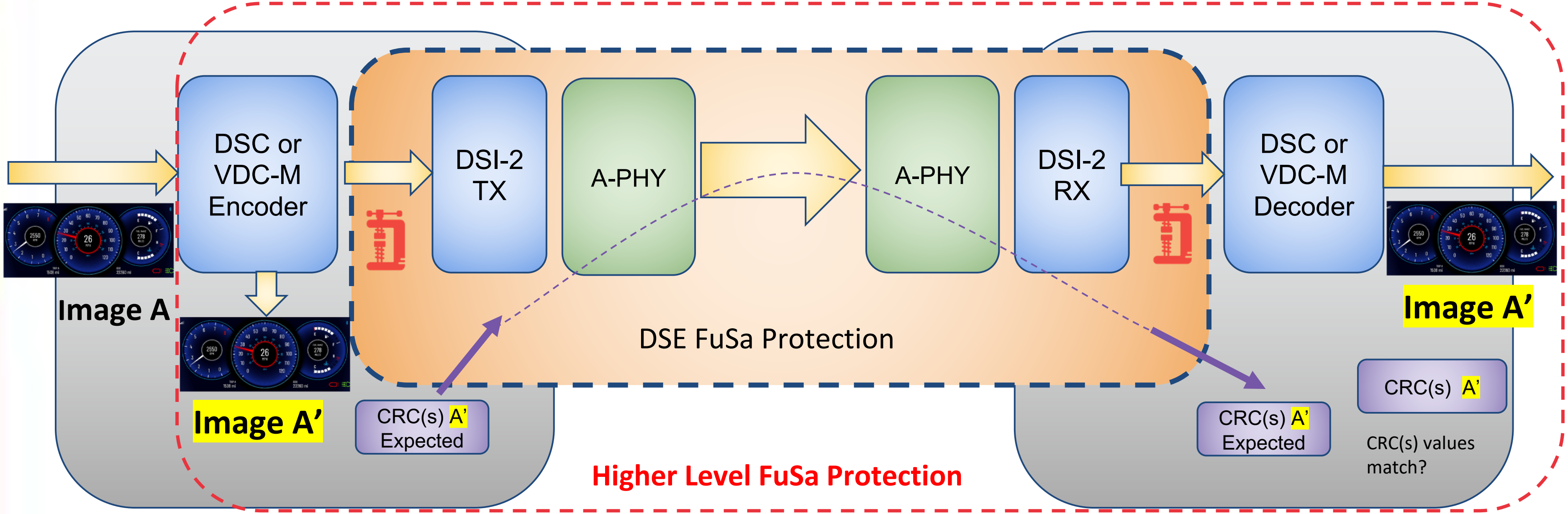
Image A

Image A'

Source: VESA DSC Whitepaper https://www.vesa.org/wp-content/uploads/2014/04/VESA_DSC-ETP200.pdf

FuSa with DSC & VDC-M Video Compression

- The integrity of the decompressed image in the display can be verified by comparing the CRC(s) of the decoded image generated by the encoder with the CRC(s) of the decoded image generated by the display



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FuSa with DSC & VDC-M Video Compression

- **Benefits of the Decoded Image CRC(s) approach:**
  - Easy to implement, **low area footprint**, removes the need for duplicated logic (a common technique for fault detection)
  - **Very high safety goal violation coverage** for both Single Point Faults (SPF) “Stuck bits” and Transient Faults (TF) “Glitches”, for the whole display subsystem
  - Using multiple CRC(s) per frame, a CRC value per “slice” helps to identify which parts of the image has corruption
- With the addition of Decoded Image CRC(s) when DSC or VDC-M compression is used, it becomes possible to meet the safety goals

Conclusions

- Video compression is essential for meeting the bandwidth requirements of current and future display applications
- VESA® DSC & VDC-M offer proven compatibility with the MIPI DSI-2℠ interface and visually lossless performance
- Integrating video compression into a design and achieving desired display features can be complex
- IP and IP subsystem solutions are available to help designers lower risk and achieve faster integration

Thank you….now time for questions

MIPI DSI-2 Homepage: www.mipi.org/specifications/dsi-2

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