Evolution of MIPI CSI-2 Imaging Conduit

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Outline

• MIPI Introduction
• Evolution of MIPI CSI Imaging Conduit
• Q&A
About MIPI Alliance

Peter Lefkin
MIPI Alliance Managing Director
About MIPI Alliance

MIPI is a global, collaborative organization founded in 2003 that comprises 300+ member companies spanning the mobile and mobile-influenced ecosystems.

**MIPI’s mission:**
To provide the hardware and software interface specifications device vendors need to create state-of-the-art, innovative mobile-connected devices while accelerating time-to-market and reducing costs
MIPI Alliance Member Ecosystem

- Automotive OEMs
- Application Processor Developers
- Device OEMs
- Consumer Electronics (Cameras, Tablets, PCs/Laptops, Peripherals, Wearables)
- Software Providers
- Semiconductor Companies
- Test Equipment Companies
- Test Labs
- IP and VIP Providers

MIPI Alliance Member Ecosystem

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What Does MIPI Alliance Do?

Define and promote specifications focusing on the mobile interface but applicable to IoT, auto & more

Provide members with access to licenses as needed to implement and market specified technologies

Complement existing standards bodies through collaboration
MIPI’s focus has always been on mobile. In fact, every smartphone on the market today has at least one MIPI specification.

With the development of new mobile-influenced markets, you can now find MIPI specifications in a variety of products:
A System of Mobile Interfaces

To date, MIPI has developed more than 45 specifications. Our leading specifications:

- CSI, CCS
- DSI
- SoundWire
- RFFE
- I3C
- UniPro

Physical layers:

- C-PHY
- D-PHY
- M-PHY
Evolution of MIPI CSI-2 Imaging Conduit

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Singularity

CSI
LRTE | USL | IENC | SROI | RAW | CCS | CTS

Unified Imaging Conduit for AI Vision Spanning Multiple Platforms

A smart connected device is blessed with cognitive computing that uses AI and perception awareness to sense, learn, reason, and make decisions when interacting with individuals or surrounding situations.
Process

• Use Cases & Applications
• Unified Software Driver
• Features and Capabilities
• End-to-end Conformance Test Suite
Evolving MIPI CSI

**Ingredients**
Photon Collectors, Transistors, Optics, Emitters, Algorithms

**Applications**
Broad Spectrum of Imaging & Vision Use cases targeting multiple platforms

MIPI CSI-2 Releases
Two different CSI architectures

- CSI-2
  - Transport
  - PHY
    - A-PHY
    - C-PHY
    - D-PHY
  - Applications
- CSI-3
- UniPro
- M-PHY
CSI-2 over C/D-PHYs

CSI-2 Imaging over D-PHY

Image Sensor

CSI-2 TX

D-PHY TX
(6-pins)

Periodic clock

Data

CSI-2 RX

D-PHY RX
(6-pins)

Application Processor

I2C Compatible 2-wire Camera Control

AF  Gyro  OIS  Flash

Pin compatible

CSI-2 Imaging over C-PHY

Image Sensor

CSI-2 TX

C-PHY TX
(6-pins)

Embedded clock & data

I2C Compatible 2-wire Camera Control

AF  Gyro  OIS  Flash

MEMS

Application Processor

CSI-2 RX

C-PHY RX
(6-pins)
Algorithm is King

- Unified Imaging Software Driver
- Enable Image Sensor Capabilities for Vision Com
- Accelerate Bring up on Reference Platforms
CSI-2 CCS

- Vertical Flip | Horizontal Mirroring

- Sub-Sampled Readout | Binning | Digital Crop
Deep Neural Networks

Myriad X Hybrid Arch Deep Neural Network
8 Cameras using 16 MIPI Lanes - 700 MP/s
Drone Collision Avoidance (DJI SPARK)

LRTE

- Dramatically Improve Sensor Aggregation
- Optimal Transport Preserving Integrity
- Real-time Perception & Decision Making
- Phase out EOS &IL Impediments
Detailed CSI-2 System Analysis & Benefits of Using LRTE PDQ

System 1: CSI-2 v2.0 over C-PHY v1.2 (3.5 Gbps/lane or 8Gbps/lane)
- 24 Gbps using 3 lanes (requires 9 wires)
- CSI-2 v2.0 supports up to 32 Virtual Channels over C-PHY

Multi Sensor Aggregator with each sensor configured as
- 1920 x 1200 (2.3MP), 12 BPP, 60 FPS

Image Sensor Packet Transport
- 1920 pixels x 1280 pixels = 230400 bits per Horizontal Row Long Packet (LP)
- 230400 bits / 240bps = 0.960 us / LP (CSI-2 Payload; ignoring PH/PF)
- Packet Header + Packet Footer = 336+48 = 384 bits
- 23424 bits / 240bps = 0.976us / LP_PHF (CSI-2 Payload with PH and PF)

CSI-2 v2.0 with Legacy C-PHY Packet Delimiters:
- LP Delimiter (SoT/EoT) = ~0.3 us
- Total Time per LP_PHF = 1.276 us
- Packet Delimiter Overhead = 23.5%
- Time per Image Frame = 1.276us x 1200 x 1.53 ms (ignoring F5/F6)
- Stream 60 frames from single image sensor requires: 1.53ms x 60 = 91.87 ms
- Maximum Supported Image Sensors on an Aggregator = 10

FLOOR[10/0.9187] = FLOOR[10.88]

CSI-2 v2.0 with LRTE PDQ:
- Time per Image Frame = 0.976us x 1200 = 1.171 ms
- Stream 60 frames from single image sensor requires: 1.172ms x 60 = 70.27 ms
- Maximum Supported Image Sensors on an Aggregator = 14

FLOOR[10/0.9187] = FLOOR[14.23]

Benefits of CSI-2 v2.0 with LRTE PDQ:
- Frame Transport Efficiency Improvement: 23.5%
- Additional Supported Image Sensors on Aggregator: +4 (over the same channel)
- Alternatively, reduce toggle rate / wires

<table>
<thead>
<tr>
<th>Considerations</th>
<th>%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Legacy PD Hor Row Overhead</td>
<td>23.51</td>
</tr>
<tr>
<td>Legacy PD Max Supported Sensors</td>
<td>10</td>
</tr>
<tr>
<td>LRTE PDQ Hor Row Overhead</td>
<td></td>
</tr>
<tr>
<td>LRTE PDQ Frame Transport Efficiency Impact</td>
<td></td>
</tr>
<tr>
<td>(reduce: power / wire / toggle)</td>
<td>23.35</td>
</tr>
<tr>
<td>LRTE PDQ Max Sensors Supported</td>
<td>14</td>
</tr>
<tr>
<td>LRTE PDQ Additional Supported Sensors</td>
<td>40.00</td>
</tr>
</tbody>
</table>
USL

- Long Reach
- Wire Reduction
- Encapsulation
- Secure Channel

**CSI-2 USL over D-PHY**

Image Sensor Module

- CSI-2 TX
- D-PHY TRX
- D-PHY RX
- CSI-2 RX

Application Processor

- Periodic FWD clock
- Camera Control Interface (CCI) over I2C / I3C / SPI
- GPIOs

**CSI-2 USL over C-PHY**

Image Sensor Module

- CSI-2 USL
- C-PHY TRX
- C-PHY RX
- EMB_CD_TRIO_0

Application Processor

- Camera Control Interface (CCI) over I2C / I3C / SPI
- GPIOs
IENC

- Enterprise Security
- Pixel Authentication
- VC Mapped Interleaved Encryption
- Threat Model & Use Cases (GCM / AES)
## DPCM Objective Qualification

- Enable 10-bit compression of RAW-12 video image with better IQ than prior version 12-8-12
- Reduce maximum absolute error of single-bit change in pixel value by a factor of 4.43x
- Qualified 5 degree slanted edge input image with low, medium, and high illumination levels:
  - 12-10-12 virtually indistinguishable from original image
  - MTF frequency response analysis closely tracks the original (HI/MI/LI - LC/MC/HC)
- Benefits include Link BW reduction cost savings

### Use Case

<table>
<thead>
<tr>
<th>Use Case</th>
<th>Per-Lane 4-Lane Bit Rate (Gbps)</th>
<th>12-10-12 DPCM Enables Use of:</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>10 bpp</td>
<td>D-PHY</td>
</tr>
<tr>
<td>4Kp60 or 1080p240</td>
<td>1.485</td>
<td>v1.1</td>
</tr>
<tr>
<td>16M (4:3) @ 30 fps</td>
<td>1.45</td>
<td>v1.1</td>
</tr>
<tr>
<td>20M (16:9 crop) @ 30 fps</td>
<td>1.371</td>
<td>v1.1</td>
</tr>
<tr>
<td>32M (4:3) @ 24 fps</td>
<td>2.263</td>
<td>v1.2</td>
</tr>
</tbody>
</table>
PSD Reduction

CSI-2 over D-PHY PSD emission reduction with scrambling (data lanes)

CSI-2 over C-PHY PSD emission reduction with scrambling (embedded clock and data)
SROI

- Phase 1 EOY 2018 Single Frame
- Phase 2 EOY 2019 Multi Frame
- ARCH: Central | Edge | Hybrid

Functional Safety

APPLICATION SPECIFIC PAYLOAD

LPS  SoT  Data ID  16-Bit Word Count (l.s. byte first)  VCX + ECC  Data 0  Data 1  Data 2  Data 3
Data WC-11  Data WC-10  Data WC-9  Data WC-8

Functional Safety Packet Footer

Message Counter (MC)

Checksum CRC (CS)

LPS  SoT  Data ID  16-Bit Word Count (l.s. byte first)  VCX + ECC  Data 0  Data 1  Data 2  Data 3
Data WC-11  Data WC-10  Data WC-9  Data WC-8

32-bit PACKET HEADER (PH)

32-bit PACKET FOOTER (PF)

PACKET DATA:
Length = Word Count (WC) * Data Word Width (8-bits). There are NO restrictions on the values of the data words

16-bit CRC-Orig (Optional) (l.s. byte first)
16-bit Row ID (Optional) (l.s. byte first)
16-bit 8-bit Source ID (Optional)
16-bit Message Counter (l.s. byte first)
16-bit Checksum (l.s. byte first)

EoT  LPS
Graceful Link Degradation

Image Sensor → Lane1 → Imaging & Vision Processor

Image Sensor → Lane1, Lane2, Lane3 → Imaging & Vision Processor

Image Sensor → Lane1, Lane3 → Imaging & Vision Processor

Image Sensor → Lane1, Lane2 → Imaging & Vision Processor
End-To-End Imaging Conduit

CSI-2 FEATURES
- SROI
- IENC
- USL_GTA_BET
- FUNC_SAFETY
- F_NF_ERR
- LRTE_ALP_PDQ
- GLD
- H_F_DUPLEX
- T_S_SYNC

SNS MODULE
- HEALTH_MONITOR
- IRX
- VCM
- GYRO
- ACC
- EPROM
- LED
- LASER
- ...

ARCH
- CENTRAL
- EDGE / DISTRIBUTED
- HYBRID

APP
- ISP
- CVE
- GFX

PHY
- DISCRETE
- INTEGRATED
• Mid-Range solutions targeting Seoul FTF
## Topology

<table>
<thead>
<tr>
<th>Form Factor</th>
<th>Mobile</th>
<th>Phablet</th>
<th>Tablet</th>
<th>2:1</th>
<th>Notebook (Hinge)</th>
<th>AIO / IOT</th>
<th>Panel</th>
<th>AR/VR</th>
<th>Drones (Commercial)</th>
<th>Robotics &amp; Medical</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reach</td>
<td>4”</td>
<td>6”</td>
<td>8”</td>
<td>12’</td>
<td>15”</td>
<td>30”</td>
<td>40”</td>
<td>60”</td>
<td>24”</td>
<td>60”</td>
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<tr>
<td>Cable</td>
<td>Flex</td>
<td>Flex</td>
<td>Flex</td>
<td>STP</td>
<td>UTP (thin) Flat behind / round edge</td>
<td>STP</td>
<td>STP</td>
<td>STP</td>
<td>Flex (lower weight)</td>
<td>STP</td>
</tr>
<tr>
<td>USL</td>
<td>Optional</td>
<td>Optional</td>
<td>Optional</td>
<td>Optional</td>
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<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>SCR / SSC*</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>D-PHY*</td>
<td>1080p, 10 BPP, 30 FPS using 1 Lane / 3 wires / 0.69 Gbps  (SSC recommended for D-PHY FWD Periodic Clock)</td>
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<tr>
<td>C-PHY</td>
<td>1080p, 10 BPP, 30 FPS using 1 Trio / 3 wires / 0.30 GSp</td>
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<td>A-PHY</td>
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<tr>
<td>Topology</td>
<td>FR4-FLEX-FR4</td>
<td>FR4-FLEX-FR4</td>
<td>FR4-FLEX-FR4</td>
<td>FR4-STP-FR4</td>
<td>FR4-STP-FR4</td>
<td>FR4-STP-FR4</td>
<td>FR4-STP-FR4</td>
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<td>FR4-STP-FR4</td>
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Summary

• CSI-2 imaging features mapped to AI & vision
• Unified imaging SW driver
• Comprehensive ETE Conformance Test Suite
• Natively support short / mid / long range platforms
• Solutions targeting IoT platforms at the Seoul FTF
Questions

https://mipi.org/working-groups/camera