Imaging interface advancements and development to meet the needs of mobile and mobile-influenced industries

mipi alliance

February 17, 2016

Haran Thanigasalam

Intel Senior Platform Architect | MIPI Camera WG Chair

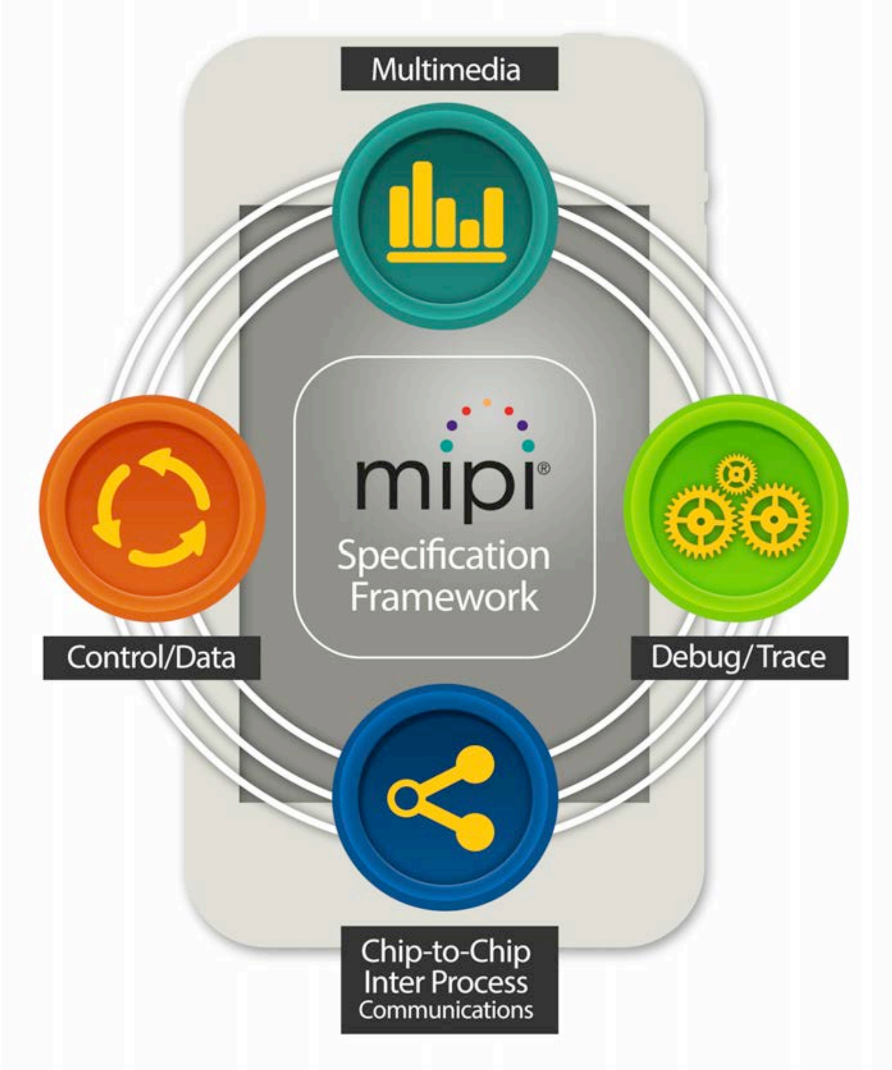
Brief overview from Peter Lefkin

Managing Director, MIPI Alliance

About MIPI Alliance

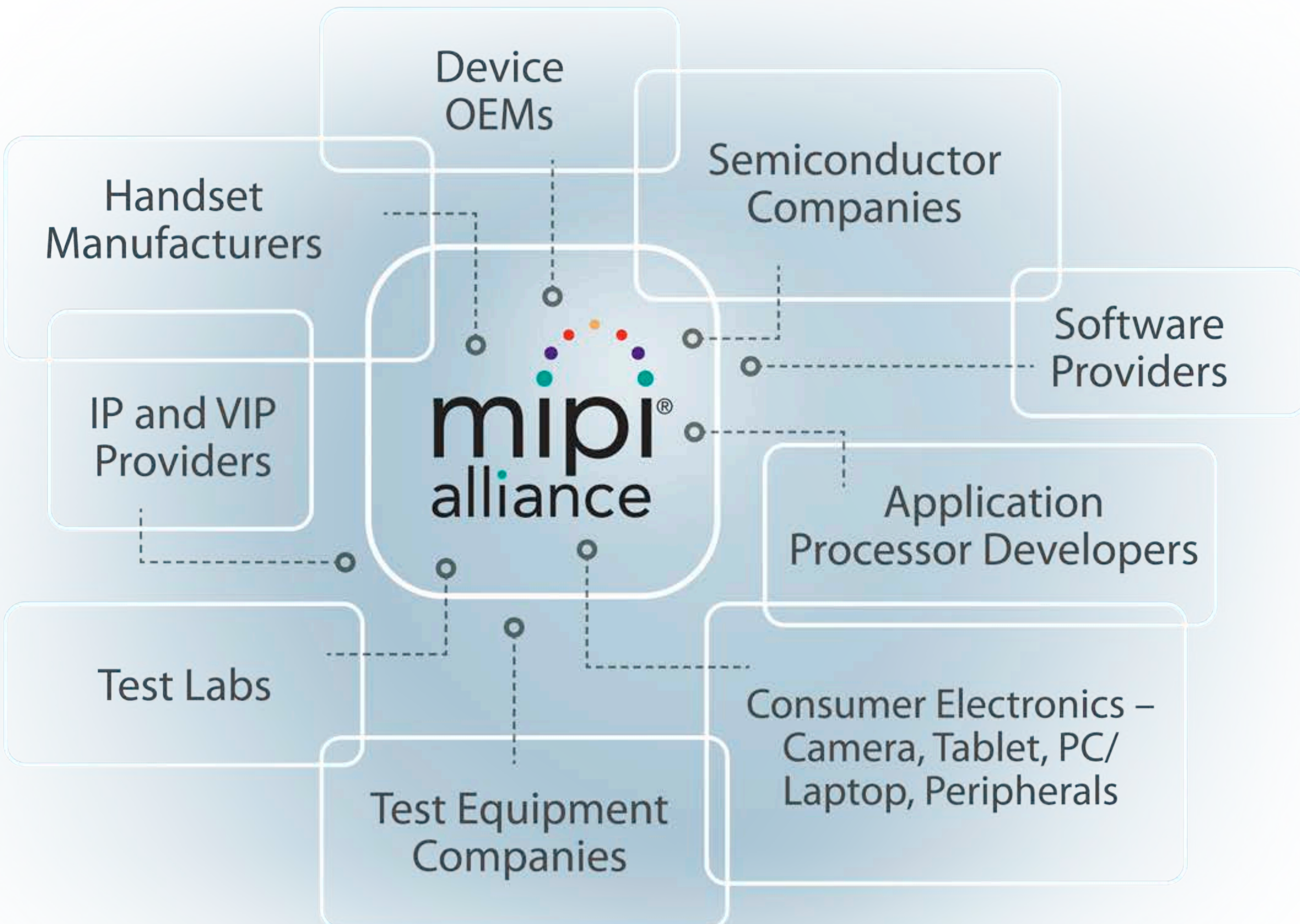
We are a global, collaborative organization comprised of over 280 member companies spanning the mobile and mobile-influenced ecosystems.

MIPI Alliance is leading innovation in mobile interface technology.

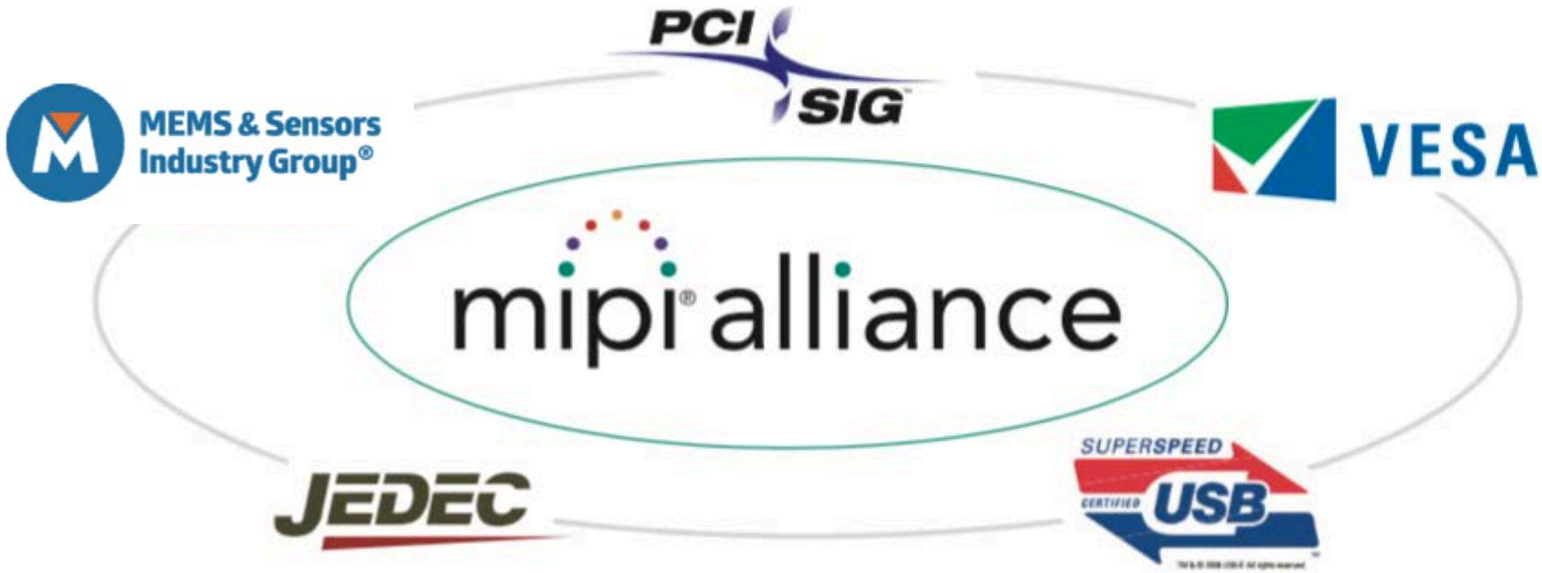


mipi alliance

MIPI Alliance Member Ecosystem



Partners



mipi alliance

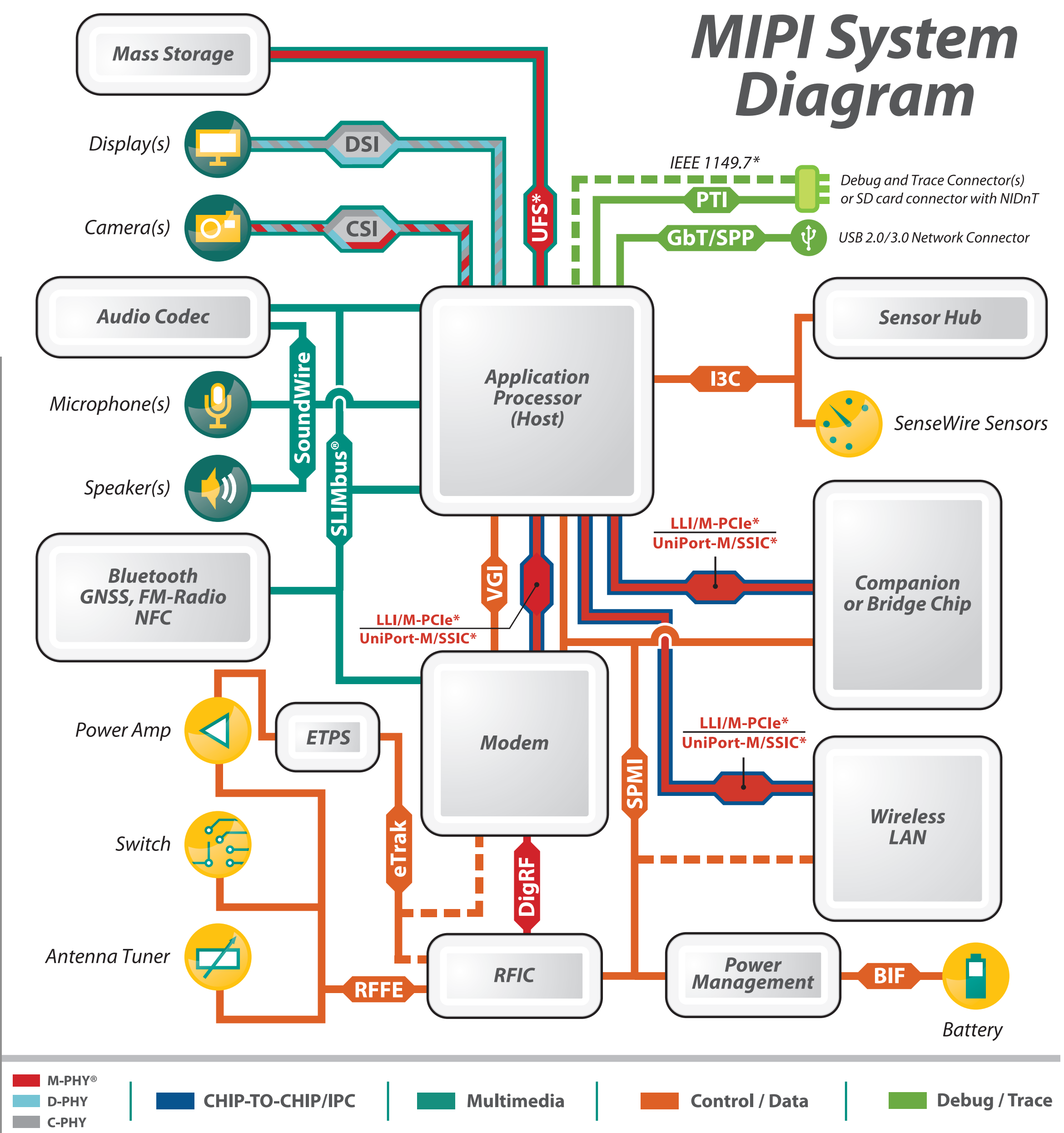
Active Technical Working Groups

Camera	Debug	Display	Low Latency Interface
Low Speed Multipoint Link	PHY (C/D/M)	Reduced Input Output	RF Front End
Sensor / I3C[SM]	Software	Test	UniPro[SM]

mipi alliance

Roadmap

MIPI Alliance continues to evolve its Roadmap to meet the needs of the mobile and mobile-influenced industry with new and revised specifications.



mipi alliance

Overview

Generational advancements and development of MIPI CSI imaging interface to meet the needs of Mobile and beyond applications including:

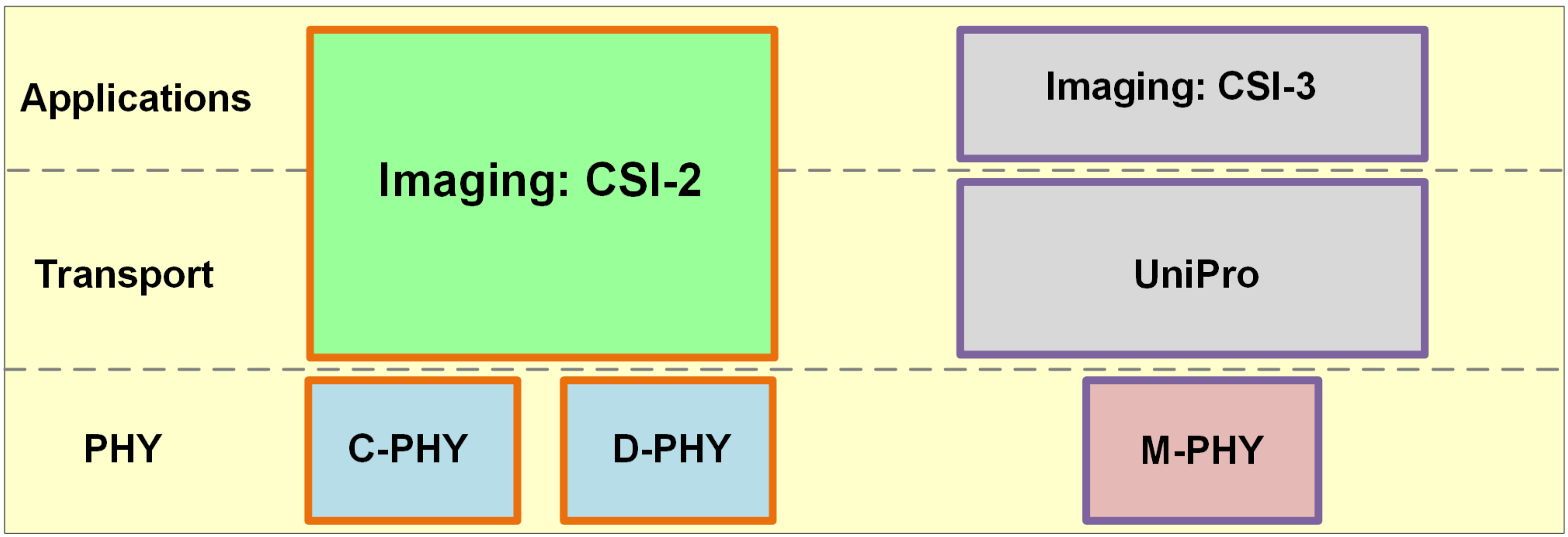
- Two equally capable MIPI imaging interface architectures
  - CSI-2 over C/D-PHYs
  - CSI-3 over UniPro and M-PHY
- Provision to mitigate PSD emissions
- Extended Virtual Channels
- High Dynamic Range enhancements
- Latency Reduction and Transport Efficiency
- Always On Metadata and Pixel Transfer
- Differential Pulse Code Modulation

mipi alliance

Two equally capable imaging interface architectures

CSI-2 protocol contains transport and application layers, and natively supports: **C-PHY**, **D-PHY**, or **combo C/D-PHY**

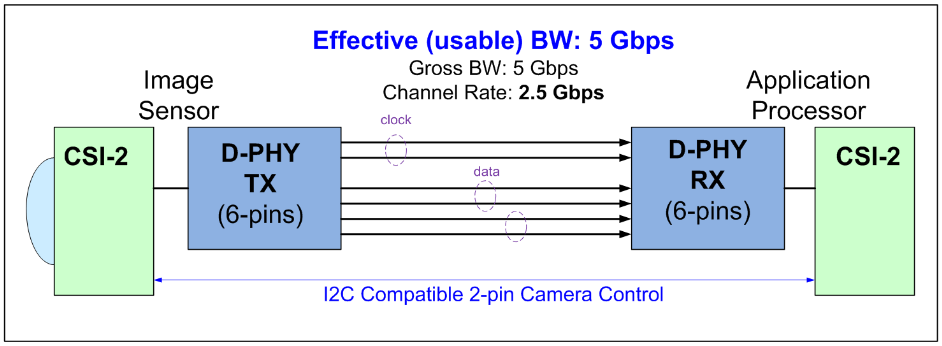
CSI-3 application stack connects to **UniPro** transport layer, which in turn bolts onto **M-PHY**



mipi alliance

Imaging Development

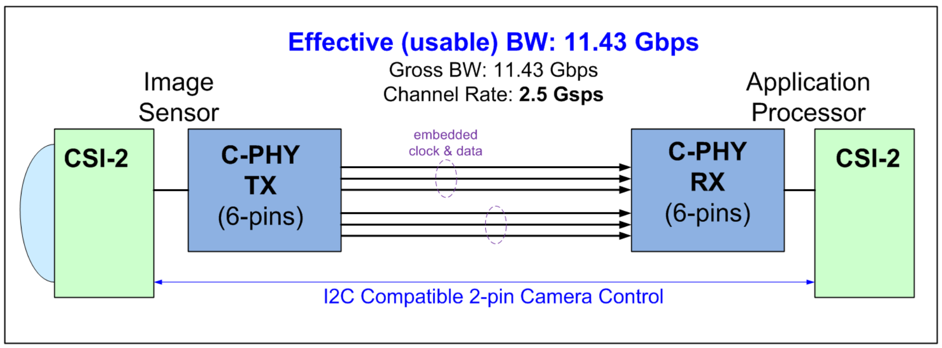
CSI-2
D-PHY



- CSI-2 D-PHY 1.2 extension Pix BW scales linearly
  - 2.5 Gbps Channel delivers 10 Gbps over 4 data lanes and a clock lane (10 D-PHY pins).

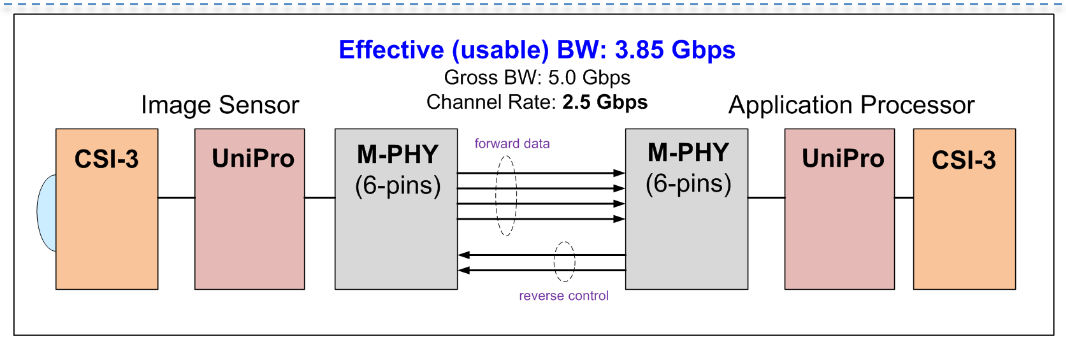
Pin compatible coexistence supports
CSI-2 over combo C/D-PHY solutions

CSI-2
C-PHY



- CSI-2 C-PHY 1.0 extension Pix BW benefit from $\log_2 5$ mapping gain
  - 2.5 Gsps Channel delivers17.1 Gbps over 3 lanes (9 C-PHY pins), or 22.7 Gbps over 4 lanes (12 C-PHY pins)

CSI-3
UniPro
M-PHY



- CSI-3 application stack connects to UniPro and M-PHY

- supports networking features using fixed gear channel rates of up to 5.8 Gbps.

- Rev control may run lower rate if asymmetric gears are supported by Image Sensor and Application Processor.

mipi alliance

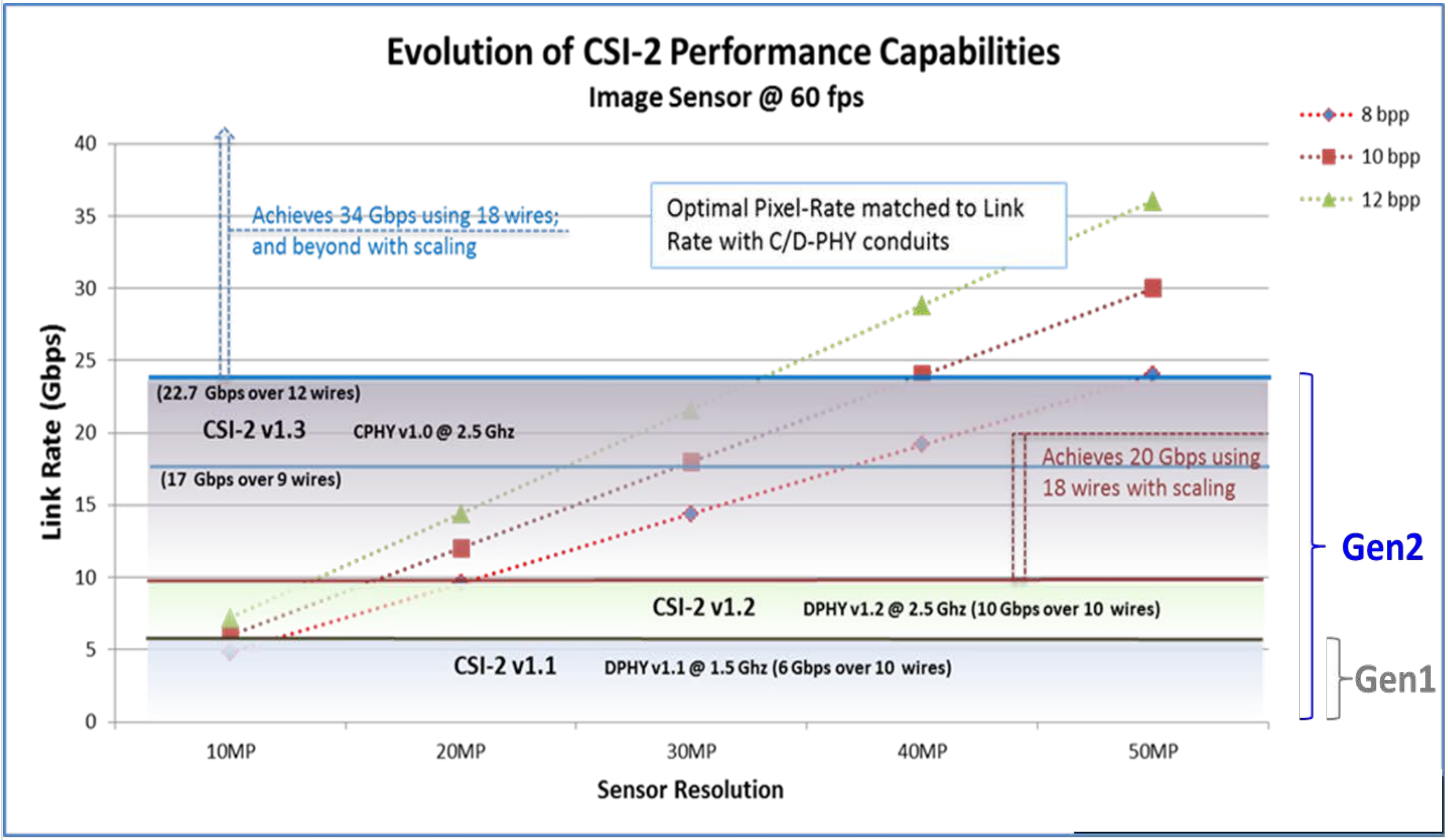
Solutions for popular imaging use case

4K @ 30 fps and 12 BPP using CSI-2					
Required MIPI Specs (IPs)	Required PHY pins	Required Lane Rate	Required BW	Variable Link Rate	Control Interface
[CSI-2] [D-PHY]	6	1.78 Gbps	3.56 Gbps	Yes	I2C
[CSI-2] [C-PHY]	3	1.55 Gsps	3.56 Gbps	Yes	I2C

4K @ 30 fps and 12 BPP using CSI-3					
Required MIPI Specs (IPs)	Required PHY pins	Required Lane Rate	Required BW	Variable Link Rate	Control Interface
[CSI-3] [UniPro] [M-PHY]	4	5.0 Gbps	3.56 Gbps	No	In-band

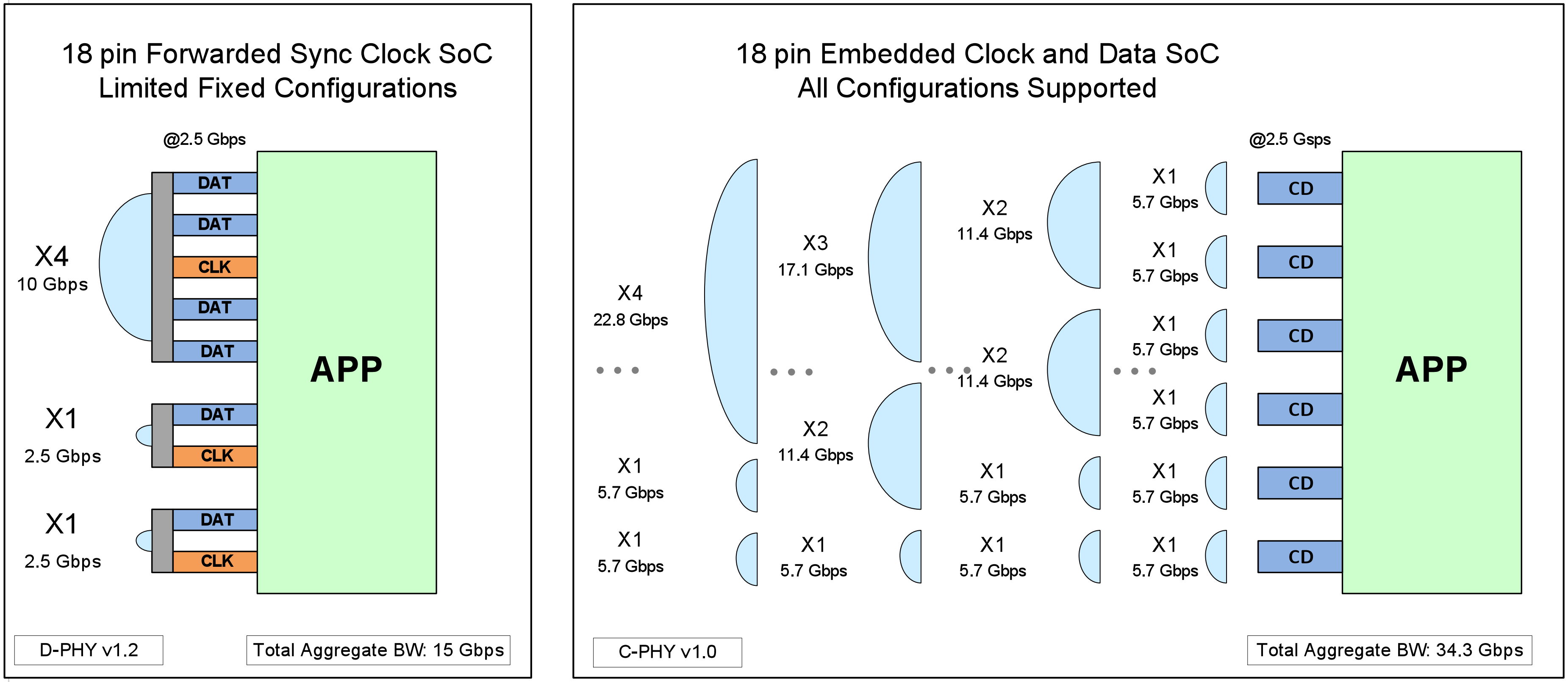
mipi alliance

CSI-2 v1.3 over C/D-PHY Evolution & Performance



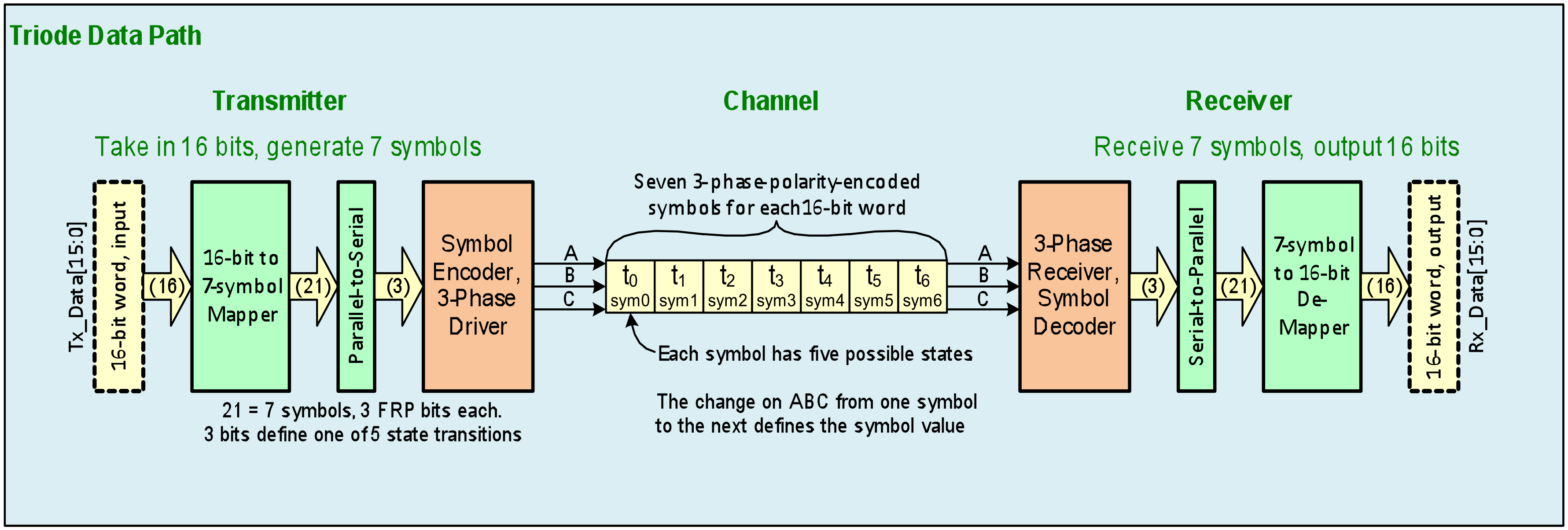
CSI-2 Benefits of Embedded Clock & Data

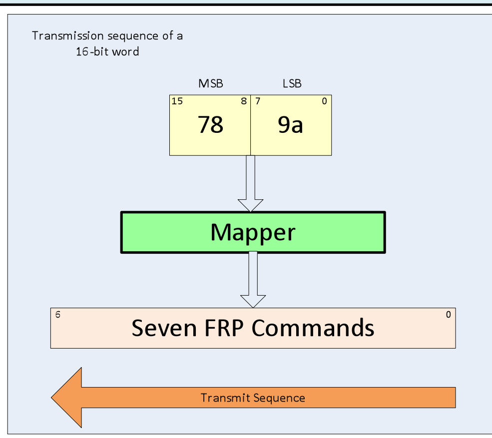
- Multiple port configurations are required to map Imaging Use Cases
- CSI-2 v1.3 provides Logical Port realizations with embedded clock & data

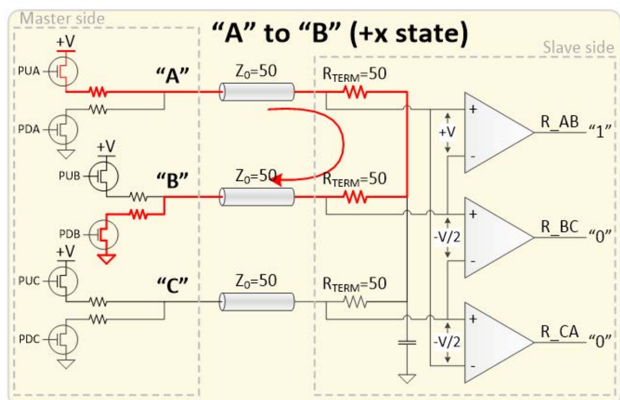


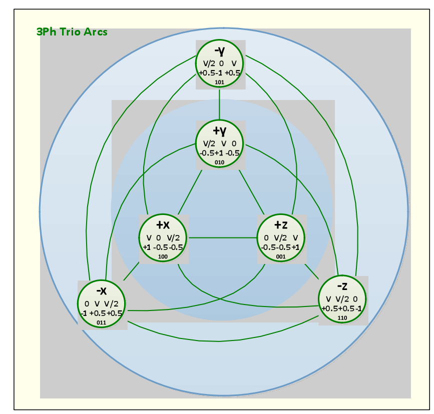
mipi alliance

CSI-2 over C-PHY (N-Phase) Data Path



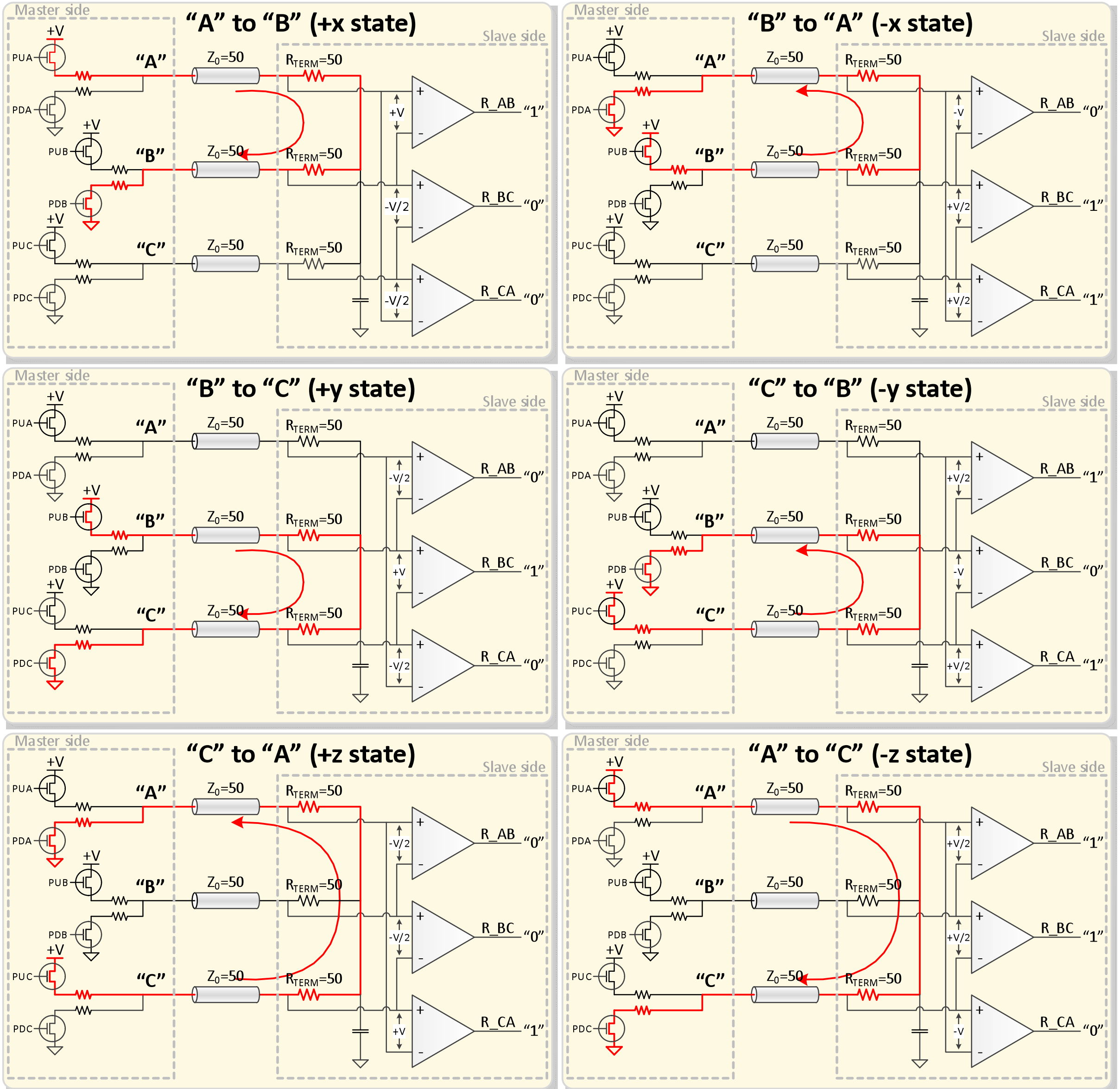






mipi alliance

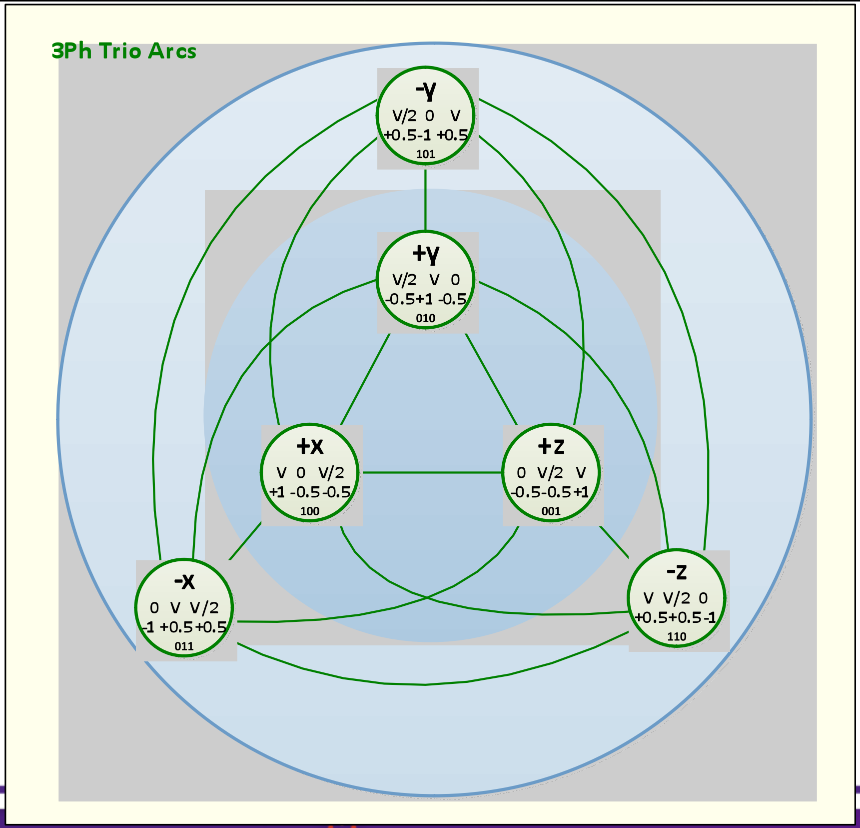
N-Phase (CSI-2 over C-PHY): 6 states using 3 wires



mipi alliance

N-Phase: 5 Transition arcs

Trio State	Wire Amplitude			Receiver diff input voltage			Receiver digital output		
	A	B	C	A - B	B - C	C - A	Rx_AB	Rx_BC	Rx_CA
+x	+V	0	+V/2	+V	-V/2	-V/2	1	0	0
-x	0	+V	+V/2	-V	+V/2	+V/2	0	1	1
+y	+V/2	+V	0	-V/2	+V	-V/2	0	1	0
-y	+V/2	0	+V	+V/2	-V	+V/2	1	0	1
+z	0	+V/2	+V	-V/2	-V/2	+V	0	0	1
-z	+V	+V/2	0	+V/2	+V/2	-V	1	1	0



mipi alliance

N-Phase: 16-bit to 7 FRP command mapping

[data15, data14, data13, data12, data11, data10, data9, data8, data7, data6, data5, data4, data3, data2, data1, data0]

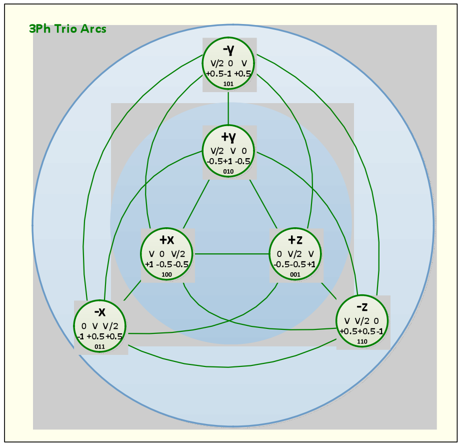
<u>Composition of 16-bit value, Tx_Data[15:0] or Rx_Data[15:0]</u>

Size	Values	Address range	Flip	Composition
(1024)	6, 4	0xfc00 to 0xffff	Flip[6:0]==0x50==[1,0,1,0,0,0,0]	[1,1,1,1,1,1, ro5, po5, ro3, po3, ro2, po2, ro1, po1, ro0, po0]
(1024)	5, 4	0xf800 to 0xfbff	Flip[6:0]==0x30==[0,1,1,0,0,0,0]	[1,1,1,1,1,0, ro6, po6, ro3, po3, ro2, po2, ro1, po1, ro0, po0]
(1024)	6, 3	0xf400 to 0xf7ff	Flip[6:0]==0x48==[1,0,0,1,0,0,0]	[1,1,1,1,0,1, ro5, po5, ro4, po4, ro2, po2, ro1, po1, ro0, po0]
(1024)	5, 3	0xf000 to 0xf3ff	Flip[6:0]==0x28==[0,1,0,1,0,0,0]	[1,1,1,1,0,0, ro6, po6, ro4, po4, ro2, po2, ro1, po1, ro0, po0]
(1024)	4, 3	0xec00 to 0xefff	Flip[6:0]==0x18==[0,0,1,1,0,0,0]	[1,1,1,0,1,1, ro6, po6, ro5, po5, ro2, po2, ro1, po1, ro0, po0]
(1024)	6, 2	0xe800 to 0xebff	Flip[6:0]==0x44==[1,0,0,0,1,0,0]	[1,1,1,0,1,0, ro5, po5, ro4, po4, ro3, po3, ro1, po1, ro0, po0]
(1024)	5, 2	0xe400 to 0xe7ff	Flip[6:0]==0x24==[0,1,0,0,1,0,0]	[1,1,1,0,0,1, ro6, po6, ro4, po4, ro3, po3, ro1, po1, ro0, po0]
(1024)	4, 2	0xe000 to 0xe3ff	Flip[6:0]==0x14==[0,0,1,0,1,0,0]	[1,1,1,0,0,0, ro6, po6, ro5, po5, ro3, po3, ro1, po1, ro0, po0]
(1024)	3, 2	0xdc00 to 0xdfff	Flip[6:0]==0x0c==[0,0,0,1,1,0,0]	[1,1,0,1,1,1, ro6, po6, ro5, po5, ro4, po4, ro1, po1, ro0, po0]
(1024)	6, 1	0xd800 to 0xdbff	Flip[6:0]==0x42==[1,0,0,0,0,1,0]	[1,1,0,1,1,0, ro5, po5, ro4, po4, ro3, po3, ro2, po2, ro0, po0]
(1024)	5, 1	0xd400 to 0xd7ff	Flip[6:0]==0x22==[0,1,0,0,0,1,0]	[1,1,0,1,0,1, ro6, po6, ro4, po4, ro3, po3, ro2, po2, ro0, po0]
(1024)	4, 1	0xd000 to 0xd3ff	Flip[6:0]==0x12==[0,0,1,0,0,1,0]	[1,1,0,1,0,0, ro6, po6, ro5, po5, ro3, po3, ro2, po2, ro0, po0]
(1024)	3, 1	0xcc00 to 0xcfff	Flip[6:0]==0x0a==[0,0,0,1,0,1,0]	[1,1,0,0,1,1, ro6, po6, ro5, po5, ro4, po4, ro2, po2, ro0, po0]
(1024)	2, 1	0xc800 to 0xcbff	Flip[6:0]==0x06==[0,0,0,0,1,1,0]	[1,1,0,0,1,0, ro6, po6, ro5, po5, ro4, po4, ro3, po3, ro0, po0]
(1024)	6, 0	0xc400 to 0xc7ff	Flip[6:0]==0x41==[1,0,0,0,0,0,1]	[1,1,0,0,0,1, ro5, po5, ro4, po4, ro3, po3, ro2, po2, ro1, po1]
(1024)	5, 0	0xc000 to 0xc3ff	Flip[6:0]==0x21==[0,1,0,0,0,0,1]	[1,1,0,0,0,0, ro6, po6, ro4, po4, ro3, po3, ro2, po2, ro1, po1]
(1024)	4, 0	0xbc00 to 0xbfff	Flip[6:0]==0x11==[0,0,1,0,0,0,1]	[1,0,1,1,1,1, ro6, po6, ro5, po5, ro3, po3, ro2, po2, ro1, po1]
(1024)	3, 0	0xb800 to 0xbbff	Flip[6:0]==0x09==[0,0,0,1,0,0,1]	[1,0,1,1,1,0, ro6, po6, ro5, po5, ro4, po4, ro2, po2, ro1, po1]
(1024)	2, 0	0xb400 to 0xb7ff	Flip[6:0]==0x05==[0,0,0,0,1,0,1]	[1,0,1,1,0,1, ro6, po6, ro5, po5, ro4, po4, ro3, po3, ro1, po1]
(1024)	1, 0	0xb000 to 0xb3ff	Flip[6:0]==0x03==[0,0,0,0,0,1,1]	[1,0,1,1,0,0, ro6, po6, ro5, po5, ro4, po4, ro3, po3, ro2, po2]

Size	Value	Address range	Flip	Composition
(4096)	6	0xafff – 0xa000	Flip[6:0]==0x40==[1,0,0,0,0,0,0]	[1,0,1,0, ro5, po5, ro4, po4, ro3, po3, ro2, po2, ro1, po1, ro0, po0]
(4096)	5	0x9fff – 0x9000	Flip[6:0]==0x20==[0,1,0,0,0,0,0]	[1,0,0,1, ro6, po6, ro4, po4, ro3, po3, ro2, po2, ro1, po1, ro0, po0]
(4096)	4	0x8fff – 0x8000	Flip[6:0]==0x10==[0,0,1,0,0,0,0]	[1,0,0,0, ro6, po6, ro5, po5, ro3, po3, ro2, po2, ro1, po1, ro0, po0]
(4096)	3	0x7fff – 0x7000	Flip[6:0]==0x08==[0,0,0,1,0,0,0]	[0,1,1,1, ro6, po6, ro5, po5, ro4, po4, ro2, po2, ro1, po1, ro0, po0]
(4096)	2	0x6fff – 0x6000	Flip[6:0]==0x04==[0,0,0,0,1,0,0]	[0,1,1,0, ro6, po6, ro5, po5, ro4, po4, ro3, po3, ro1, po1, ro0, po0]
(4096)	1	0x5fff – 0x5000	Flip[6:0]==0x02==[0,0,0,0,0,1,0]	[0,1,0,1, ro6, po6, ro5, po5, ro4, po4, ro3, po3, ro2, po2, ro0, po0]
(4096)	0	0x4fff – 0x4000	Flip[6:0]==0x01==[0,0,0,0,0,0,1]	[0,1,0,0, ro6, po6, ro5, po5, ro4, po4, ro3, po3, ro2, po2, ro1, po1]
(16384)	(0 – 6 are all zero)	0x3fff – 0x0000	Flip[6:0]==0x00==[0,0,0,0,0,0,0]	[0,0, ro6, po6, ro5, po5, ro4, po4, ro3, po3, ro2, po2, ro1, po1, ro0, po0]

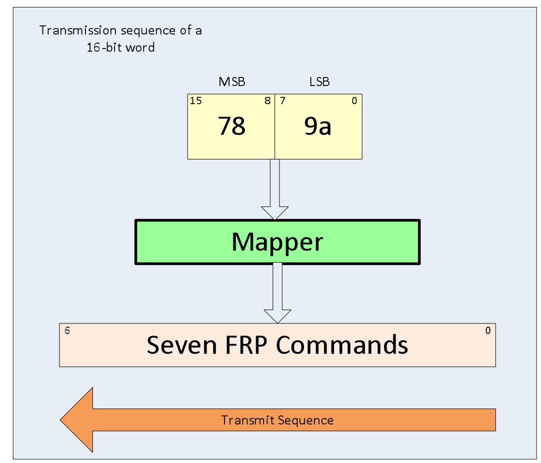
<u>Legend for abbreviated bit values above:</u>

ro0 ⇒ Rotate[0]	po0 ⇒ Polarity[0]
ro1 ⇒ Rotate[1]	po1 ⇒ Polarity[1]
ro2 ⇒ Rotate[2]	po2 ⇒ Polarity[2]
ro3 ⇒ Rotate[3]	po3 ⇒ Polarity[3]
ro4 ⇒ Rotate[4]	po4 ⇒ Polarity[4]
ro5 ⇒ Rotate[5]	po5 ⇒ Polarity[5]
ro6 ⇒ Rotate[6]	po6 ⇒ Polarity[6]



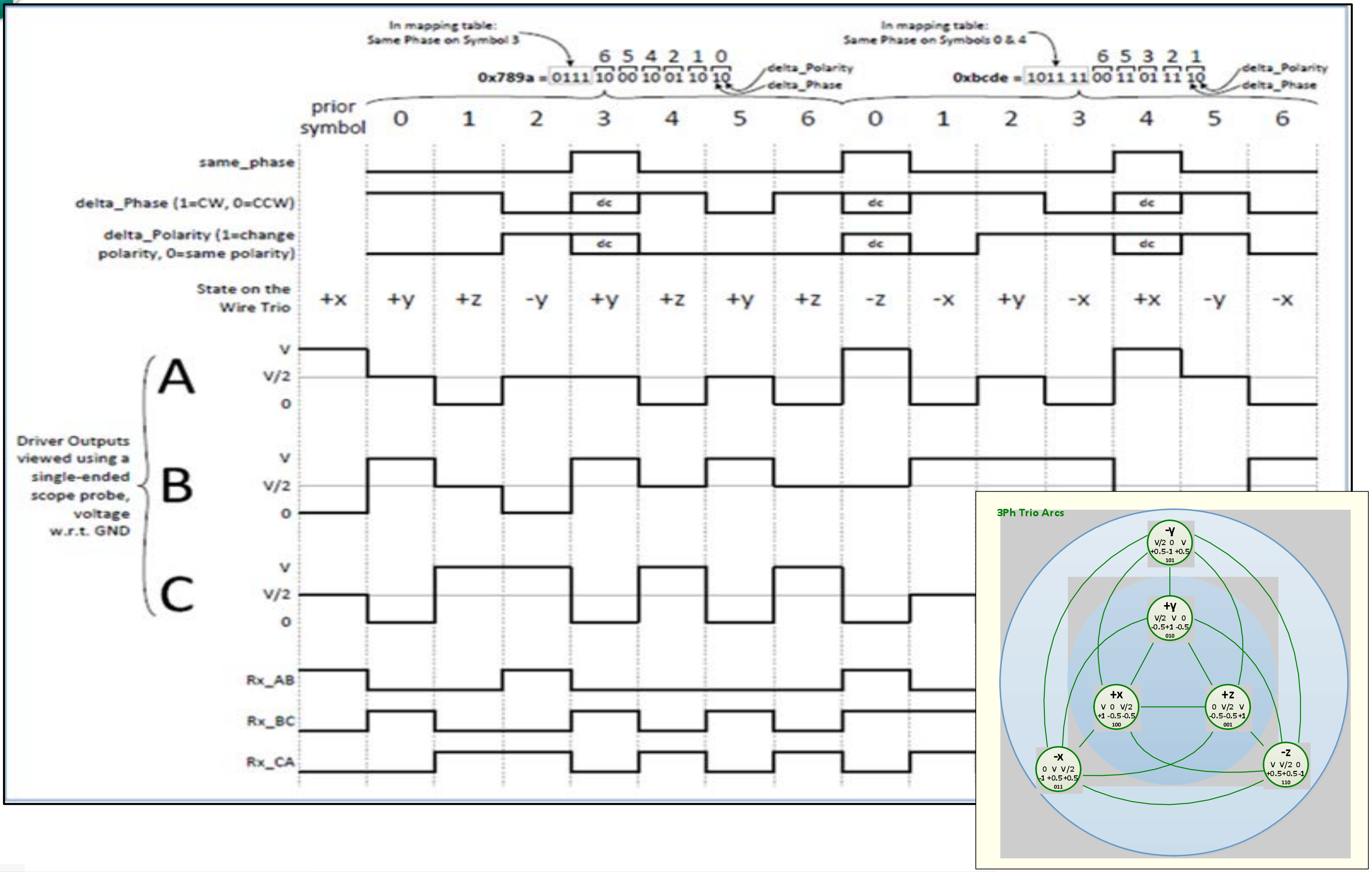
N-Phase: Example of CSI-2 pixel data to C-PHY signaling 1/2

16-bit Pix Data		Mapping to symbols over 7 UI					Encoding to Wire State			
hex	decimal	Region	Tx Sym	F	R	P	State	A	B	C
							+x	*V*	*0*	*V/2*
789a	30874	3; 4K	2	0	1	0	+y	V/2	V	0
			2	0	1	0	+z	0	V/2	V
			1	0	0	1	-y	V/2	0	V
			4	1	0	0	+y	V/2	V	0
			2	0	1	0	+z	0	V/2	V
			0	0	0	0	+y	V/2	V	0
			2	0	1	0	+z	0	V/2	V
bcde	48350	4,0; 1K	4	1	0	0	-z	V	V/2	0
			2	0	1	0	-x	0	V	V/2
			3	0	1	1	+y	V/2	V	0
			1	0	0	1	-x	0	V	V/2
			4	1	0	0	+x	V	0	V/2
			3	0	1	1	-y	V/2	0	V
			0	0	0	0	-x	0	V	V/2



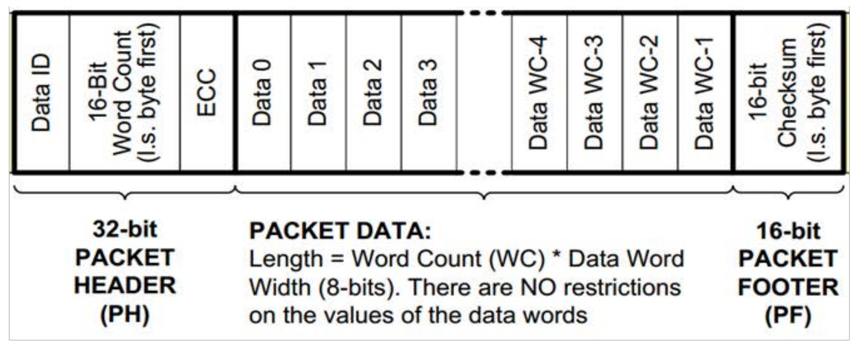
mipi alliance

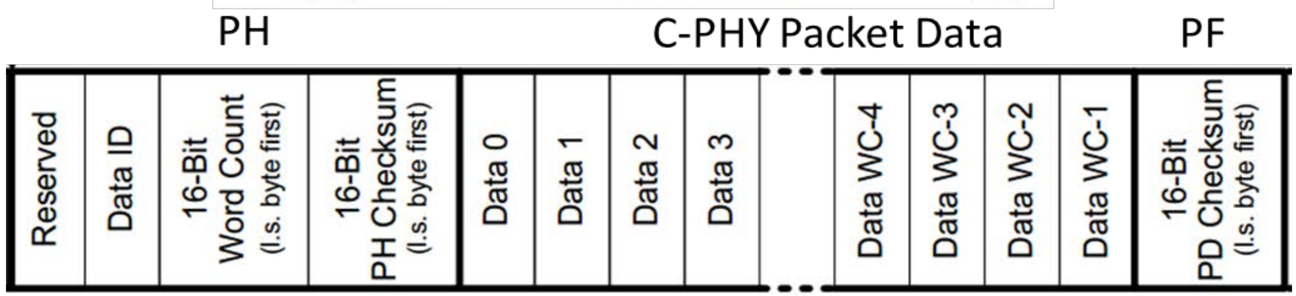
N-Phase: Example of CSI-2 pixel data to C-PHY signaling 2/2

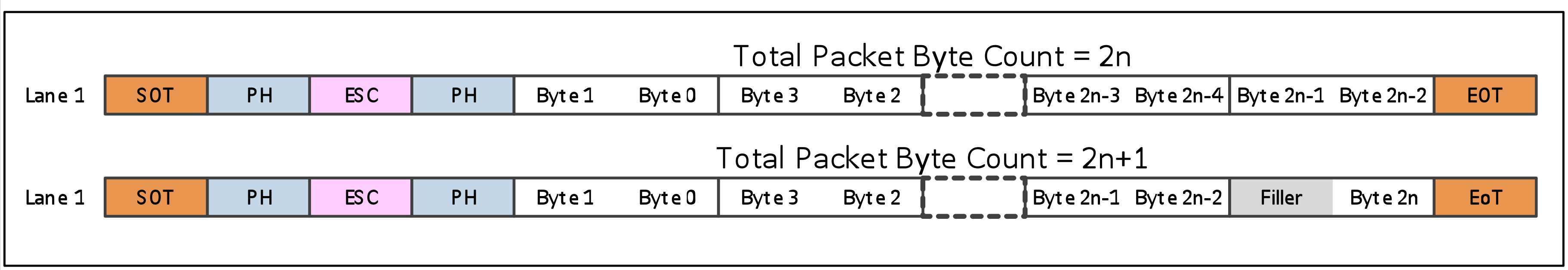


mipi alliance

N-Phase Mission Critical Transfers 1/2







mipi alliance

N-Phase mission critical transfers 2/2

Link Error Example (a): Loss of No Symbol Clocks

Symbol Interval — TX: Transmit ESCAPE [s0:s6] — RX: Detect ESCAPE [s1:s6] — 7 Received Symbols

								s0	s1	s2	s3	s4	s5	s6			
Transmitted Symbols	2	1	3	2	1	3	0	3	4	4	4	4	4	3	2	4	3
Transmitted Wire States	+z	+x	-z	+x	+y	-x	+y	+x	-y	+y	-y	+y	-y	+y	-z	-x	+x	-y
Received Wire States	+z	+x	-z	+x	+y	-x	+y	+z	-y	+y	-y	+y	-y	+y	-z	-x	+x	-y
Received Symbols	2	1	3	2	1	3	2	1	4	4	4	4	4	3	2	4	3

Link Error Example (b): Loss of One Symbol Clock

Symbol Interval — TX: Transmit ESCAPE [s0:s6] — RX: Detect ESCAPE [s1:s6] — 7 Received Symbols

								s0	s1	s2	s3	s4	s5	s6			
Transmitted Symbols	1	3	0	3	4	1	4	3	4	4	4	4	4	3	0	3	1
Transmitted Wire States	+z	-y	+z	+y	-z	+z	-y	+y	-z	+z	-z	+z	-z	+z	-x	-z	+x	-z
Received Wire States	+z	-y	+z	+y	-z	+z	-y	-y	-z	+z	-z	+z	-z	+z	-x	+x	-y	-x
Received Symbols	1	3	0	3	4	1	1	2	4	4	4	4	4	3	0	3	1

Link Error Example (c): Loss of Two Symbol Clocks

Symbol Interval — TX: Transmit ESCAPE [s0:s6] — RX: Detect ESCAPE [s1:s6] — 7 Received Symbols

								s0	s1	s2	s3	s4	s5	s6			
Transmitted Symbols	4	3	1	2	0	1	1	3	4	4	4	4	4	3	0	2	4
Transmitted Wire States	+z	-z	+x	-z	-x	-z	+y	-x	+y	-y	+y	-y	+y	-y	+z	+y	+z	-z
Received Wire States	+z	-z	+x	-z	-x	-z	+y	+y	+y	-y	+y	-y	+y	-y	+z	+y	+z	-z
Received Symbols	4	3	1	2	0	1	1	1	4	4	4	4	4	3	0	2	4

Notes:

- Symbols are transmitted serially from left to right
- Wire state and symbol errors are highlighted in yellow
- ▲ : point at which symbol clock is lost
- ▲ : point at which symbol clock is restored
- ◆ : point of incorrect word alignment
- ◆ : point at which correct word alignment is restored

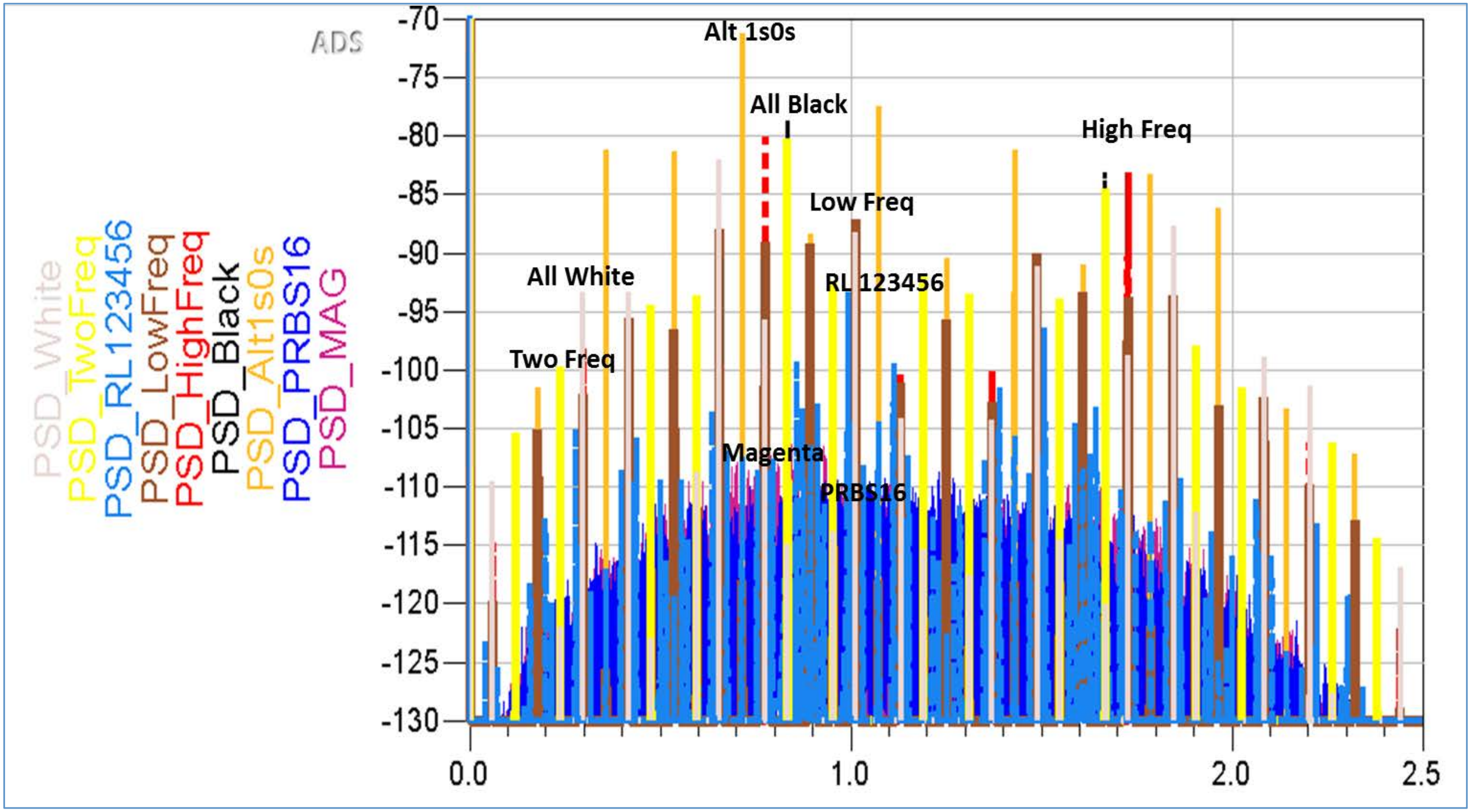
mipi alliance

Evolution of CSI-2 Imaging Interface

Imaging Interface	Description Interface Performance	Release / Adoption
Gen 1	**CSI-2 v1.1** protocol over D-PHY v1.1 (at 1.5 Gbps), and bidirectional command over I2C_FM (at 400 Kbps) Provides effective (usable) BW of 3 Gbps over 6 D-PHY v1.1 pins	EOY 2012
Gen 2	**CSI-2 v1.2** protocol over D-PHY v1.2 (at 2.5 Gbps), and bidirectional command over I2C_FM (at 400 Kbps) **CSI-2 v1.3** protocol over C-PHY v1.0 (2.5 Gsps or 5.7 Gbps) and D-PHY v1.2 (at 2.5 Gbps), and bidirectional command over I2C_FM (at 400 Kbps) Provides effective (usable) BW of 5 Gbps over 6 D-PHY v1.2 pins Provides effective (usable) BW of 11.43 Gbps over 6 C-PHY v1.0 pins	EOY 2014
Gen 3	**CSI-2 v2.0** protocol supports C-PHY v1.2 and D-PHY v2.1, with bidirectional command over I2C_FMP (1GHz) and I3C v1.0. **C-PHY v1.2** provides up to **4.5 Gsps (10.3 Gbps) over 3 pins** **D-PHY v2.1** provides up to **4.5 Gbps over 4 pins** Bidirectional CCI over I2C_FMP provides around 880 Kbps of effective BW, and CCI over **I3C v1.0** provides effective BW of: 10.67 Mbps over SDR, 19.2 Mbps over HDR-DDR, 18 Mbps over HDR-TSL, and 29.3 Mbps over HDR-TSP. Provides effective (usable) BW of 9 Gbps over 6 D-PHY v2.1 pins Provides effective (usable) BW of 20.6 Gbps over 6 C-PHY v1.2 pins	EOY 2016

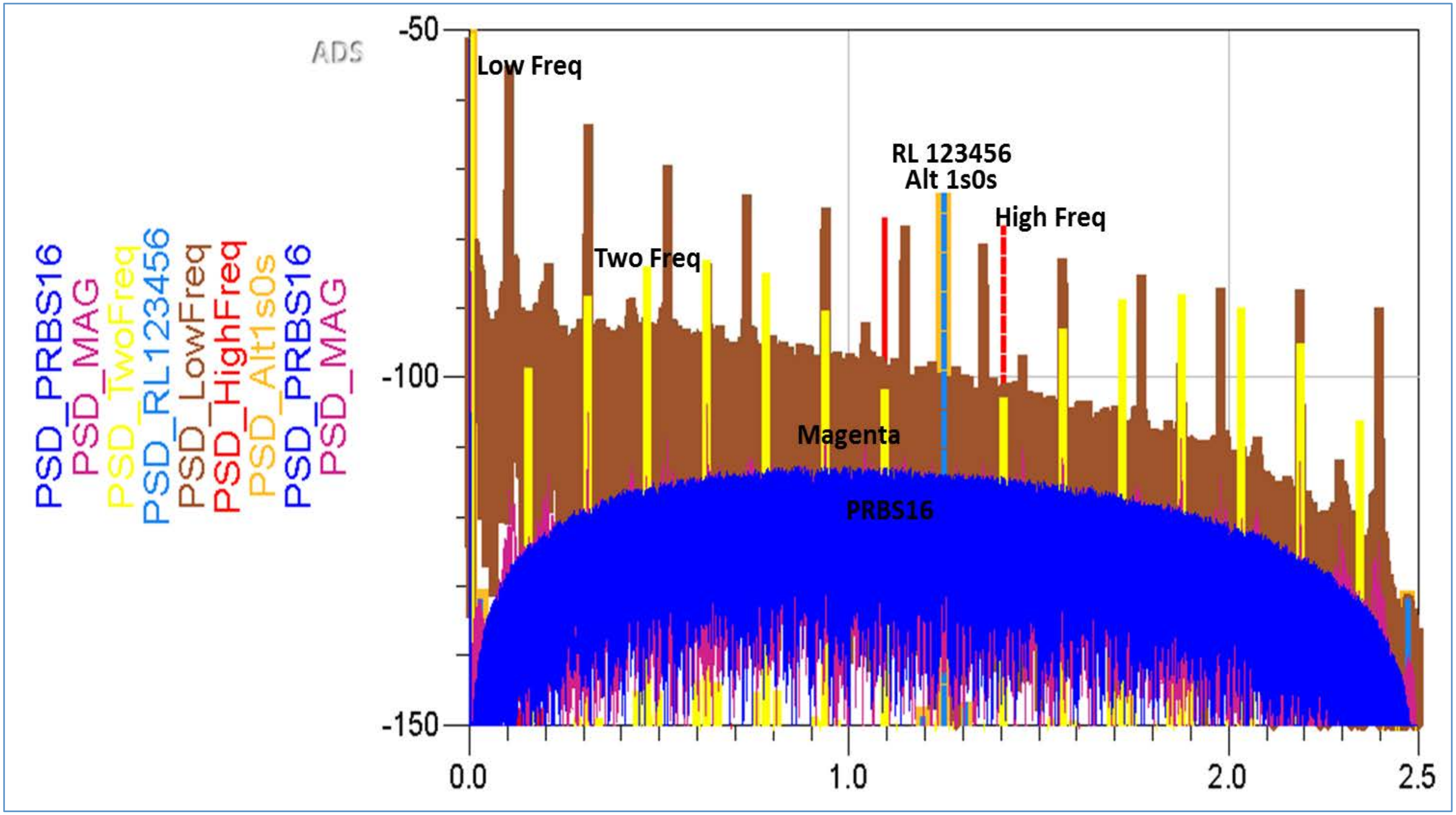
mipi alliance

CSI-2 over C-PHY PSD emission reduction from scrambling

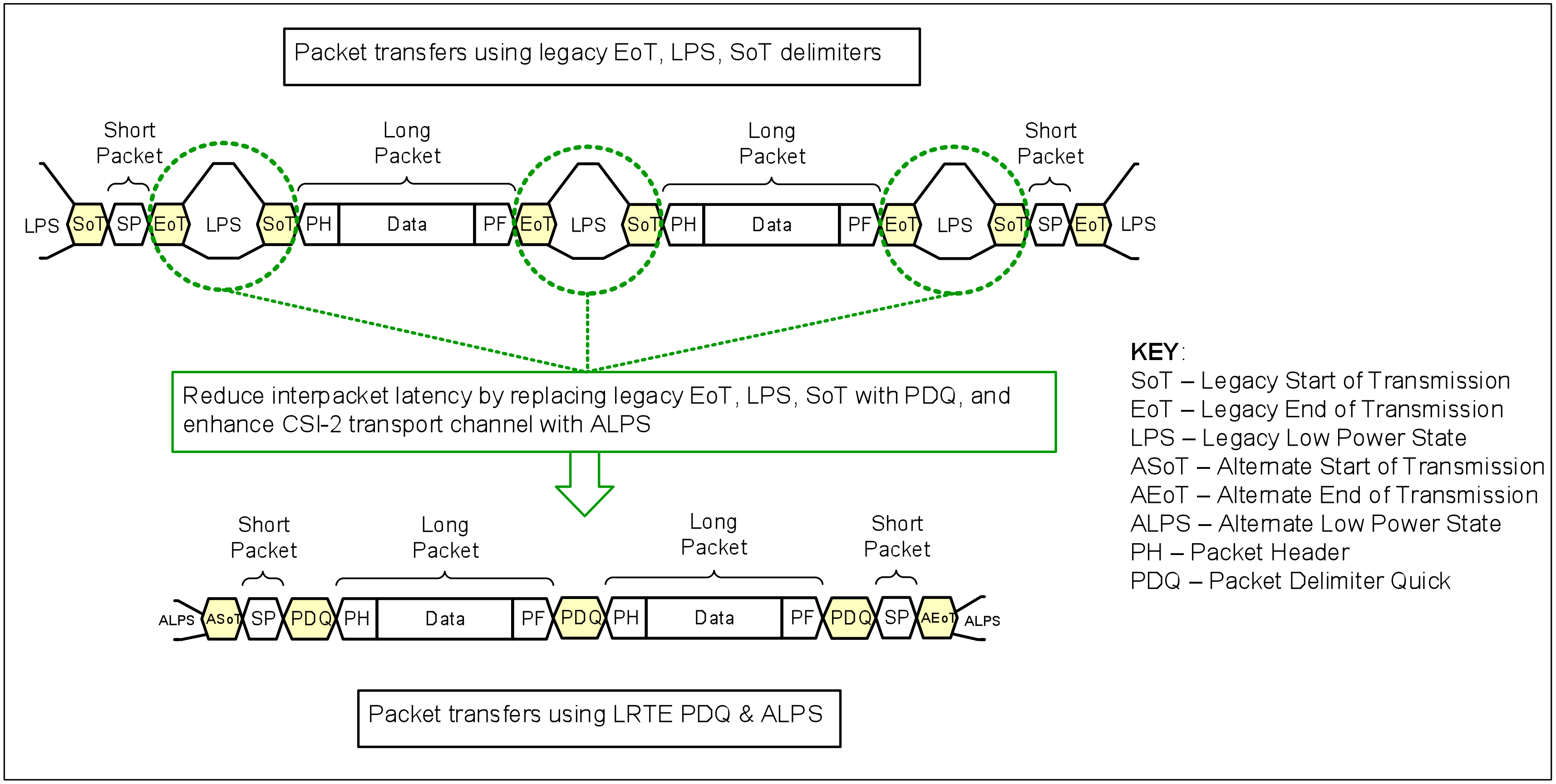


mipi alliance

CSI-2 over D-PHY PSD emission reduction from scrambling



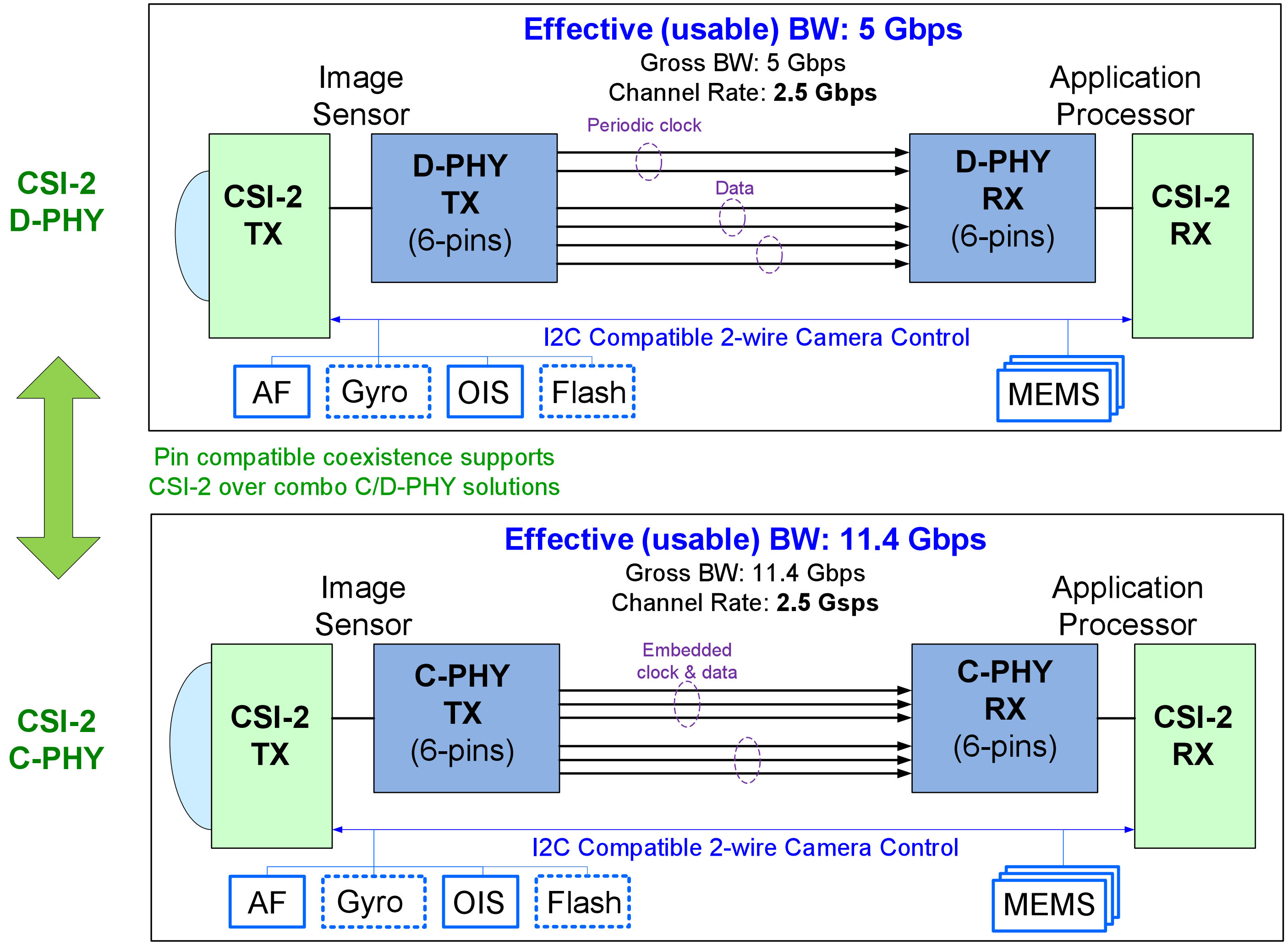
CSI-2 Latency Reduction Transport Efficiency



- Reduce latency and improve efficiency (preserving PHY based delimiters / B2B)
- Provides longer reach over C/D-PHYs without need for redrivers or retimers
- Alleviates electrical overstress current leakages impediments

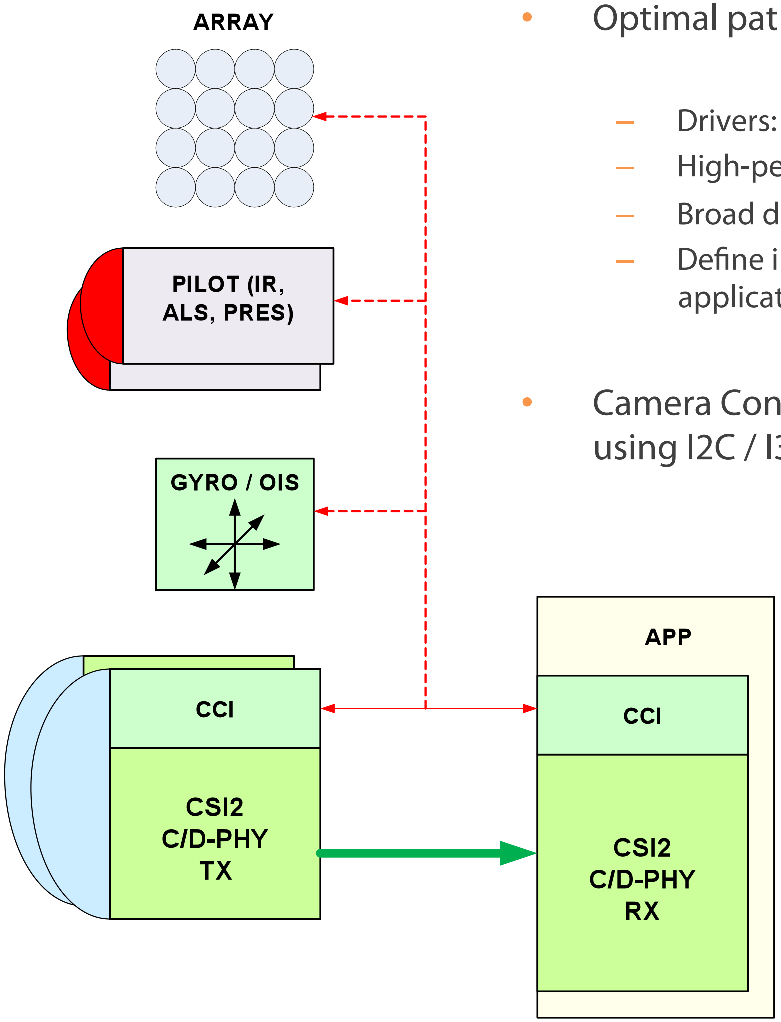
mipi alliance

CSI-2 Sensor Fusion using CCI



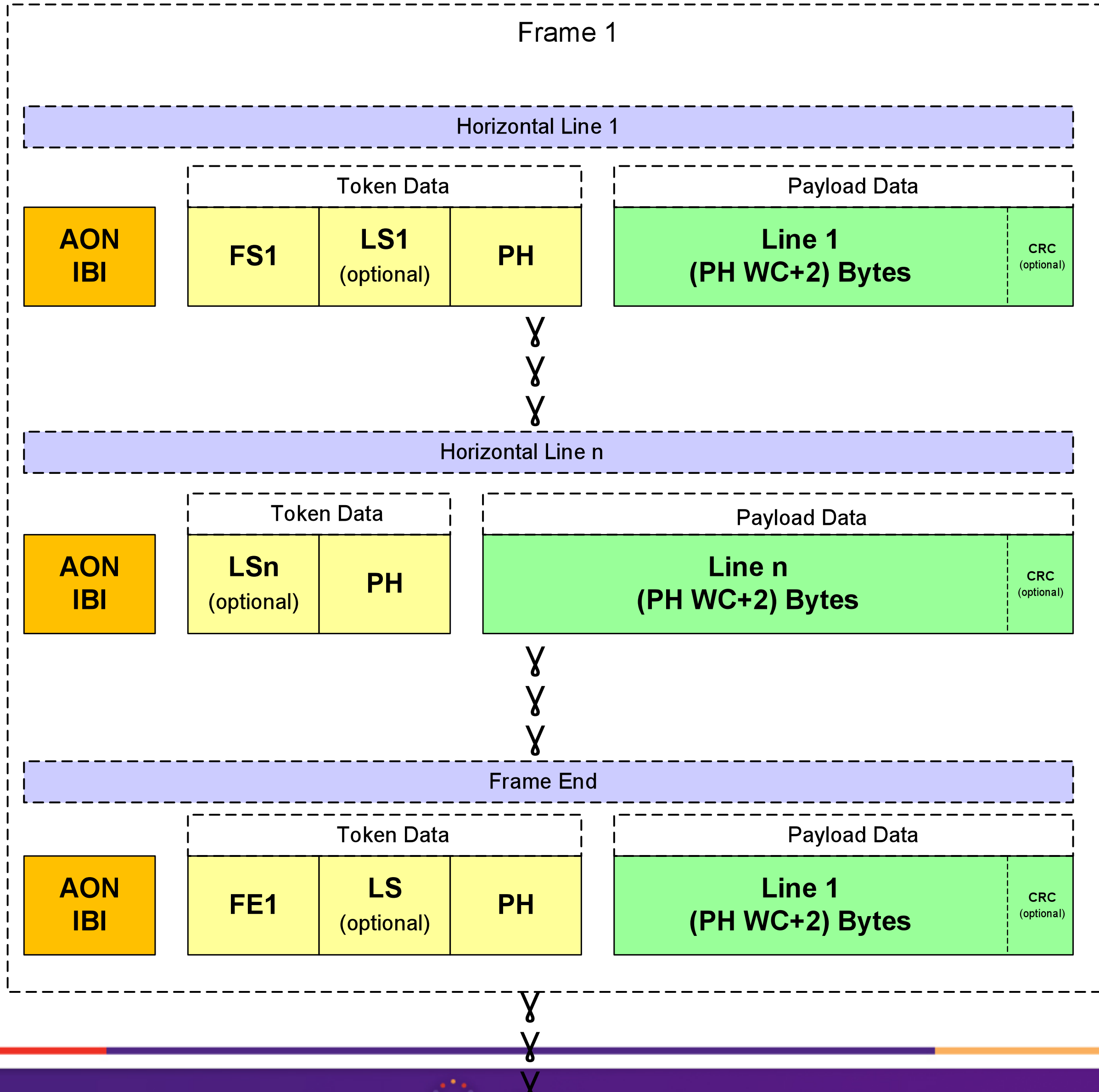
mipi alliance

CSI-2 CCI and AON Advancements 1/2



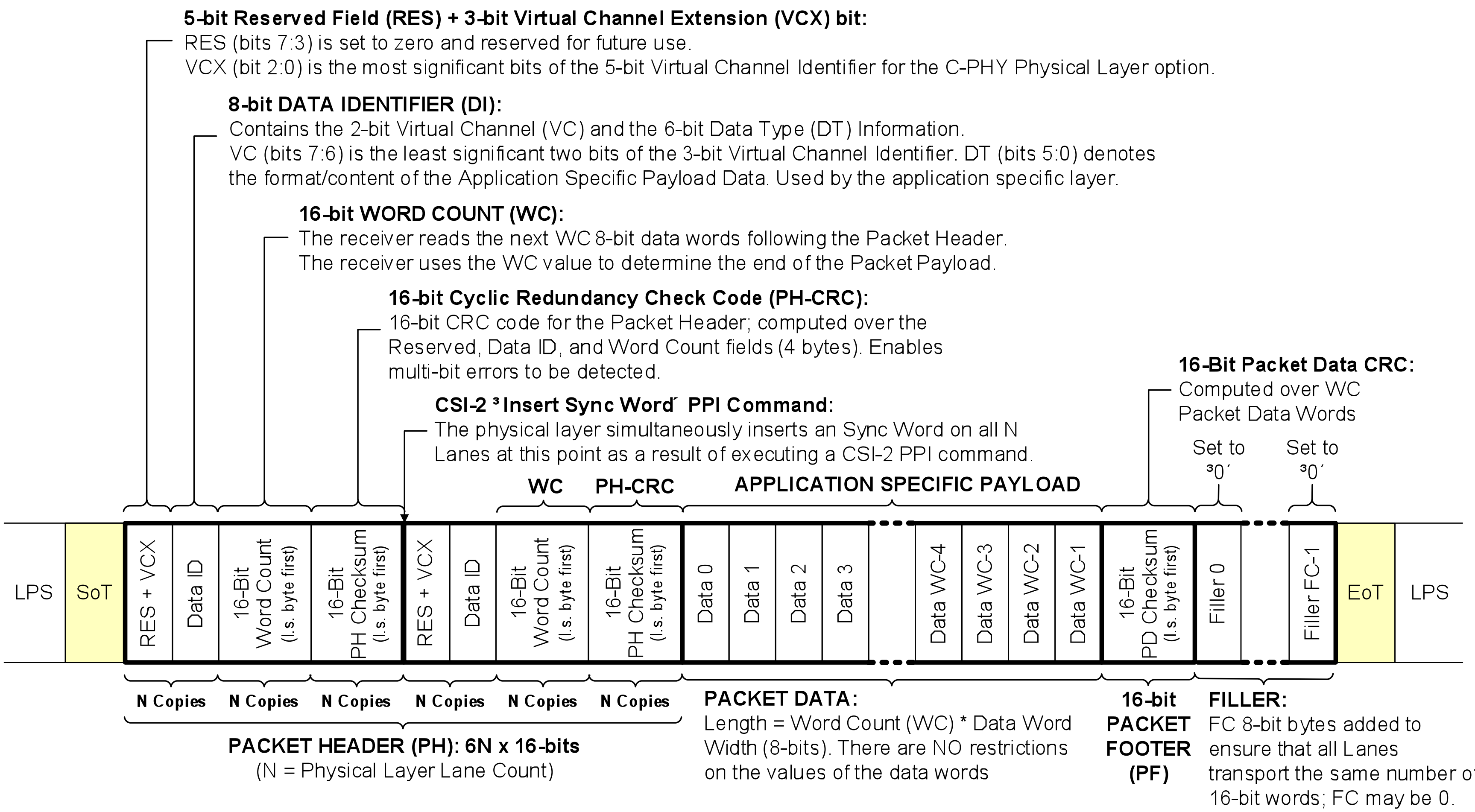
- Optimal pathway for multiple forward-looking advancements in imaging
  - Drivers: Health, Convenience, Security, Lifestyle, Efficiency
  - High-perf pixel conduit needs met with C/D-PHY advancements
  - Broad definitions and fuzzy range: (i.e. Wearable: Near Body, On Body, In Body)
  - Define imaging requirements for CCI, emerging AOI, array, and non-symmetrical applications
- Camera Controller Interface (CCI) and AON advancement considerations using I2C / I3C (SDR DDR, TSL, TSP)
  - Point-to-Point and Multi-Drop configurations

CSI-2 CCI and AON Advancements 2/2



mipi alliance

CSI-2 over C-PHY Virtual Channel Extension



mipi alliance

CSI-2 over D-PHY Virtual Channel Extension

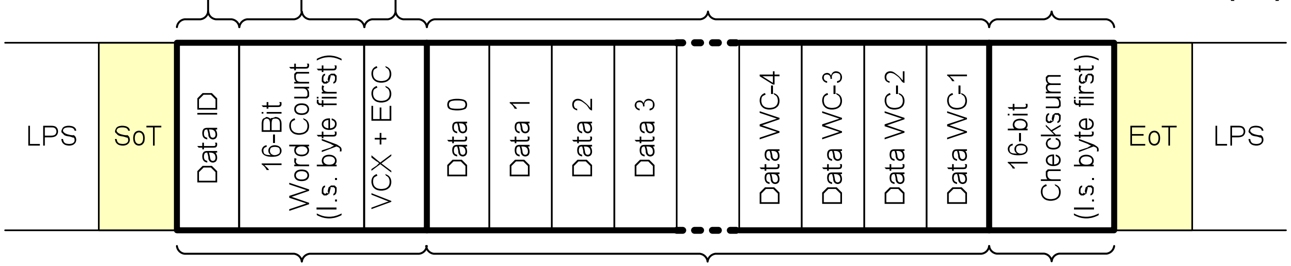
8-bit DATA IDENTIFIER (DI):
Contains the 2-bit Virtual Channel (VC) and the 6-bit Data Type (DT) Information.
VC (bits 7:6) is the least significant two bits of the 3-bit Virtual Channel Identifier. DT (bits 5:0) denotes the format/content of the Application Specific Payload Data. Used by the application specific layer.

16-bit WORD COUNT (WC):
The receiver reads the next WC data words independent of their values. The receiver is NOT looking for any embedded sync sequences within the payload data. The receiver uses the WC value to determine the end of the Packet Payload.

6-bit Error Correction Code (ECC) + 2 Virtual Channel Extension (VCX) bits
ECC (bits 5:0) enables 1-bit errors within the packet header to be corrected and 2-bit errors to be detected. VCX (bits 7:6) are the most significant bit of the 4-bit Virtual Channel Identifier for the D-PHY physical layer option.

APPLICATION SPECIFIC PAYLOAD

CHECKSUM/CRC (CS)



32-bit PACKET HEADER (PH)

PACKET DATA:
Length = Word Count (WC) * Data Word Width (8-bits). There are NO restrictions on the values of the data words

16-bit PACKET FOOTER (PF)

mipi alliance

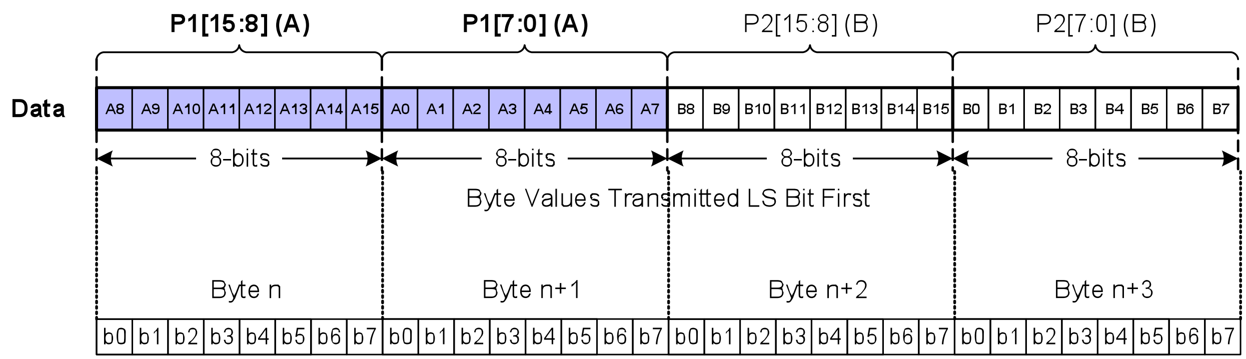
CSI-2 DPCM & HDR Advancements

- DPCM 12-10-12
  - SNR & IQ Benefits over varying degrees of noise, edges, MTF
  - Superior to straight RAW-10 capture or existing DPCM 12-8-12

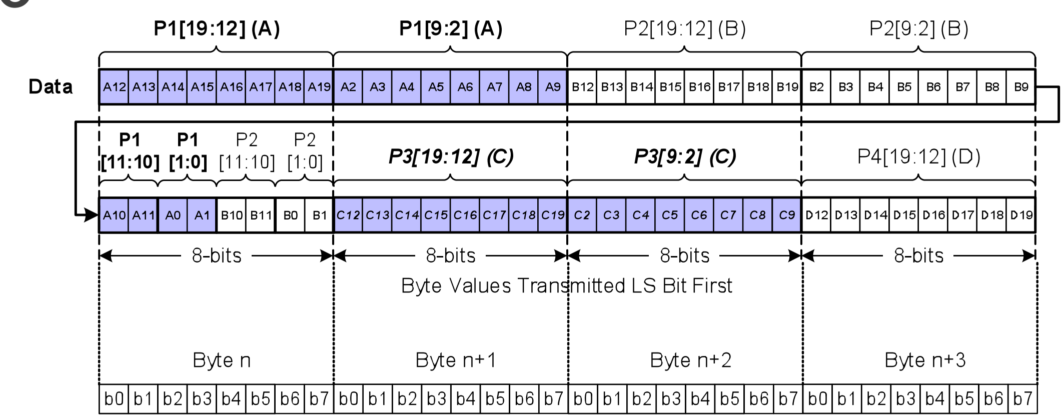
mipi alliance

CSI-2 HDR Advancements

- HDR-16



- HDR-20



mipi alliance

Questions?

mipi alliance

Backup

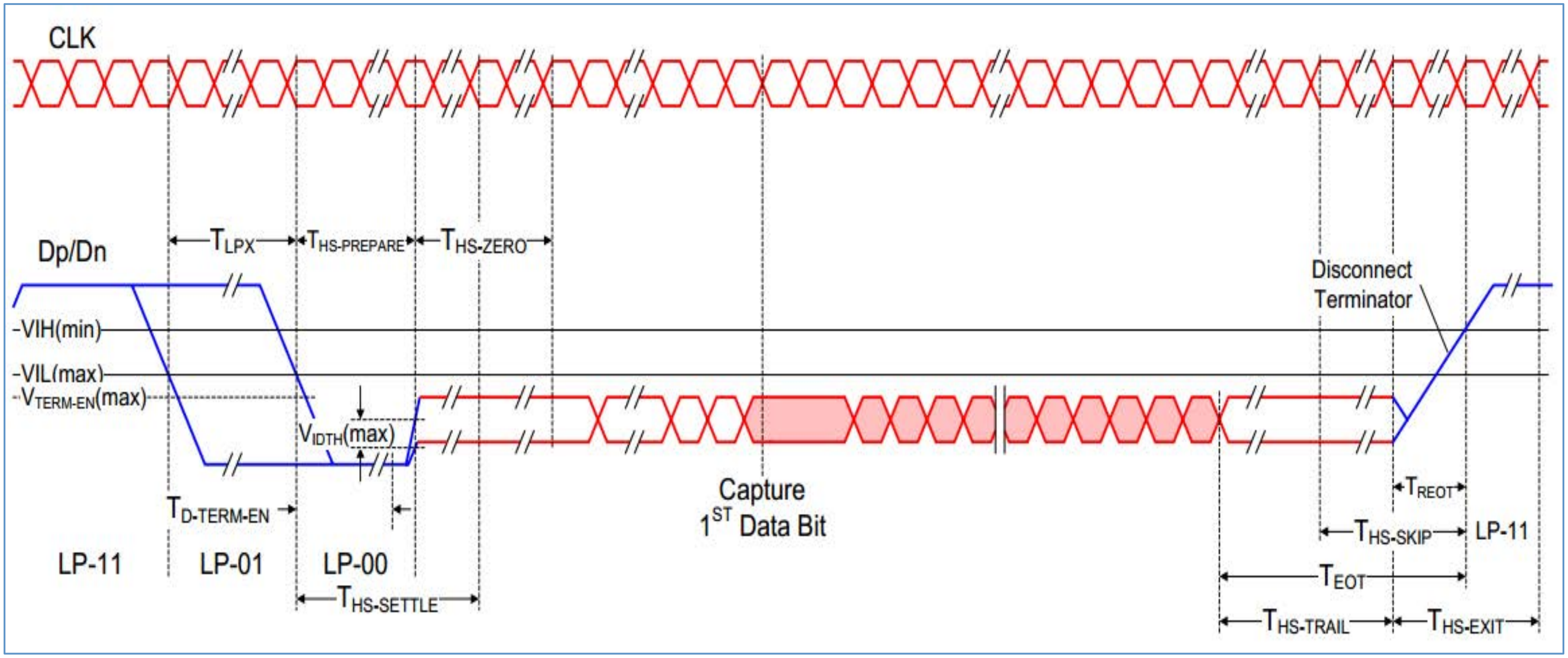
MIPI C/D/M PHYs

PHY Characteristics

Characteristic	*M-PHY v3.1*	*D-PHY v1.2*	*C-PHY v1.0*
Primary use case	Performance driven, bidirectional packet/ network oriented interface	Efficient unidirectional streaming interface, with low speed in-band reverse channel	Efficient unidirectional streaming interface, with low speed in-band reverse channel
HS clocking method	Embedded Clock	DDR Source-Sync Clock	Embedded Clock
Channel compensation	Equalization	Data skew control relative to clock	Encoding to reduce data toggle rate
Minimum configuration and pins	1 lane per direction, dual-simplex, 2 pins each (4 total)	1 lane plus clock, simplex, 4 pins	1 lane (trio), simplex, 3 pins
Maximum transmitter swing amplitude	SA: 250mV (peak) LA: 500mV (peak)	LP: 1300mV (peak) HS: 360mV (peak)	LP: 1300mV (peak) HS: 425mV (peak)
Data rate per lane (HS)	HS-G1: 1.25, 1.45 Gb/s HS-G2: 2.5, 2.9 Gb/s HS-G3: 5.0, 5.8 Gb/s (Line rates are 8b10b encoded)	80 Mbps to ~2.5 Gbps (aggregate)	80 Msym/s to 2.5 Gsym/s times 2.28 bits/sym, or max 5.7 Gbps (aggregate)
Data rate per lane (LS)	10kbps – 600 Mbps	< 10 Mbps	< 10 Mbps
Bandwidth per Port (3 or 4 lanes)	~ 4.0 – 18.6 Gb/s (aggregate BW)	Max ~10 Gbps per 4-lane port (aggregate)	Max ~ 17.1 Gbps per 3-lane port (aggregate)
Typical pins per Port (3 or 4 lanes)	10 (4 lanes TX, 1 lane RX)	10 (4 lanes, 1 lane clock)	9 (3 lanes)

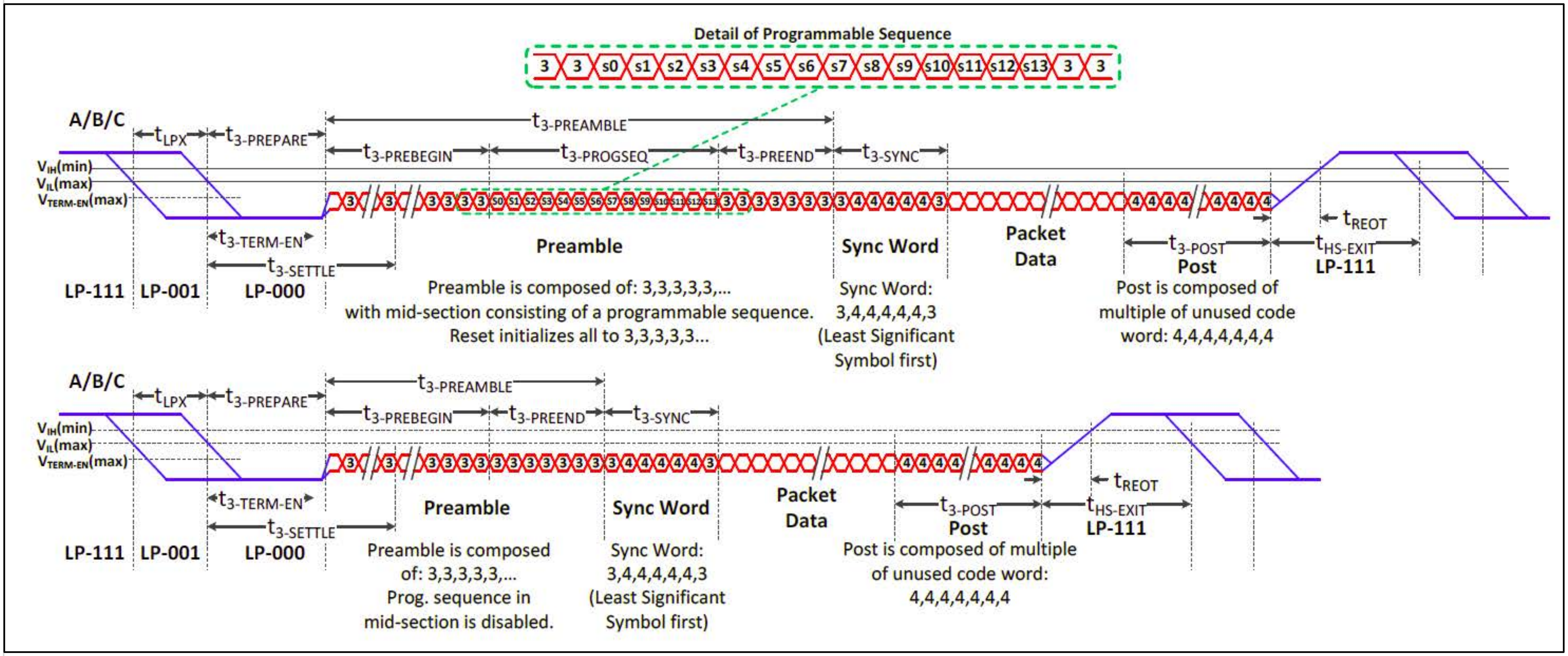
mipi alliance

CSI-2 over D-PHY signaling



mipi alliance

CSI-2 over C-PHY (N-Phase) signaling



mipi alliance