Imaging interface advancements and development to meet the needs of mobile and mobile-influenced industries

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Brief overview from Peter Lefkin
Managing Director, MIPI Alliance
About MIPI Alliance

We are a global, collaborative organization comprised of over 280 member companies spanning the mobile and mobile-influenced ecosystems.

MIPI Alliance is leading innovation in mobile interface technology.
MIPI Alliance Member Ecosystem
Partners
Active Technical Working Groups

- Camera
- Debug
- Display
- Low Latency Interface
- Low Speed Multipoint Link
- PHY (C/D/M)
- Reduced Input Output
- RF Front End
- Sensor / I3C℠
- Software
- Test
- UniPro℠
MIPI Alliance continues to evolve its Roadmap to meet the needs of the mobile and mobile-influenced industry with new and revised specifications.
Overview

Generational advancements and development of MIPI CSI imaging interface to meet the needs of Mobile and beyond applications including:

- Two equally capable MIPI imaging interface architectures
  - CSI-2 over C/D-PHYs
  - CSI-3 over UniPro and M-PHY
- Provision to mitigate PSD emissions
- Extended Virtual Channels
- High Dynamic Range enhancements
- Latency Reduction and Transport Efficiency
- Always On Metadata and Pixel Transfer
- Differential Pulse Code Modulation
Two equally capable imaging interface architectures

- **CSI-2** protocol contains transport and application layers, and natively supports: C-PHY, D-PHY, or combo C/D-PHY

- **CSI-3** application stack connects to **UniPro** transport layer, which in turn bolts onto M-PHY

<table>
<thead>
<tr>
<th>Applications</th>
<th>Imaging: CSI-2</th>
<th>Imaging: CSI-3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transport</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PHY</td>
<td>C-PHY</td>
<td>UniPro</td>
</tr>
<tr>
<td></td>
<td>D-PHY</td>
<td>M-PHY</td>
</tr>
</tbody>
</table>
CSI-2 D-PHY 1.2 extension Pix BW scales linearly
- 2.5 Gbps Channel delivers 10 Gbps over 4 data lanes and a clock lane (10 D-PHY pins).

CSI-2 C-PHY 1.0 extension Pix BW benefit from $\log_2{5}$ mapping gain
- 2.5 Gbps Channel delivers 17.1 Gbps over 3 lanes (9 C-PHY pins), or 22.7 Gbps over 4 lanes (12 C-PHY pins).

CSI-3 application stack connects to UniPro and M-PHY
- supports networking features using fixed gear channel rates of up to 5.8 Gbps.
- Rev control may run lower rate if asymmetric gears are supported by Image Sensor and Application Processor.
## Solutions for popular imaging use case

### 4K @ 30 fps and 12 BPP using CSI-2

<table>
<thead>
<tr>
<th>Required MIPI Specs (IPs)</th>
<th>Required PHY pins</th>
<th>Required Lane Rate</th>
<th>Required BW</th>
<th>Variable Link Rate</th>
<th>Control Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>[CSI-2] [D-PHY]</td>
<td>6</td>
<td>1.78 Gbps</td>
<td>3.56 Gbps</td>
<td>Yes</td>
<td>I2C</td>
</tr>
<tr>
<td>[CSI-2] [C-PHY]</td>
<td>3</td>
<td>1.55 Gbps</td>
<td>3.56 Gbps</td>
<td>Yes</td>
<td>I2C</td>
</tr>
</tbody>
</table>

### 4K @ 30 fps and 12 BPP using CSI-3

<table>
<thead>
<tr>
<th>Required MIPI Specs (IPs)</th>
<th>Required PHY pins</th>
<th>Required Lane Rate</th>
<th>Required BW</th>
<th>Variable Link Rate</th>
<th>Control Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>[CSI-3] [UniPro] [M-PHY]</td>
<td>4</td>
<td>5.0 Gbps</td>
<td>3.56 Gbps</td>
<td>No</td>
<td>In-band</td>
</tr>
</tbody>
</table>
CSI-2 v1.3 over C/D-PHY Evolution & Performance

Evolution of CSI-2 Performance Capabilities
Image Sensor @ 60 fps

- Achieves 34 Gbps using 18 wires; and beyond with scaling
- Optimal Pixel-Rate matched to Link Rate with C/D-PHY conduits

- 8 bpp
- 10 bpp
- 12 bpp

- Gen1
  - CSI-2 v1.1
    - DPHY v1.1 @ 1.5 GHz (6 Gbps over 10 wires)
- Gen2
  - CSI-2 v1.2
    - DPHY v1.2 @ 2.5 GHz (10 Gbps over 10 wires)
  - CPHY v1.0 @ 2.5 Gzh
    - (17 Gbps over 9 wires)

- (22.7 Gbps over 12 wires)

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CSI-2 Benefits of Embedded Clock & Data

- Multiple port configurations are required to map Imaging Use Cases
- CSI-2 v1.3 provides Logical Port realizations with embedded clock & data
CSI-2 over C-PHY (N-Phase) Data Path

Triode Data Path

**Transmitter**
- Take in 16 bits, generate 7 symbols
- 21 = 7 symbols, 3 FRP bits each.
- 3 bits define one of 5 state transitions

**Channel**
- Seven 3-phase-polarity-encoded symbols for each 16-bit word
- Each symbol has five possible states
- The change on ABC from one symbol to the next defines the symbol value

**Receiver**
- Receive 7 symbols, output 16 bits

Transmission sequence of a 16-bit word

```
  78  9a
```

Mapper

Seven FRP Commands

**Master side**

```
"A" to "B" (+x state)
```

```markdown
Z = 50
R_{TERMINAL} = 50
```

Slave side

```
"A" to "B" (+x state)
```

```markdown
Z = 50
R_{TERMINAL} = 50
```

MIF Tree Area

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N-Phase (CSI-2 over C-PHY): 6 states using 3 wires
### N-Phase: 5 Transition arcs

<table>
<thead>
<tr>
<th>Trio State</th>
<th>Wire Amplitude</th>
<th>Receiver diff input voltage</th>
<th>Receiver digital output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A</td>
<td>B</td>
<td>C</td>
</tr>
<tr>
<td>+X</td>
<td>+V</td>
<td>0</td>
<td>+V/2</td>
</tr>
<tr>
<td>-X</td>
<td>0</td>
<td>+V</td>
<td>+V/2</td>
</tr>
<tr>
<td>+Y</td>
<td>+V/2</td>
<td>+V</td>
<td>0</td>
</tr>
<tr>
<td>-Y</td>
<td>+V/2</td>
<td>0</td>
<td>+V</td>
</tr>
<tr>
<td>+Z</td>
<td>0</td>
<td>+V/2</td>
<td>+V</td>
</tr>
<tr>
<td>-Z</td>
<td>+V</td>
<td>+V/2</td>
<td>0</td>
</tr>
</tbody>
</table>

**3Ph Trio Arcs**

- **Y**: V/2, 0, V, 0.5+1, 0.5
- **X**: V, 0, V/2, -V, 0.5-0.5
- **Z**: 0, V/2, V, 0, 0.5+1

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### N-Phase: 16-bit to 7 FRP command mapping

#### Composition of 16-bit value, Tx Data[15:0] or Rx Data[15:0]

<table>
<thead>
<tr>
<th>Value</th>
<th>Action</th>
<th>16-bit Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td></td>
<td>0x0000</td>
</tr>
<tr>
<td>0001</td>
<td></td>
<td>0x0001</td>
</tr>
<tr>
<td>0010</td>
<td></td>
<td>0x0010</td>
</tr>
<tr>
<td>0011</td>
<td></td>
<td>0x0011</td>
</tr>
<tr>
<td>0100</td>
<td></td>
<td>0x0100</td>
</tr>
<tr>
<td>0101</td>
<td></td>
<td>0x0101</td>
</tr>
<tr>
<td>0110</td>
<td></td>
<td>0x0110</td>
</tr>
<tr>
<td>0111</td>
<td></td>
<td>0x0111</td>
</tr>
<tr>
<td>1000</td>
<td></td>
<td>0x1000</td>
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<tr>
<td>1001</td>
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</tr>
<tr>
<td>1010</td>
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<tr>
<td>1011</td>
<td></td>
<td>0x1011</td>
</tr>
<tr>
<td>1100</td>
<td></td>
<td>0x1100</td>
</tr>
<tr>
<td>1101</td>
<td></td>
<td>0x1101</td>
</tr>
<tr>
<td>1110</td>
<td></td>
<td>0x1110</td>
</tr>
<tr>
<td>1111</td>
<td></td>
<td>0x1111</td>
</tr>
</tbody>
</table>

#### Legend for abbreviated bit values above
- ro0 ⇒ Rotate[0]
- ro0 ⇒ Polarity[0]
- ro1 ⇒ Rotate[1]
- ro1 ⇒ Polarity[1]
- ro2 ⇒ Rotate[2]
- ro2 ⇒ Polarity[2]
- ro3 ⇒ Rotate[3]
- ro3 ⇒ Polarity[3]
- ro4 ⇒ Rotate[4]
- ro4 ⇒ Polarity[4]
- ro5 ⇒ Rotate[5]
- ro5 ⇒ Polarity[5]
- ro6 ⇒ Rotate[6]
- ro6 ⇒ Polarity[6]

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### N-Phase: Example of CSI-2 pixel data to C-PHY signaling 1/2

<table>
<thead>
<tr>
<th>16-bit Pix Data hex</th>
<th>16-bit Pix Data decimal</th>
<th>Mapping to symbols over 7 UI Region</th>
<th>Encoding to Wire State State</th>
<th>A</th>
<th>B</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>789a</td>
<td>30874</td>
<td>3; 4K</td>
<td>+x</td>
<td>V</td>
<td>0</td>
<td>V/2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>bcede</td>
<td>48350</td>
<td>4,0; 1K</td>
<td>+y</td>
<td>V/2</td>
<td>V</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>+z</td>
<td>0</td>
<td>V/2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>+y</td>
<td>V/2</td>
<td>V</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>+y</td>
<td>V/2</td>
<td>V</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>+z</td>
<td>0</td>
<td>V/2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>+y</td>
<td>V/2</td>
<td>V</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>+z</td>
<td>0</td>
<td>V/2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>+z</td>
<td>0</td>
<td>V/2</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>
N-Phase: Example of CSI-2 pixel data to C-PHY signaling 2/2
N-Phase Mission Critical Transfers 1/2

PH

C-PHY Packet Data

PF

32-bit PACKET HEADER (PH)

PACKET DATA: Length = Word Count (WC) * Data Word Width (8-bits). There are NO restrictions on the values of the data words

16-bit PACKET FOOTER (PF)

Total Packet Byte Count = 2n

Lane 1

SOT  PH  ESC  PH  Byte 1  Byte 0  Byte 3  Byte 2  Byte 2n-3  Byte 2n-4  Byte 2n-1  Byte 2n-2  EoT

Total Packet Byte Count = 2n+1

Lane 1

SOT  PH  ESC  PH  Byte 1  Byte 0  Byte 3  Byte 2  Byte 2n-1  Byte 2n-2  Filler  Byte 2n  EoT
### N-Phase mission critical transfers 2/2

#### Link Error Example (a): Loss of No Symbol Clocks

<table>
<thead>
<tr>
<th>Symbol Interval</th>
<th>Transmitted Symbols</th>
<th>Received Symbols</th>
</tr>
</thead>
<tbody>
<tr>
<td>s0 s1 s2 s3 s4 s5</td>
<td>2 1 3 2 1 3 0 3 4 4 4 4 3 2 4 3</td>
<td>2 1 3 2 1 3 2 1 4 4 4 4 3 2 4 3</td>
</tr>
</tbody>
</table>

- **Transmitted Symbols:**
  - +z: point at which symbol clock is lost
  - +y: point at which symbol clock is restored
  - -x: point of incorrect word alignment
  - -y: point at which correct word alignment is restored

- **Wire States:**
  - +z: point at which symbol clock is lost
  - +y: point at which symbol clock is restored
  - -x: point of incorrect word alignment
  - -y: point at which correct word alignment is restored

- **Notes:**
  - Symbols are transmitted serially from left to right
  - Wire state and symbol errors are highlighted in yellow

#### Link Error Example (b): Loss of One Symbol Clock

<table>
<thead>
<tr>
<th>Symbol Interval</th>
<th>Transmitted Symbols</th>
<th>Received Symbols</th>
</tr>
</thead>
<tbody>
<tr>
<td>s0 s1 s2 s3 s4 s5</td>
<td>1 3 0 3 4 1 4 3 4 4 4 4 3 0 3 1</td>
<td>1 3 0 3 4 1 1 7 4 4 4 4 4 3 0 3 1</td>
</tr>
</tbody>
</table>

#### Link Error Example (c): Loss of Two Symbol Clocks

<table>
<thead>
<tr>
<th>Symbol Interval</th>
<th>Transmitted Symbols</th>
<th>Received Symbols</th>
</tr>
</thead>
<tbody>
<tr>
<td>s0 s1 s2 s3 s4 s5</td>
<td>4 3 1 2 0 1 1 3 4 4 4 4 4 3 0 2 4</td>
<td>4 3 1 2 0 1 1 1 4 4 4 4 4 3 0 2 4</td>
</tr>
</tbody>
</table>

- **Notes:**
  - Symbols are transmitted serially from left to right
  - Wire state and symbol errors are highlighted in yellow
  - ▲: point at which symbol clock is lost
  - ▲: point at which symbol clock is restored
  - ●: point of incorrect word alignment
  - ◆: point at which correct word alignment is restored
## Evolution of CSI-2 Imaging Interface

<table>
<thead>
<tr>
<th>Imaging Interface</th>
<th>Description</th>
<th>Interface Performance</th>
<th>Release / Adoption</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gen 1</td>
<td><strong>CSI-2 v1.1</strong> protocol over D-PHY v1.1 (at 1.5 Gbps), and bidirectional command over I2C_FM (at 400 Kbps)</td>
<td><strong>Provides effective (usable) BW of 3 Gbps over 6 D-PHY v1.1 pins</strong></td>
<td>EOY 2012</td>
</tr>
<tr>
<td>Gen 2</td>
<td><strong>CSI-2 v1.2</strong> protocol over D-PHY v1.2 (at 2.5 Gbps), and bidirectional command over I2C_FM (at 400 Kbps)</td>
<td><strong>CSI-2 v1.3</strong> protocol over C-PHY v1.0 (2.5 Gsps or 5.7 Gbps) and D-PHY v1.2 (at 2.5 Gbps), and bidirectional command over I2C_FM (at 400 Kbps)</td>
<td><strong>Provides effective (usable) BW of 5 Gbps over 6 D-PHY v1.2 pins</strong>  <strong>Provides effective (usable) BW of 11.43 Gbps over 6 C-PHY v1.0 pins</strong></td>
</tr>
<tr>
<td>Gen 3</td>
<td><strong>CSI-2 v2.0</strong> protocol supports C-PHY v1.2 and D-PHY v2.1, with bidirectional command over I2C_FMP (1GHz) and I3C v1.0.</td>
<td>** CSI-2 v2.0** protocol supports C-PHY v1.2 and D-PHY v2.1, with bidirectional command over I2C_FMP (1GHz) and I3C v1.0.  <strong>C-PHY v1.2</strong> provides up to <strong>4.5 Gsps (10.3 Gbps)</strong> over <strong>3 pins</strong>  <strong>D-PHY v2.1</strong> provides up to <strong>4.5 Gbps over 4 pins</strong>  <strong>Bidirectional CCI over I2C_FMP provides around 880 Kbps of effective BW, and CCI over I3C v1.0 provides effective BW of: 10.67 Mbps over SDR, 19.2 Mbps over HDR-DDR, 18 Mbps over HDR-TSL, and 29.3 Mbps over HDR-TSP.</strong>  <strong>Provides effective (usable) BW of 9 Gbps over 6 D-PHY v2.1 pins</strong>  <strong>Provides effective (usable) BW of 20.6 Gbps over 6 C-PHY v1.2 pins</strong></td>
<td>EOY 2016</td>
</tr>
</tbody>
</table>
CSI-2 over C-PHY PSD emission reduction from scrambling
CSI-2 over D-PHY PSD emission reduction from scrambling
CSI-2 Latency Reduction Transport Efficiency

- Reduce latency and improve efficiency (preserving PHY based delimiters / B2B)
- Provides longer reach over C/D-PHYs without need for redrivers or retimers
- Alleviates electrical overstress current leakages impediments
CSI-2 Sensor Fusion using CCI

Effective (usable) BW: 5 Gbps
- Gross BW: 5 Gbps
- Channel Rate: 2.5 Gbps

Effective (usable) BW: 11.4 Gbps
- Gross BW: 11.4 Gbps
- Channel Rate: 2.5 Gbps

CSI-2 D-PHY
- TX
- RX

CSI-2 C-PHY
- TX
- RX

I2C Compatible 2-wire Camera Control

AF, Gyro, OIS, Flash, MEMS

Pin compatible coexistence supports
CSI-2 over combo C/D-PHY solutions
CSI-2 CCI and AON Advancements 1/2

- Optimal pathway for multiple forward-looking advancements in imaging
  - Drivers: Health, Convenience, Security, Lifestyle, Efficiency
  - High-perf pixel conduit needs met with C/D-PHY advancements
  - Broad definitions and fuzzy range: (i.e. Wearable: Near Body, On Body, In Body)
  - Define imaging requirements for CCI, emerging AOI, array, and non-symmetrical applications

- Camera Controller Interface (CCI) and AON advancement considerations using I2C / I3C (SDR DDR, TSL, TSP)
  - Point-to-Point and Multi-Drop configurations
CSI-2 CCI and AON Advancements 2/2
CSI-2 over C-PHY Virtual Channel Extension

5-bit Reserved Field (RES) + 3-bit Virtual Channel Extension (VCX) bit:
RES (bits 7:3) is set to zero and reserved for future use.
VCX (bit 2:0) is the most significant bits of the 5-bit Virtual Channel Identifier for the C-PHY Physical Layer option.

8-bit DATA IDENTIFIER (DI):
Contains the 2-bit Virtual Channel (VC) and the 6-bit Data Type (DT) Information.
VC (bits 7:6) is the least significant two bits of the 3-bit Virtual Channel Identifier. DT (bits 5:0) denotes the format/content of the Application Specific Payload Data. Used by the application specific layer.

16-bit WORD COUNT (WC):
The receiver reads the next WC 8-bit data words following the Packet Header.
The receiver uses the WC value to determine the end of the Packet Payload.

16-bit Cyclic Redundancy Check Code (PH-CRC):
16-bit CRC code for the Packet Header; computed over the Reserved, Data ID, and Word Count fields (4 bytes). Enables multi-bit errors to be detected.

CSI-2 *Insert Sync Word* PPI Command:
The physical layer simultaneously inserts a Sync Word on all N Lanes at this point as a result of executing a CSI-2 PPI command.

16-Bit Packet Data CRC:
Computed over WC Packet Data Words
Set to \( \theta \)
Set to \( \theta \)

**PACKET HEADER (PH): 6N x 16-bits**
(\( N = \) Physical Layer Lane Count)

**PACKET DATA**:
Length = Word Count (WC) * Data Word Width (8-bits). There are NO restrictions on the values of the data words

16-bit PACKET FOOTER (PF)
FILLER:
FC 8-bit bytes added to ensure that all Lanes transport the same number of 16-bit words; FC may be 0.
CSI-2 over D-PHY Virtual Channel Extension

8-bit DATA IDENTIFIER (DI):
Contains the 2-bit Virtual Channel (VC) and the 6-bit Data Type (DT) Information.
VC (bits 7:6) is the least significant two bits of the 3-bit Virtual Channel Identifier. DT (bits 5:0) denotes the format/content of the Application Specific Payload Data. Used by the application specific layer.

16-bit WORD COUNT (WC):
The receiver reads the next WC data words independent of their values. The receiver is NOT looking for any embedded sync sequences within the payload data. The receiver uses the WC value to determine the end of the Packet Payload.

6-bit Error Correction Code (ECC) + 2 Virtual Channel Extension (VCX) bits
ECC (bits 5:0) enables 1-bit errors within the packet header to be corrected and 2-bit errors to be detected. VCX (bits 7:6) are the most significant bit of the 4-bit Virtual Channel Identifier for the D-PHY physical layer option.

APPLICATION SPECIFIC PAYLOAD

CHECKSUM/CRC (CS)

32-bit PACKET HEADER (PH)

PACKET DATA:
Length = Word Count (WC) * Data Word Width (8-bits). There are NO restrictions on the values of the data words

16-bit PACKET FOOTER (PF)
CSI-2 DPCM & HDR Advancements

- DPCM 12-10-12
  - SNR & IQ Benefits over varying degrees of noise, edges, MTF
  - Superior to straight RAW-10 capture or existing DPCM 12-8-12
CSI-2 HDR Advancements

• HDR-16

- P1[15:8] (A) - P1[7:0] (A) - P2[15:8] (B) - P2[7:0] (B)


- Byte Values Transmitted LS Bit First

- Byte n, Byte n+1, Byte n+2, Byte n+3

b0 b1 b2 b3 b4 b5 b6 b7 b0 b1 b2 b3 b4 b5 b6 b7 b0 b1 b2 b3 b4 b5 b6 b7

• HDR-20

- P1[19:12] (A) - P1[9:2] (A) - P2[19:12] (B) - P2[9:2] (B)


- Byte Values Transmitted LS Bit First

- Byte n, Byte n+1, Byte n+2, Byte n+3

b0 b1 b2 b3 b4 b5 b6 b7 b0 b1 b2 b3 b4 b5 b6 b7 b0 b1 b2 b3 b4 b5 b6 b7
Questions?
Backup
# MIPI C/D/M PHYs

## PHY Characteristics

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>M-PHY v3.1</th>
<th>D-PHY v1.2</th>
<th>C-PHY v1.0</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Primary use case</strong></td>
<td>Performance driven, bidirectional packet/network oriented interface</td>
<td>Efficient unidirectional streaming interface, with low speed in-band reverse channel</td>
<td>Efficient unidirectional streaming interface, with low speed in-band reverse channel</td>
</tr>
<tr>
<td><strong>HS clocking method</strong></td>
<td>Embedded Clock</td>
<td>DDR Source-Sync Clock</td>
<td>Embedded Clock</td>
</tr>
<tr>
<td><strong>Channel compensation</strong></td>
<td>Equalization</td>
<td>Data skew control relative to clock</td>
<td>Encoding to reduce data toggle rate</td>
</tr>
<tr>
<td><strong>Minimum configuration and pins</strong></td>
<td>1 lane per direction, dual-simplex, 2 pins each (4 total)</td>
<td>1 lane plus clock, simplex, 4 pins</td>
<td>1 lane (trio), simplex, 3 pins</td>
</tr>
<tr>
<td><strong>Maximum transmitter swing amplitude</strong></td>
<td>SA: 250mV (peak) LA: 500mV (peak)</td>
<td>LP: 1300mV (peak) HS: 360mV (peak)</td>
<td>LP: 1300mV (peak) HS: 425mV (peak)</td>
</tr>
<tr>
<td><strong>Data rate per lane (HS)</strong></td>
<td>HS-G1: 1.25, 1.45 Gb/s HS-G2: 2.5, 2.9 Gb/s HS-G3: 5.0, 5.8 Gb/s (Line rates are 8b10b encoded)</td>
<td>80 Mbps to ~2.5 Gbps (aggregate)</td>
<td>80Msym/s to 2.5 Gsym/s times 2.28 bits/sym, or max 5.7 Gbps (aggregate)</td>
</tr>
<tr>
<td><strong>Data rate per lane (LS)</strong></td>
<td>10kbps ~ 600 Mbps</td>
<td>&lt; 10 Mbps</td>
<td>&lt; 10 Mbps</td>
</tr>
<tr>
<td><strong>Bandwidth per Port (3 or 4 lanes)</strong></td>
<td>~ 4.0 ~ 18.6 Gb/s (aggregate BW)</td>
<td>Max ~10 Gbps per 4-lane port (aggregate)</td>
<td>Max ~ 17.1 Gbps per 3-lane port (aggregate)</td>
</tr>
<tr>
<td><strong>Typical pins per Port (3 or 4 lanes)</strong></td>
<td>10 (4 lanes TX, 1 lane RX)</td>
<td>10 (4 lanes, 1 lane clock)</td>
<td>9 (3 lanes)</td>
</tr>
</tbody>
</table>
CSI-2 over D-PHY signaling
CSI-2 over C-PHY (N-Phase) signaling

**Diagram Description:**

- **Preamble:**
  - Composed of: 3,3,3,3,3, with mid-section consisting of a programmable sequence.
  - Reset initializes all to 3,3,3,3,3.

- **Sync Word:**
  - 3,4,4,4,4,4,3 (Least Significant Symbol first)

- **Packet Data:**
  - Post is composed of multiple of unused code word: 4,4,4,4,4,4

**Timeline:**

- **LP-111:**
  - LP-001
  - LP-000

- **A/B/C:**
  - LP-111
  - LP-001
  - LP-000

- **Important Timings:**
  - t3-PREBEGIN
  - t3-PROGSEQ
  - t3-PREEND
  - t3-SYNC
  - t3-TERM-EN
  - t3-SETTLE
  - t3-PREPARE
  - t3-POST
  - t3-EXIT
  - t3-REOT