MIPI UniPort-M
Integrating the M-PORT into UniPro

Jürgen Urban
UniPro Working Group Chairman
11 Nov. 2015 – MIPI Member Webinar
Legal Disclaimer

The material contained herein is not a license, either expressly or impliedly, to any IPR owned or controlled by any of the authors or developers of this material or MIPI®. The material contained herein is provided on an “AS IS” basis and to the maximum extent permitted by applicable law, this material is provided AS IS AND WITH ALL FAULTS, and the authors and developers of this material and MIPI hereby disclaim all other warranties and conditions, either express, implied or statutory, including, but not limited to, any (if any) implied warranties, duties or conditions of merchantability, of fitness for a particular purpose, of accuracy or completeness of responses, of results, of workmanlike effort, of lack of viruses, and of lack of negligence. ALSO, THERE IS NO WARRANTY OR CONDITION OF TITLE, QUIET ENJOYMENT, QUIET POSSESSION, CORRESPONDENCE TO DESCRIPTION OR NON-INFRINGEMENT WITH REGARD TO THIS MATERIAL.

All materials contained herein are protected by copyright laws, and may not be reproduced, republished, distributed, transmitted, displayed, broadcast or otherwise exploited in any manner without the express prior written permission of MIPI Alliance. MIPI, MIPI Alliance and the dotted rainbow arch and all related trademarks, tradenames, and other intellectual property are the exclusive property of MIPI Alliance and cannot be used without its express prior written permission.

IN NO EVENT WILL ANY AUTHOR OR DEVELOPER OF THIS MATERIAL OR MIPI BE LIABLE TO ANY OTHER PARTY FOR THE COST OF PROCURING SUBSTITUTE GOODS OR SERVICES, LOST PROFITS, LOSS OF USE, LOSS OF DATA, OR ANY INCIDENTAL, CONSEQUENTIAL, DIRECT, INDIRECT, OR SPECIAL DAMAGES WHETHER UNDER CONTRACT, TORT, WARRANTY, OR OTHERWISE, ARISING IN ANY WAY OUT OF THIS OR ANY OTHER AGREEMENT RELATING TO THIS MATERIAL, WHETHER OR NOT SUCH PARTY HAD ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.
MIPI Alliance: A Brief Introduction

Peter B. Lefkin
Managing Director
About MIPI Alliance

• 282 Members (as of 31 October 2015)
• 45+ specifications and supporting docs
• We drive mobile and mobile-influenced interface technology through the development of hardware and software specifications
• We work globally and collaboratively with other standards bodies to benefit the mobile ecosystem
MIPI Alliance Member Ecosystem
Active MIPI Alliance Working Groups

- Camera
- Debug
- Display
- Low Latency Interface
- Low Speed Multipoint Link (New - SoundWire\textsuperscript{SM})
- Marketing

- PHY (C / D / M)
- Reduced Input Output (RIO) (New)
- Sensor / I3C\textsuperscript{SM} (New)
- Software (New)
- Technical Steering Group
- Test
- \textbf{UniPro}\textsuperscript{SM}
Recent Announcements

- 29 October 2015 - MIPI Alliance Introduces a Family of MIPI Gigabit Debug Interface Specifications for Mobile and Mobile-Influenced Designs

- 12 August - MIPI Alliance Releases New MIPI M-PHY v4.0 Specification, Achieving a Peak Transmission Rate of Nearly 12 Gbps
The Future of MIPI – Beyond Mobile

• Mobile influences everything

• Everything gets faster, smaller and lower power
  – MIPI will continue to evolve specs to take advantage of the evolution of technology in mobile devices
11 Nov. 2015 - MIPI Member Webinar MIPI UniPort-M Integrating the M-PORT into UniPro

• Facilitator
  Peter Lefkin – Managing Director, MIPI Alliance

• Presenter
  Jürgen Urban – Chairman, MIPI UniPro Working Group
Contact

• Slide set available under:
  – Public site - http://mipi.org/learning-center/webinars
  – Members site open to all members - https://members.mipi.org/wg/Marketing/document/folder/5737

• In case of further questions/feedback:
  – UniPro-questions@mipi.org (Adopters)
  – bugzilla@mipi.org (Contributors)
Agenda

• Definitions and Conventions
• M-PHY SAP mapping to RMMI
• Intra LANE timings
• UniPort_M intra SUB-LINK timings
• UniPort_M LINK timings
• Q&A
DEFINITIONS AND CONVENTIONS
Disclaimer

• This Webinar lays out the UniPro WG perspective on M-PHY integration
  – Other protocols using M-PHY may look at a different angle towards M-PHY integration
  – Discussion baseline: UniPro v1.6x + M-PHY v3.x

• This Webinar discusses implementations
  – It does not claim or intend to deliver universal implementation truths
  – Other solutions/interpretations conformant with both, M-PHY and UniPro specification may rightfully exist
  – In case of contradictions/ambiguities the spec prevails
## LANE Categorization

<table>
<thead>
<tr>
<th>physical implementation</th>
<th>LSS</th>
<th>Connection state after LSS</th>
<th>Lane state after LSS</th>
<th>M-PHY state</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Lane</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>physical Lane</td>
<td></td>
<td>Logical Lane</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>unavailable Lane</td>
<td></td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td></td>
</tr>
<tr>
<td>available Lane</td>
<td></td>
<td>unconnected Lane</td>
<td>off (Off_Mode)</td>
<td>unpowered</td>
<td></td>
</tr>
<tr>
<td>Count in PA_AvailTxDataLanes and PA_AvailRxDataLanes</td>
<td></td>
<td>inactive/unused (Hibernate_Mode)</td>
<td>HIBERN8</td>
<td>no count in PA_ACTIVE_TxDataLanes or PA_ACTIVE_RxDataLanes</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Count in PA_CONNECTED Tx DataLanes and PA_CONNECTED Rx DataLanes</td>
<td>inactive, unused Lane, dummy burst (LinkCfg)</td>
<td>ACTIVATED, HIBERN8</td>
<td>no de-skew symbol, skip patterns, scrambling, dummy payload, no count in PA_ACTIVE_TxDataLanes or PA_ACTIVE_RxDataLanes</td>
</tr>
<tr>
<td></td>
<td></td>
<td>active/used Lane (FastMode, SlowMode, FastAuto_Mode, SlowAuto_Mode, Hibernate_Mode)</td>
<td>ACTIVATED, HIBERN8</td>
<td>no count in PA_ACTIVE_TxDataLanes or PA_ACTIVE_RxDataLanes</td>
<td></td>
</tr>
</tbody>
</table>

**Red Text:** Terminology used in UniPro v1.6x  
**Blue Text:** Terminology used in M-PHY v3.x
Dummy BURST

- Dummy Bursts are used during PACP_PWR_req traffic to configure inactive Lanes in synchronization with potentially attached Media Converters
  - During PACP_PWR_req a BURST or a dummy BURST is started on all connected LANEs
  - The peer M-RX ignores Dummy BURSTs
  - Dummy Bursts are not part of the MK0, MK1 Lane deskew.
  - Dummy Bursts, however, follow entirely the M-PHY spec (they require prepare/sync period, MK0 and TOB)
  - Dummy Bursts are scrambled, if requested
We use the Link terminology found in M-PHY spec. Note: The UniPro spec does not know SUB-LINKs, they are called LINK there.
Logical Lane versus physical Lane

• Logical Lane numbering does typically not match w/ physical Lane numbering
  – M-PORT clocking is primarily driven by state of logical LANE #0
  – M-PORT needs to know LANE mapping from UniPro to derive the necessary M-PHY clocking

• Alternatively:
  – Application may restrict arbitrary PCB routing
  – Logical Lane is always identical to physical Lane
LINECFG

• LINE-CFG is used for Media Converters
• UniPro v1.41:
  – M-PHY LINECFG implementation and use is mandated
• UniPro v1.6x:
  – M-PHY LINECFG implementation is mandated (for backward compatibility w/ v1.41)
  – M-PHY LINECFG use is not mandated, left to the application to decide.
  – M-RX must be able to tolerate a LINECFG sequence, i.e. re-sync to SLEEP/STALL at DIF-N
  – If PA_Local_TX_LCC_Enable=0, there is no expectation that the M-TX ever emits LINECFG.
M-PHY SAP MAPPING TO RMMI
# M-TX DATA SAP and RMMI

<table>
<thead>
<tr>
<th>M-PHY SAP</th>
<th>RMMI Mapping</th>
<th>Reference clocking</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>M-LANE-SYMBOL</td>
<td>request TX_ProtDORDY; TX_Symbol; TX_DataNCtrl</td>
<td>TX_SymbolClk</td>
<td>The UniPro stack should issue changes to TX_ProtDORDY on the same clock cycle for all active Lanes in a multi-LANE LINK. Failing to synchronize TX_ProtDORDY leads to errors in the PA_PDU lane distribution and merging.</td>
</tr>
<tr>
<td>M-LANE-SYMBOL</td>
<td>confirm TX_ProtDORDY &amp;&amp; TX_PhyDIRDY</td>
<td>TX_SymbolClk</td>
<td>TX_PhyDIRDY signals only readiness of the M-TX to receive data from the stack. Only in conjunction with TX_ProtDORDY the UniPro stack interprets a confirm and advances to the next Symbol data. In a multi-LANE LINK, the UniPro stack must receive (TX_ProtDORDY &amp;&amp; TX_PhyDIRDY) on all M-TX LANES at the same time for not breaking the PA_PDU lane distribution.</td>
</tr>
<tr>
<td>M-LANE-PREPARE</td>
<td>request rising edge (TX_Burst)</td>
<td>TX_SymbolClk</td>
<td>UniPro uses the M-TX generated default SYNC pattern.</td>
</tr>
<tr>
<td>M-LANE-PREPARE</td>
<td>confirm rising edge (TX_SaveState_Status_N) after rising edge (TX_Burst)</td>
<td>TX_SymbolClk</td>
<td>UniPro uses the M-TX generated default SYNC pattern.</td>
</tr>
<tr>
<td>M-LANE-SYNC</td>
<td>request unused in UniPro</td>
<td></td>
<td>M-LANE-Sync.confirm cannot be represented using TX_SaveState_Status_N as entry into LINE-CFG separates the two events. It cannot be represented as a function of the falling edge of TX_Burst, as the M-PHY adds BurstClosure extension in PWM traffic.</td>
</tr>
<tr>
<td>M-LANE-Sync</td>
<td>confirm unused in UniPro</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M-LANE-BurstEnd</td>
<td>request falling edge (TX_Burst)</td>
<td>TX_SymbolClk</td>
<td>M-LANE-BurstEnd.confirm cannot be represented using TX_SaveState_Status_N as entry into LINE-CFG separates the two events. It cannot be represented as a function of the falling edge of TX_Burst, as the M-PHY adds BurstClosure extension in PWM traffic.</td>
</tr>
<tr>
<td>M-LANE-BurstEnd</td>
<td>confirm no mapping in RMMI</td>
<td>TX_SymbolClk</td>
<td>There is no direct mapping into RMMI. M-LANE-SaveState.indication indicates entry into SLEEP or into STALL state but does not indicate entry into HIBERN8. TX_SaveState_Status_N is a level sensitive signal indicating also also a HIBERN8 state.</td>
</tr>
<tr>
<td>M-LANE-SaveState</td>
<td>indication falling edge (TX_SaveState_Status_N)</td>
<td>TX_SymbolClk</td>
<td></td>
</tr>
</tbody>
</table>
**M-TX SYMBOL RMMI mapping**

### GOOD!

- **SAVE**
- **PREPARE**
- **SYNC**
- **PAYLOAD**
- **Trailing**
- **TOB**
- **SAVE**

### BAD!

- **SAVE**
- **PREPARE**
- **SYNC**
- **PAYLOAD**
- **Trailing**
- **TOB**
- **SAVE**

### Legitimate (asking for trouble!)

- **SAVE**
- **PREPARE**
- **SYNC**
- **PAYLOAD**
- **Trailing**
- **TOB**
- **SAVE**

---

**M-TX needs to transform this into SYNC!**

<table>
<thead>
<tr>
<th>TX_Symbol[31:0]</th>
<th>TX_ProtDORDY[3:0]</th>
<th>MARKER1</th>
<th>MARKER0</th>
<th>FILLER</th>
<th>FILLER</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

- **e.g. PA_PDU #2**

---

Copyright © 2015 MIPI Alliance. All rights reserved.
## M-RX DATA SAP and RMMI

<table>
<thead>
<tr>
<th>M-PHY SAP</th>
<th>RMMI Mapping</th>
<th>Reference clocking</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>M-LANE-SYM</td>
<td>RX_Symbol; RX_SymbolErr; RX_DataNCtrl; RX_PhyDORDY;</td>
<td>RX_SymbolClk</td>
<td></td>
</tr>
<tr>
<td>M-LANE-PRO</td>
<td>rising edge (RX_Burst)</td>
<td>RX_SymbolClk</td>
<td>rising edge means synchronous edge detection</td>
</tr>
<tr>
<td>M-LANE-BurstEnd</td>
<td>falling edge (RX_Burst)</td>
<td>RX_SymbolClk</td>
<td>falling edge means synchronous edge detection</td>
</tr>
<tr>
<td>M-LANE-HIBERN8Exit</td>
<td>rising edge (RX_Hibern8Exit_Type_I)</td>
<td>Async</td>
<td>At the time of exit from HIBERN8, there is typically no RX_SymbolClk available. The asynchronous signal may be used to switch on RX_SymbolClk at system level. The UniPro protocol may then use a sampled version of this RMMI signal</td>
</tr>
<tr>
<td>M-LANE-MRXSaveState</td>
<td>No representation in the RX_SymbolClk domain, fallback solution: falling edge (RX_CfgRdyN) after falling edge (RX_Burst)</td>
<td>RX_CfgClk</td>
<td>There is no corresponding representation of this M-RX Data SAP in RMMI. The end of a BURST indicated by M-LANE-BurstEnd.indication may differ substantially from M-LANE-SaveState.indication in case of running through LINE-CFG or in case of a long PWM Tail-of-Burst. It is assumed the M-RX keeps RX_CfgRdyN high during TOB and LINE-CFG and asserts it to low only, when entering SAVE state</td>
</tr>
</tbody>
</table>
# M-TX CTRL SAP and RMMI

<table>
<thead>
<tr>
<th>M-PHY SAP</th>
<th>RMMI Mapping</th>
<th>Reference clocking</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>M-CTRL-CFGGET</td>
<td>request ~TX_AttrWRn &amp;&amp; TX_CfgEnbl</td>
<td>TX_CfgClk</td>
<td>There is no mandate for an M-Phy to implement TX_CfgRdyN = High after M-CTRL-CFGGET.request</td>
</tr>
<tr>
<td>M-CTRL-CFGGET</td>
<td>confirm if (TX_Burst==0): first cycle of (TX_CfgRdyN==0) after TX_CfgEnbl</td>
<td>TX_CfgClk</td>
<td>Usually only during TX_BURST==1, exception: TX_HIBERN8_Control</td>
</tr>
<tr>
<td>M-CTRL-CFGGET</td>
<td>confirm if (TX_Burst==1): N/A</td>
<td>TX_CfgClk</td>
<td>During BURST, TX_CfgRdyN is always high. The confirm is postponed until after the M-TX enters SAVE state and executes RCT.</td>
</tr>
<tr>
<td>M-CTRL-CFGSET</td>
<td>request TX_AttrWRn &amp;&amp; TX_CfgEnbl</td>
<td>TX_CfgClk</td>
<td>There is no mandate for an M-Phy to implement TX_CfgRdyN = High after M-CTRL-CFGSET.request</td>
</tr>
<tr>
<td>M-CTRL-CFGSET</td>
<td>confirm first cycle of (TX_CfgRdyN==0) after M-CTRL-CFGREADY.request</td>
<td>TX_CfgClk</td>
<td>No M-TX CTRL SAP representation exists for this RMMI signal. UniPro does not use this signal, the corresponding M-PHY input should be clamped to appropriate values.</td>
</tr>
<tr>
<td>M-CTRL-RESET</td>
<td>request TX_Reset</td>
<td>TX_CfgClk</td>
<td>No M-TX CTRL SAP representation exists for this RMMI signal. UniPro does not use this signal, the corresponding M-PHY input should be set to 0.</td>
</tr>
<tr>
<td>M-CTRL-RESET</td>
<td>confirm falling edge (TX_CfgRdyN) after TX_Reset</td>
<td>TX_CfgClk</td>
<td>No M-TX CTRL SAP representation exists for this RMMI signal. However, UniPro needs to control this signal, if the M-TX transmitter can drive a weak DIF-N with RSE_PO termination.</td>
</tr>
<tr>
<td>M-CTRL-LINERESET</td>
<td>request TX_LineReset</td>
<td>TX_CfgClk</td>
<td>No M-TX CTRL SAP representation exists for this RMMI signal. UniPro does not use this signal, the corresponding M-PHY input should be set to 0.</td>
</tr>
<tr>
<td>M-CTRL-LINERESET</td>
<td>confirm falling edge (TX_CfgRdyN) after TX_LineReset</td>
<td>TX_CfgClk</td>
<td>No M-TX CTRL SAP representation exists for this RMMI signal. UniPro does not use this signal, the corresponding M-PHY input should be set to 0.</td>
</tr>
<tr>
<td>N/A</td>
<td>TX_InLnCfg (unused, legacy)</td>
<td>TX_CfgClk</td>
<td>No M-TX CTRL SAP representation exists for this RMMI signal. UniPro does not use this signal, the corresponding M-PHY input should be set to 0.</td>
</tr>
<tr>
<td>N/A</td>
<td>TX_DIFNDrive (optional)</td>
<td>TX_CfgClk</td>
<td>No M-TX CTRL SAP representation exists for this RMMI signal. However, UniPro needs to control this signal, if the M-TX transmitter can drive a weak DIF-N with RSE_PO termination.</td>
</tr>
<tr>
<td>N/A</td>
<td>TX_Controlled_ActTimer (unused)</td>
<td>constant 0</td>
<td>No M-TX CTRL SAP representation exists for this RMMI signal. UniPro does not use this signal, the corresponding M-PHY input should be set to 0.</td>
</tr>
</tbody>
</table>
# M-RX CTRL SAP and RMMI

<table>
<thead>
<tr>
<th>M-PHY SAP</th>
<th>RMMI Mapping</th>
<th>Reference clocking</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>M-CTRL-CFGGET request</td>
<td>~RX_AttrWRn &amp;&amp; RX_CfgEnbl</td>
<td>RX_CfgClk</td>
<td></td>
</tr>
<tr>
<td>M-CTRL-CFGGET confirm</td>
<td>if (RX_Burst==0): first cycle of (RX_CfgRdyN==0) after M-CTRL-CFGGET.request</td>
<td>RX_CfgClk</td>
<td>There is no mandate for the M-PHY to de-assert (High Level) RX_CfgRdyN after an M-CTRL-CFGGET.request.</td>
</tr>
<tr>
<td></td>
<td>if (RX_Burst==1): N/A</td>
<td>RX_CfgClk</td>
<td></td>
</tr>
<tr>
<td></td>
<td>RX_AttrRdCnf (optional)</td>
<td>RX_CfgClk</td>
<td></td>
</tr>
<tr>
<td>M-CTRL-CFGSET request</td>
<td>RX_AttrWRn &amp;&amp; RX_CfgEnbl</td>
<td>RX_CfgClk</td>
<td></td>
</tr>
<tr>
<td>M-CTRL-CFGSET confirm</td>
<td>if (RX_Burst==0): first cycle of (RX_CfgRdyN==0) after M-CTRL-CFGSET.request</td>
<td>RX_CfgClk</td>
<td>There is no mandate for the M-PHY to de-assert (High Level) RX_CfgRdyN after an M-CTRL-CFGSET.request.</td>
</tr>
<tr>
<td></td>
<td>if (RX_Burst==1): N/A</td>
<td>RX_CfgClk</td>
<td></td>
</tr>
<tr>
<td>M-CTRL-CFGREADY request</td>
<td>RX_CfgUpdt</td>
<td>RX_CfgClk</td>
<td></td>
</tr>
<tr>
<td>M-CTRL-CFGREADY confirm</td>
<td>first cycle of (RX_CfgRdyN==0) after M-CTRL-CFGREADY.request</td>
<td>RX_CfgClk</td>
<td>There is no mandate for the M-PHY to de-assert (High Level) RX_CfgRdyN after an M-CTRL-CFGSET.request.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>During BURST, RX_CfgRdyN is always high, the confirm is postponed until after the M-RX enters SAVE state and executes RCT.</td>
</tr>
<tr>
<td>M-CTRL-RESET request</td>
<td>RX_Reset</td>
<td>RX_CfgClk</td>
<td></td>
</tr>
<tr>
<td>M-CTRL-RESET confirm</td>
<td>falling edge (RX_CfgRdyN) after falling edge (RX_RESET)</td>
<td>RX_CfgClk</td>
<td></td>
</tr>
<tr>
<td>M-CTRL-LINERESET indication</td>
<td>falling edge (RX_CfgRdyN) after falling edge (RX_LineReset)</td>
<td>RX_CfgClk</td>
<td></td>
</tr>
<tr>
<td>N/A</td>
<td>RX_InLnCfg constant</td>
<td></td>
<td>No SAP representation for this optional RMMI signal. UniPro does not use this signal.</td>
</tr>
<tr>
<td>M-CTRL-LCCReadStatus indication</td>
<td>RX_LCCRdDet</td>
<td>RX_CfgClk</td>
<td>Exists only, if LINE-CFG is implemented.</td>
</tr>
</tbody>
</table>
Unipro Configuration of M-PORT

**PA Layer:**
- M-PHY attributes requiring synchronization between local and peer are changed under PA Layer control
- Only during an open BURST
  - Exception: Configuring the exit from HIBERN8
- UniPro Protocol ensures that TX BURST and RX BURST stay open during configuration.

**Application:**
- M-PHY attributes requiring no synchronization
- Configuration at any time
- M-CTRL-CFGRDY.request must be generated by a DME_POWERMODE.req
UniPro Configuration sequence of M-TX during BURST

- M-LANE-PREPARE.request
  - M-LANE-PREPARE.confirm
- M-LANE-SYMBOL.request (MK0, CTRL)
  - M-LANE-SYMBOL.confirm
- Multiple M-CTRL-CFGSET.request
  - No M-CTRL-CFGSET.confirm (!)
- Single M-CTRL-CFGREADY.request
- M-LANE-SYMBOL.request (MK2, CTRL)
  - M-LANE-SYMBOL.confirm
- M-LANE-BurstEnd.request
  - M-LANE-BurstEnd.confirm
  - RCT
  - M-CTRL-CFGREADY.confirm
Potential Pitfall: race condition between M-TX DATA and M-TX CTRL SAP

- TX_SymbolClk
- TX_Symbol
- TX_Burst
- TX_SaveState_Status_N
- TX_CfgClk
- TX_CfgUpdt

M-LANE-BurstEnd.request

BURST  EOB  TOB  STALL

M-TX RCT

internal M-TX CfgUpdt delay

M-CTRL-CFGREADY.request
UniPro Configuration sequence of M-RX during BURST

- M-LANE-PREPARE.indication
- M-LANE-SYMBOL.indication (MK0, CTRL)
  - Multiple M-CTRL-CFGSET.request
    - No M-CTRL-CFGSET.confirm (!)
  - Single M-CTRL-CFGREADY.request
- M-LANE-SYMBOL.request (MK2, CTRL)
  - M-LANE-SYMBOL.confirm
- M-LANE-BurstEnd.request
  - M-LANE-SYMBOL.indication (MK2, CTRL)
  - M-LANE-BurstEnd.indication
  - RCT
  - M-CTRL-CFGREADY.confirm
INTRA LANE TIMINGS
**Intra Lane setup**

- In the following diagrams, one complete LANE is shown, local M-TX to peer M-RX

  ![Diagram](image)

- Only the most critical timings are shown
- SAP timings are ideal!
  - SAP.indication are signalled delayed on RMMI
  - SAP.confirm are signalled delayed on RMMI
  - SAP.request cause delayed responses inside M-PHY
HS-BURST to LINE-RESET

Local MTX

M-TX FSM:
M-TX Drive:
LINE State at MTX pins:

Peer MRX

M-RX FSM:
LINE State at MRX pins:
M-RX termination:
HS-BURST to HIBERN8

M-TX FSM:
- HS-BURST
- TOB
- STALL
- HIBERN8

M-TX Drive:
- DATA / Mk
- DIF-N(RS

LINE State at MTX pins:
- DIF-X(R or NT)
- DIF-N(R or NT)

M-LANE-BurstEnd.request
M-LANE-SaveState.indication(STALL)
M-CTRL-CFGREADY.confirm

M-RX FSM:
- HS-BURST
- TOB detection
- STALL
- HIBERN8

LINE State at MRX pins:
- DATA / Mk
- DIF-N(R or NT)

M-CTRL-CFGREADY.confirm

M-RX termination:
- HS-RX terminated, unterminated
- unterminated

TX_Hibern8Time_Capability
TX_Advanced_Hibern8Time_Capability
RX_Hibern8Time_Capability
RX_Advanced_Hibern8Time_Capability
SQD

Copyright © 2015 MIPI Alliance. All rights reserved.
HS-BURST to STALL, no Config

- M-TX FSM:
  - HS-BURST → TOB → STALL
  - M-TX Drive:
    - DATA / MKn
  - LINE State at MTX pins:
    - DIF-N(RSE_TX)
  - TX_Min_STALL_NoConfig_Time

- M-RX FSM:
  - HS-BURST → TOB detection → STALL → HS-PREPARE
  - LINE State at MRX pins:
    - DATA / MKn
  - M-RX termination:
    - HS-RX terminated, unterminated
SUB-LINK connection example

SUB-LINK example

M-TX0 → M-RX2

Logical LANE #0
M-TX1 → M-RX3

Logical LANE #1
M-TX2 → M-RX0

Logical LANE #2
M-TX3 → M-RX1

UniPro: HIBERNATE
M-TX1 → M-RX3
M-TX2 → M-RX0
M-TX3 → M-RX1

UniPro: LINKUP on 1 LANEs
M-TX1 → M-RX3
M-TX2 → M-RX0
M-TX3 → M-RX1

UniPro: LINK-CFG
M-TX1 → M-RX3
M-TX2 → M-RX0
M-TX3 → M-RX1
SUB-LINK management

• M-PHY attributes of all Lanes should be kept consistent at all times
  – May want to combine the attribute banks of all Lanes in a SUB-LINK
  – M-TX-CTRL SAP may be shared for SUB-LINK
  – M-RX-CTRL SAP may be shared for SUB-LINK

• Exception:
  – TX_DRIVER_POLARITY
  – TX_HIBERN8_Control
  – TX_HS_Equalizer_Settings
  – RX_Enter_HIBERN8
Lane Alignment

LANE 0
- SAVE
- PREPARE
- SYNC
- PAYLOAD
- Trailing
- TOB
- SAVE
- PA_PDUs
- FILLER

LANE 1
- SAVE
- PREPARE
- SYNC
- PAYLOAD
- Trailing
- TOB
- SAVE
- PA_PDUs
- FILLER

LANE 2 (good)
- SAVE
- PREPARE
- SYNC
- FILLER
- Trailing
- TOB
- SAVE
- FILLER
- FILLER

LANE 3 (bad)
- SAVE
- PREPARE
- SYNC
- FILLER
- Trailing
- TOB
- SAVE
- FILLER
- FILLER

T1
Powermode change w/ dummy BURST

- Same waveform for PACP_PWR_req and PACP_PWR_cnf
- Signal integrity:
  - LANE #1 enters/exits HIBERN8, when LANE #0 is in SAVE state
  - BURST and DUMMY BURST start and stop at same time
- LCC-MODE can either enter HIBERN8 or change Powermode, but not both at the same time
Powermode change w/ advanced MC

- Need two Powermode changes in a row:
  - 1st change activates all connected LANEs into desired GEAR and MODE
  - 2nd change de-activates unused LANEs into HIBERN8
PACP_PWR_req with retry

- PACP_PWR cnf (PWR_OK) only after second PACP_PWR_req
- During PACP_retry, the BURST must be kept open
- M-TX is configured only once even with retry
LINE-RESET in LINKUP
after unsuccessful PACP_PWR_req

- Before LINE-RESET, all LANEs are either ACTIVATED or run a DUMMY BURST, no need to wake up from HIBERN8.
- After LINE-RESET, LANE #0 is ACTIVATED in PWM-G1, all other LANEs run Dummy BURST in PWM-G1.
Entry into HIBERN8 after LINE-RESET

- LINE-RESET sends LINK into PWM-G1
- After exit from HIBERN8 the LINK is still in that MODE and GEAR and Application needs to re-program into desired GEAR
  - Check consequences for Application Auto Hibernate!
Scrambling in HS-MODE

- Scrambling is difficult to debug
  - Test equipment re-synchronizes scrambler on a SYNC symbol (MK0, MK1)
  - UniPro implementation should be able to insert periodical (MK0, MK1) for debug purposes
    - Via DME_POWERMODE.req(unchanged, unchanged)
    - Via any other implementation specific mechanism
- Scrambling should include FLR sequence after MK2
Shared RefClk

- UniPort_M does not define the frequency of the Shared RefClk
  - Application should do!
- Application may program RefClk frequency into peer before changing to HS-MODE
- M-PHY architectures requiring a shared reference clock need
  - RX_REF_CLOCK_SHARED_Capability=1 or/and
  - TX_REF_CLOCK_SHARED_Capability=1
Clocking concepts, examples

a) Host Controlled Shared RefCk

b) System Generated Shared RefCk

c) Locally Generated RefCk, no Sharing
Shared RefClk switching recommendations

- RefClk is mandatory during HS-MODE
- Switching is Application Controlled
- RefClk shall be switched on:
  - Before DME_HIBERNATE_EXIT.req into HS-MODE
  - Before DME_POWERMODE.req into HS-MODE
- RefClk should be switched off after
  - DME_HIBERNATE_ENTER.ind (after delay)
Skip architecture

L2 TX buffer

Skip insertion
Clk

8b10b encode
Clk

PISO

TX_SYMBOLCLK

Local PLL

TX

Dp

Dn

RX_SYMBOLCLK

10b8b decode
Clk

Skip removal
Clk

WrClk RdClk

WrEn

Elastic Buffer

Deskew

Ring Buffer

Clk

L2 RX buffer

Local PLL

SYMBOLCLK

RX_SYMBOLCLK

SUB-LINK

L2 TX buffer

SIPO

Clk

RX

CDR

SYMBOLCLK

+/- 2000 ppm
Purpose of SKIP architectures

• For Applications mandating same GEAR/MODE in forward and reverse SUB-LINK

• Eases core implementation by reducing clock domain crossings
  – Inserting skip reduces tx payload bandwidth up to the point the receiver can process it

• Shared RefClk based Applications may not benefit from
**LinkStartup**

- UniPro v1.61 requires a synchronized DME_RESET.req between local and peer Device
  - Synchronous reset line
  - Synchronous entry into LINK DOWN
  - Within 100ms synchronous DME_LINKSTARTUP.req()
LINKSTARTUP timeout loop

```
Local DME
  PA_LM_LINKSTARTUP.req
  LINKSTARTUP TIMER
  100ms expired
  PA_LM_LINKSTARTUP.cnf_L(FAILURE)
  PA_LM_LINKSTARTUP.ind
  100ms
  PA_LM_LINKSTARTUP.req
  LINKSTARTUP TIMER
  100ms expired

Local PA
  LINKDOWN
  Wait TRG0

Peer PA
  LINKDOWN
  TRG0
  PA_LM_LINKSTARTUP.ind

Peer DME
  100ms
  PA_LM_LINKSTARTUP.req
  LINKSTARTUP TIMER
  100ms expired
  TRG0
  100ms expired
```
Link Performance, Burst Control
Burst control from Application

- Start Tsync already with Application buffer write!
- Save power on reverse channel by keeping Tsync small
Power Saving with small TSync

![Graph showing the relationship between TSYNC_LENGTH (coarse) and Percent in STALL for different OutAck values.](image-url)
QUESTIONS AND (HOPEFULLY) ANSWERS
BACKUP SLIDES
Shared RefClk switching (informative)

- Shared RefClk shall not be switched off
  - With DME_RESET.req (is only local!)
  - With DME_LINKLOSS.ind (only inbound Link!)
  - With detected LINE-RESET (unsynchronized between forward and reverse channel)
  - After a PWR_FATAL response (peer may need RefClk to recover!)

- Shared RefClk may be switched off
  - After DME_POWERMODE.ind(PWR_OK) for both SUB-LINKs into LS-MODE (after delay)
  - DME_POWERMODE.cnf (FAILURE), when none of the SUB-LINKs is in HS-MODE
  - DME_LINKSTARTUP.ind()
LINECFG to HIBERN8

M-TX FSM:
- T1: LCC-MODE
- T2: SAVE
- T7: HIBERN8
- T8: HIBERN8

M-TX Drive:
- PWM b0, PWM b1
- DIF-N(RxSE_TX)
- DIF-Q
- DIF-Z

LINE state at M-TX pins:
- PWM b0, PWM b1
- T1: LCC-MODE
- T2: SAVE
- T7: HIBERN8
- T8: HIBERN8

M-RX FSM:
- T1: LCC-MODE
- T2: SAVE
- T7: HIBERN8
- T8: HIBERN8

M-RX termination:
- PWM-RX unterminated, terminated
- SQ-RX, no SQD
- SQ-RX, SQD

LINE state at M-RX:
- PWM b0, PWM b1
- T1: LCC-MODE
- T2: SAVE
- T7: HIBERN8
- T8: HIBERN8

M-RX state at M-RX pins:
- PWM b0, PWM b1
- T1: LCC-MODE
- T2: SAVE
- T7: HIBERN8
- T8: HIBERN8

M-CTRL-CFGREADY.confirm
- TX_Hibern8Time_Capability
- TX_Advanced_Hibern8Time_Capability
- RX_Hibern8Time_Capability
- RX_Advanced_Hibern8Time_Capability

SAVE
Initiator Config

1. PACP_RequestTimer expired?
   - Yes: PACP_PWR_cnf == PWR_BUSY?
     - Yes: Configure MODULEs (Initiator)
     - No: PACP_PWR_cnf == PWR_OK?
       - Yes: PACP_PWR_req received and accepted?
         - No: check 5.7.12.1.1 step 2) of [MIPI02]
         - Yes: Schedule Stop of Initiator process
       - No: PACP_PWR_req re-transmission possible?
         - Yes: attempt a PACP_PWR_req re-try
         - No: prepare for PA_LM_HIBERNATE_ENTER.ind (PWR_LOCAL)
           - Yes: Schedule an M-LANE-BurstEnd.request
           - No: Configure CONNECTED Modules (TX and RX) into HIBERN8
         - No: PACP_PWR_req received but rejected?
           - Yes: check 5.7.12.1.1
           - No: Prepare for PA_LM_HIBERNATE_ENTER.ind (PWR_FATAL_ERROR)
             - Yes: Schedule an M-LANE-BurstEnd.request
             - No: Configure temporarily ACTIVATED MODULEs (TX and RX) into HIBERN8.
   - No: Configure MODULEs (Initiator)

2. BURST after LINE-RESET?
   - Yes: PACP_PWR_req received and accepted?
     - No: Schedule Stop of Initiator process
     - Yes: Schedule an M-LANE-BurstEnd.request
   - No: PACP_PWR req re-transmission possible?
     - Yes: Schedule Stop of Initiator process
     - No: Configuring Modules (Initiator)
Peer Config

Configure Modules (responder)
PACP_PWR_req received!

Check 5.7.12.1.1 step 2) of [MIPI02]
Collision detected?

Yes

received PACP_PWR_req rejected based on DevID field check?

Yes

Schedule PACP_PWR cnf(PWR_BUSY)

abort responder process and continue concurrent initiator process

No

No

Schedule PACP_PWR cnf(PWR_OK)

schedule new configuration:
all CONNECTED RX and TX LANEs to enter Hibern8

Configure Modules (responder)
End