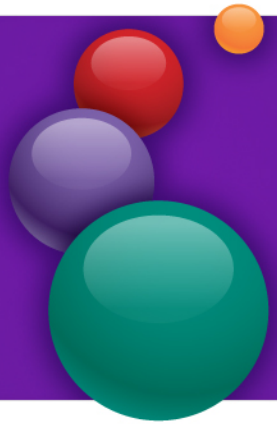
MIPI UniPort-M
Integrating the M-PORT into UniPro



Jürgen Urban
UniPro Working Group Chairman
11 Nov. 2015 – MIPI Member Webinar

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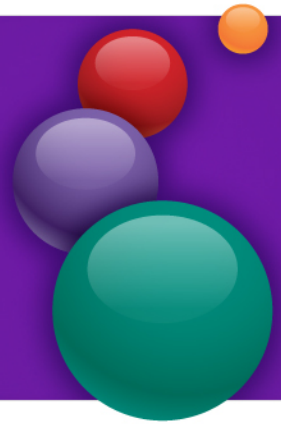
MIPI Alliance:
A Brief Introduction

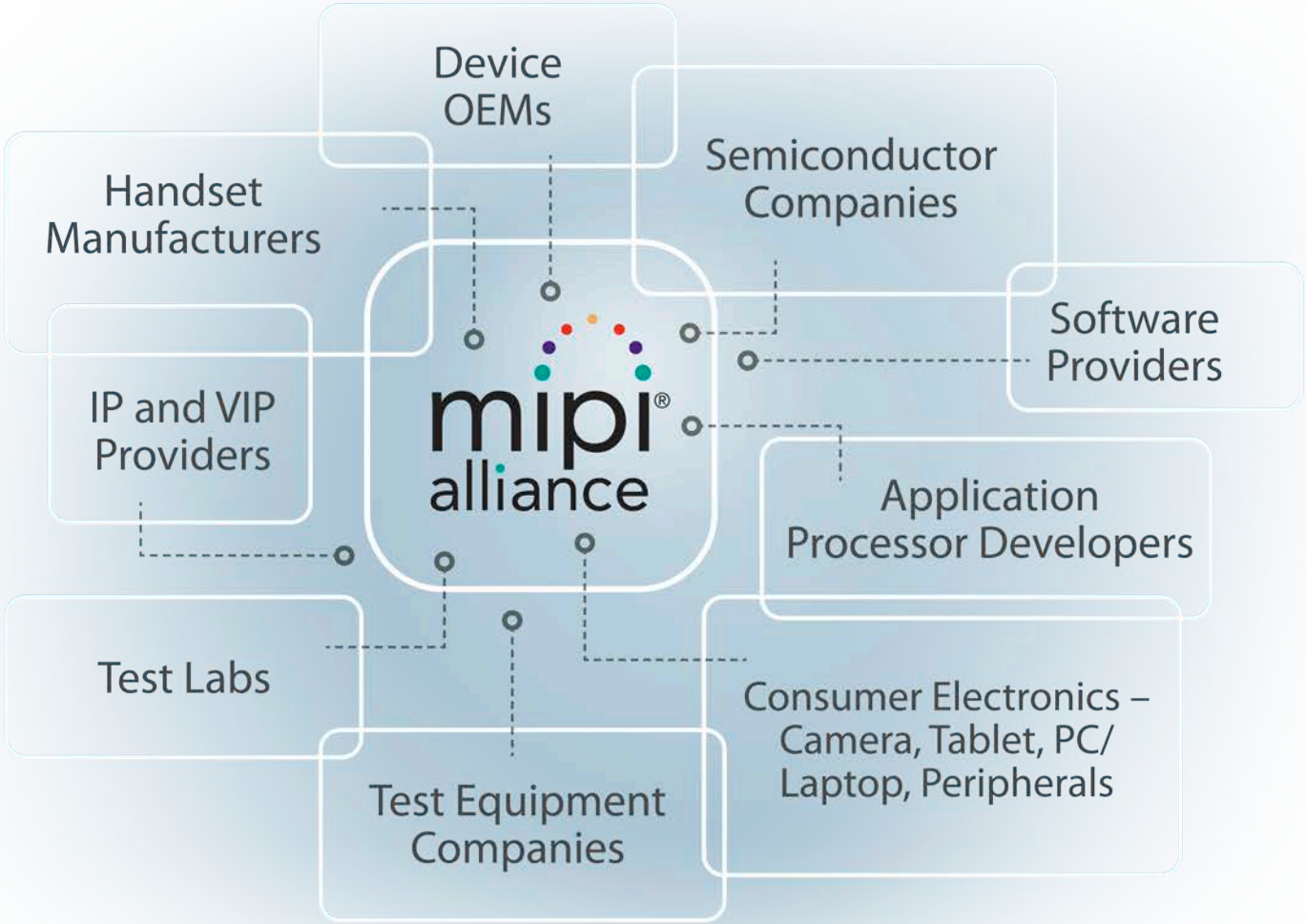


Peter B. Lefkin
Managing Director

About MIPI Alliance

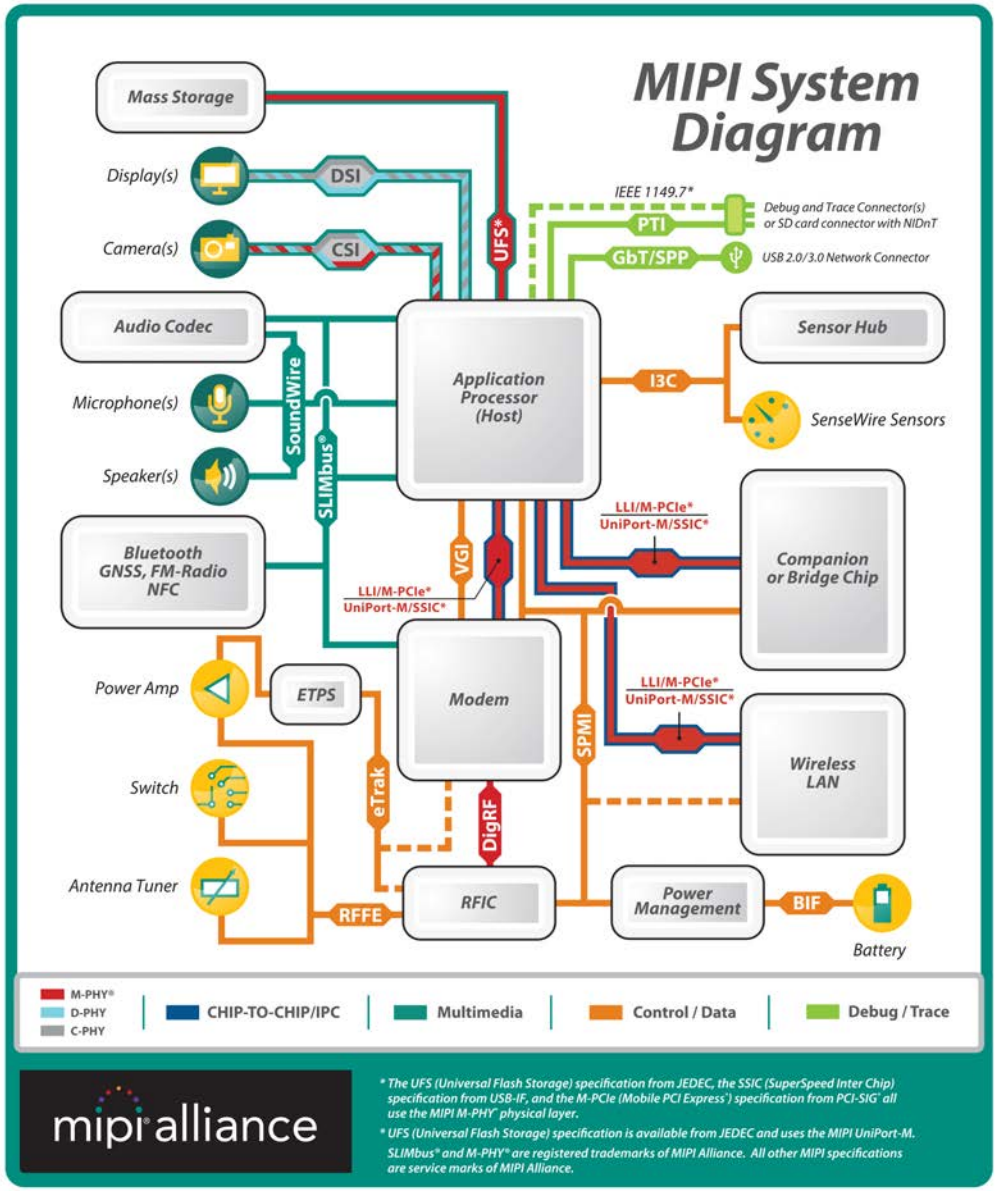
- 282 Members (as of 31 October 2015)
- 45+ specifications and supporting docs
- We drive **mobile** and **mobile-influenced interface** technology through the development of hardware and software **specifications**
- We work **globally** and **collaboratively** with other standards bodies to **benefit the mobile ecosystem**

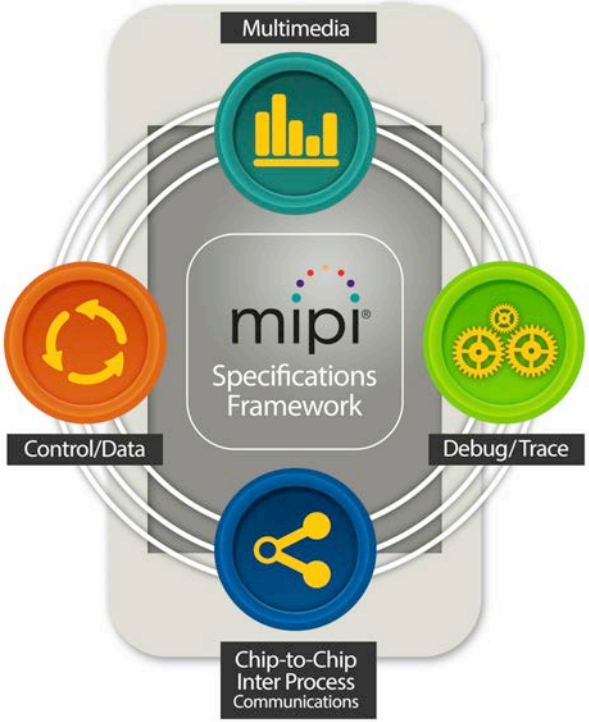
MIPI Alliance Member Ecosystem



Active MIPI Alliance Working Groups

- Camera
- Debug
- Display
- Low Latency Interface
- Low Speed Multipoint Link (New - SoundWire℠)
- Marketing
- PHY (C / D / M)
- Reduced Input Output (RIO) (New)
- Sensor / I3C℠ (New)
- Software (New)
- Technical Steering Group
- Test
- **UniPro℠**





Recent Announcements

- 29 October 2015 - MIPI Alliance Introduces a Family of MIPI Gigabit Debug Interface Specifications for Mobile and Mobile-Influenced Designs

- 12 August - MIPI Alliance Releases New MIPI M-PHY v4.0 Specification, Achieving a Peak Transmission Rate of Nearly 12 Gbps

The Future of MIPI – Beyond Mobile

- Mobile influences **everything**
- Everything gets faster, smaller and lower power
  - MIPI will continue to evolve specs to take advantage of the evolution of technology in mobile devices

11 Nov. 2015 - MIPI Member Webinar MIPI UniPort-M Integrating the M-PORT into UniPro

- Facilitator

  Peter Lefkin – Managing Director, MIPI Alliance

- Presenter

  Jürgen Urban – Chairman, MIPI UniPro Working Group

Contact

- Slide set available under:
  - Public site - http://mipi.org/learning-center/webinars
  - Members site open to all members - https://members.mipi.org/wg/Marketing/document/folder/5737
- In case of further questions/feedback:
  - UniPro-questions@mipi.org (Adopters)
  - bugzilla@mipi.org (Contributors)

Agenda

- Definitions and Conventions
- M-PHY SAP mapping to RMMI
- Intra LANE timings
- UniPort_M intra SUB-LINK timings
- UniPort_M LINK timings
- Q&A

DEFINITIONS AND CONVENTIONS

Disclaimer

- This Webinar lays out the UniPro WG perspective on M-PHY integration
  - Other protocols using M-PHY may look at a different angle towards M-PHY integration
  - Discussion baseline: UniPro v1.6x + M-PHY v3.x
- This Webinar discusses implementations
  - It does not claim or intend to deliver universal implementation truths
  - Other solutions/interpretations conformant with both, M-PHY and UniPro specification may rightfully exist
  - In case of contradictions/ambiguities the spec prevails

LANE Categorization

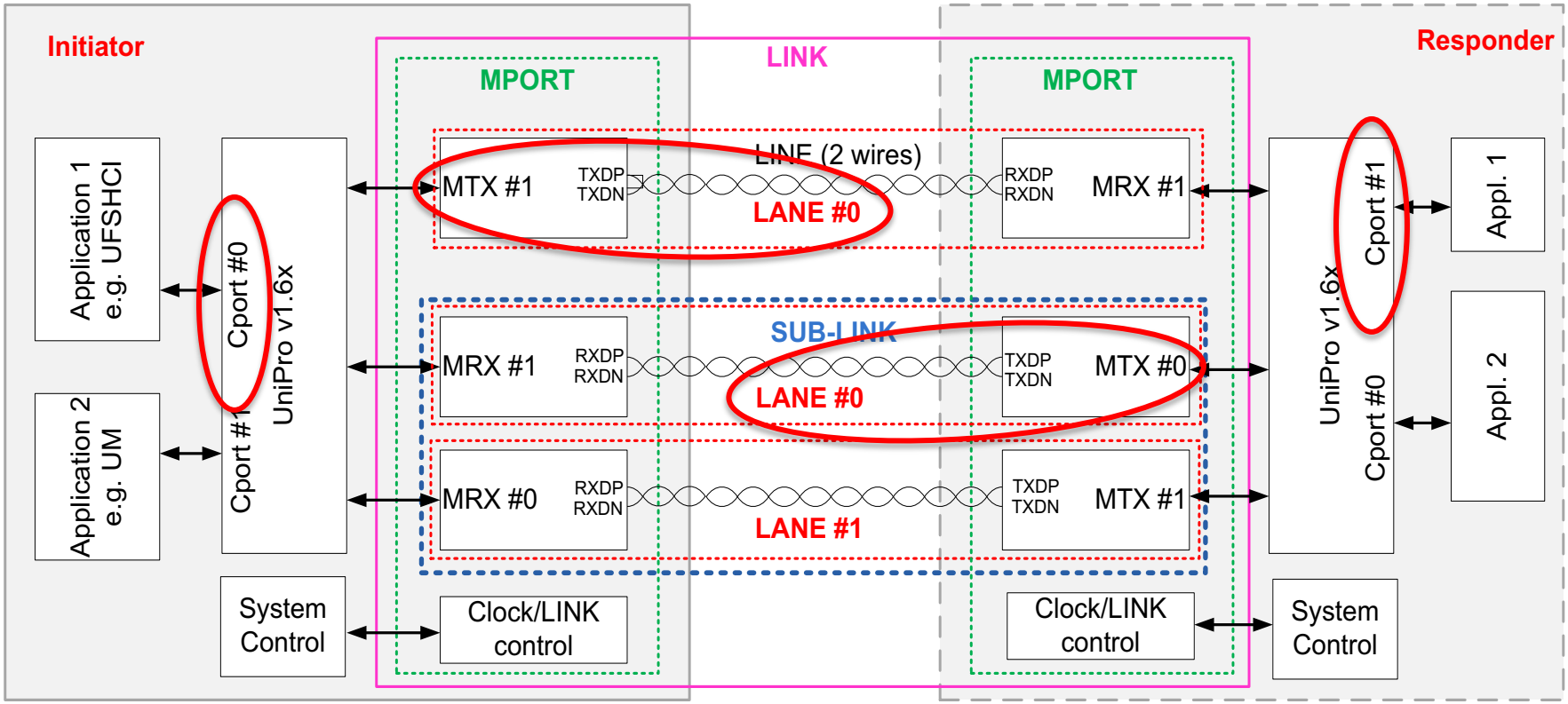
	physical implementation	LSS	Connection state after LSS	Lane state after LSS	M-PHY state	Comment
Data Lane	physical Lane	LINK STARTUP	logical Lane			
	unavailable Lane		N/A	N/A	N/A	PHY is physically not implemented, DME or PACP access results in BAD_INDEX Error
	available Lane Count in PA_AvailTxDataLanes and PA_AvailRxDataLanes		unconnected Lane	off (Off_Mode)	unpowered	PHY is physically implemented and can be accessed during LINKDOWN and LSS. UniPro fails to establish a peer connection during LSS. When in OFF_STATE, the response to DME or PACP access is undefined in v1.61, suggestion to use BAD_INDEX
			connected Lane Count in PA_ConnectedTxDataLanes and PA_ConnectedRxDataLanes	inactive/unused (Hibernate_Mode)	HIBERN8	no count in PA_ActiveTxDataLanes or PA_ActiveRxDataLanes
				inactive, unused Lane, dummy burst (LinkCfg)	ACTIVATED, LINE-RESET, (LINE-CONFIG)	no de-skew symbol, skip patterns, scrambling, dummy payload, no count in PA_ActiveTxDataLanes or PA_ActiveRxDataLanes
				active/used Lane (FastMode, SlowMode, FastAuto_Mode, SlowAuto_Mode, Hibernate_Mode). Count in PA_ActiveTxDataLanes and PA_ActiveRxDataLanes	ACTIVATED, HIBERN8	de-skew symbol, data traffic, skip patterns, scrambling.

Red Text: Terminology used in UniPro v1.6x
Blue Text: Terminology used in M-PHY v3.x

Dummy BURST

- Dummy Bursts are used during PACP_PWR_req traffic to configure inactive Lanes in synchronization with potentially attached Media Converters
  - During PACP_PWR_req a BURST or a dummy BURST is started on all connected LANEs
  - The peer M-RX ignores Dummy BURSTs
  - Dummy Bursts are not part of the MK0, MK1 Lane deskew.
  - Dummy Bursts, however, follow entirely the M-PHY spec (they require prepare/sync period, MK0 and TOB)
  - Dummy Bursts are scrambled, if requested

LINK Terminology



We use the Link terminology found in M-PHY spec.
Note: The UniPro spec does not know SUB-LINKs, they are called LINK there.

Logical Lane versus physical Lane

- Logical Lane numbering does typically not match w/ physical Lane numbering
  - M-PORT clocking is primarily driven by state of logical LANE #0
  - M-PORT needs to know LANE mapping from UniPro to derive the necessary M-PHY clocking
- Alternatively:
  - Application may restrict arbitrary PCB routing
  - Logical Lane is always identical to physical Lane

LINECFG

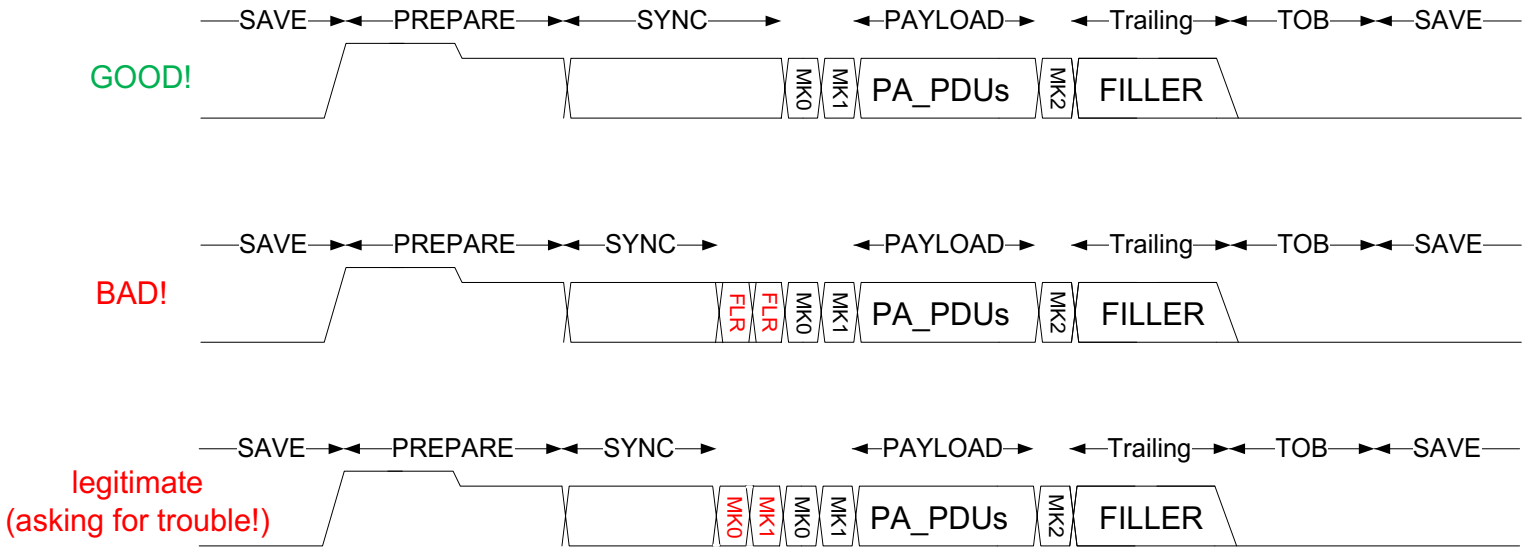
- LINE-CFG is used for Media Converters
- UniPro v1.41:
  - M-PHY LINECFG implementation and use is mandated
- UniPro v1.6x:
  - M-PHY LINECFG implementation is mandated (for backward compatibility w/ v1.41)
  - M-PHY LINECFG use is not mandated, left to the application to decide.
  - M-RX must be able to tolerate a LINECFG sequence, i.e. re-sync to SLEEP/STALL at DIF-N
  - If PA_Local_TX_LCC_Enable=0, there is no expectation that the M-TX ever emits LINECFG.

M-PHY SAP MAPPING TO RMMI

M-TX DATA SAP and RMMI

M-PHY SAP		RMMI Mapping	Reference clocking	Comment
M-LANE-SYMBOL	request	TX_ProtDORDY; TX_Symbol ; TX_DataNCtrl	TX_SymbolClk	The UniPro stack should issue changes to TX_ProtDORDY on the same clock cycle for all active Lanes in a multi-LANE LINK. Failing to synchronize TX_ProtDORDY leads to errors in the PA_PDU lane distribution and merging
M-LANE-SYMBOL	confirm	TX_ProtDORDY && TX_PhyDIRDY	TX_SymbolClk	TX_PhyDIRDY signals only readyness of the M-TX to receive data from the stack. Only in conjunction with TX_ProtDORDY the UniPro stack interprets a confirm and advances to the next Symbol data. In a multi-LANE LINK, the UniPro stack must receive (TX_ProtDORDY && TX_PhyDIRDY) on all M-TX LANES at the same time for not breaking the PA_PDU Lane distribution
M-LANE-PREPARE	request	rising edge (TX_Burst)	TX_SymbolClk	
M-LANE-PREPARE	confirm	rising edge (TX_SaveState_Status_N) after rising edge (TX_Burst)	TX_SymbolClk	
M-LANE-SYNC	request	unused in UniPro		UniPro uses the M-TX generated default SYNC pattern
M-LANE-SYNC	confirm	unused in UniPro		UniPro uses the M-TX generated default SYNC pattern
M-LANE-BurstEnd	request	falling edge (TX_Burst)	TX_SymbolClk	
M-LANE-BurstEnd	confirm	no mapping in RMMI	TX_SymbolClk	M-LANE-BurstEnd.confirm cannot be represented using TX_SaveState_Status_N as entry into LINE-CFG seperates the two events. It cannot be represented as a function of the falling edge of TX_Burst, as the M-PHY adds BurstClosure extension in PWM traffic.
M-LANE-SaveState	indication	falling edge (TX_SaveState_Status_N)	TX_SymbolClk	There is no direct mapping into RMMI. M-LANE-SaveState.indication indicates entry into SLEEP or into STALL state but does not indicate entry into HIBERN8. TX_SaveState_Status_N is a level sensitive signal indicating also also a HIBERN8 state.

M-TX SYMBOL RMMI mapping



RMMI

31 e.g. PA_PDU #2 PA_PDU #0 0

TX_Symbol[31:0]	MARKER1	MARKER0	FILLER	FILLER
TX_ProtDORDY[3:0]	1	1	0	0

M-TX needs to transform this into SYNC!

M-RX DATA SAP and RMMI

M-PHY SAP		RMMI Mapping	Reference clocking	Comment
M-LANE-SYMBOL	indication	RX_Symbol; RX_SymbolErr; RX_DataNCtrl; RX_PhyDORDY;	RX_SymbolClk	
M-LANE-PREPARE	indication	rising edge (RX_Burst)	RX_SymbolClk	rising edge means synchronous edge detection
M-LANE-BurstEnd	indication	falling edge (RX_Burst)	RX_SymbolClk	falling edge means synchronous edge detection
M-LANE-HIBERN8Exit	indication	rising edge (RX_Hibern8Exit_Type_I)	Async	At the time of exit from HIBERN8, there is typically no RX_SymbolClk available. The asynchronous signal may be used to switch on RX_SymbolClk at system level. The UniPro protocol may then use a sampled version of this RMMI signal
M-LANE-MRXSaveState	indication	No representation in the RX_SymbolClk domain, fallback solution: falling edge (RX_CfgRdyN) after falling edge (RX_Burst)	RX_CfgClk	There is no corresponding representation of this M-RX Data SAP in RMMI. The end of a BURST indicated by M-LANE-BurstEnd.indication may differ substantially from M-LANE-SaveState.indication in case of running through LINE-CFG or in case of a long PWM Tail-of-Burst. It is assumed the M-RX keeps RX_CfgRdyN high during TOB and LINE-CFG and asserts it to low only, when entrering SAVE state

M-TX CTRL SAP and RMMI

M-PHY SAP		RMMI Mapping	Reference clocking	Comment
M-CTRL-CFGGET	request	~TX_AttrWRn && TX_CfgEnbl	TX_CfgClk	
M-CTRL-CFGGET	confirm	if (TX_Burst==0): first cycle of (TX_CfgRdyN==0) after TX_CfgEnbl if (TX_Burst==1): N/A	TX_CfgClk	There is no mandate for an M-Phy to implement TX_CfgRdyN = High after M-CTRL-CFGGET.request
M-CTRL-CFGSET	request	TX_AttrWRn && TX_CfgEnbl	TX_CfgClk	
M-CTRL-CFGSET	confirm	if (TX_Burst==0): first cycle of (TX_CfgRdyN==0) after TX_CfgEnbl if (TX_Burst==1): N/A	TX_CfgClk	There is no mandate for an M-Phy to implement TX_CfgRdyN = High after M-CTRL-CFGSET.request
M-CTRL-CFGREADY	request	TX_CfgUpdt	TX_CfgClk	Usually only during TX_BURST==1, exception: TX_HIBERN8_Control
M-CTRL-CFGREADY	confirm	first cycle of (TX_CfgRdyN==0) after M-CTRL-CFGREADY.request	TX_CfgClk	During BURST, TX_CfgRdyN is always high. The confirm is postponed until after the M-TX enters SAVE state and executes RCT.
M-CTRL-RESET	request	TX_Reset	TX_CfgClk	
M-CTRL-RESET	confirm	falling edge (TX_CfgRdyN) after TX_Reset	TX_CfgClk	falling edge means synchronous edge detection
M-CTRL-LINERESET	request	TX_LineReset	TX_CfgClk	
M-CTRL-LINERESET	confirm	falling edge (TX_CfgRdyN) after TX_LineReset	TX_CfgClk	falling edge means synchronous edge detection
N/A		TX_InLnCfg (unused, legacy)	TX_CfgClk	No M-TX CTRL SAP representation exists for this RMMI signal. UniPro does not use this signal, the corresponding M-PHY input should be clamped to appropriate values.
N/A		TX_DIFNDrive (optional)	TX_CfgClk	No M-TX CTRL SAP representation exists for this RMMI signal. However, UniPro needs to control this signal, if the M-TX transmitter can drive a weak DIF-N with R_{SE_PO} termination
N/A		TX_Controlled_ActTimer (unused)	constant 0	No M-TX CTRL SAP representation exists for this RMMI signal. UniPro does not use this signal, the corresponding M-PHY input should be set to 0.

M-RX CTRL SAP and RMMI

M-PHY SAP		RMMI Mapping	Reference clocking	Comment
M-CTRL-CFGGET	request	~RX_AttrWRn && RX_CfgEnbl	RX_CfgClk	
M-CTRL-CFGGET	confirm	if (RX_Burst==0): first cycle of (RX_CfgRdyN==0) after M-CTRL-CFGGET.request if (RX_Burst==1): N/A	RX_CfgClk	There is no mandate for the M-PHY to de-assert (High Level) RX_CfgRdyN after an M-CTRL-CFGGET.request.
		RX_AttrRdCnf (optional)	RX_CfgClk	
M-CTRL-CFGSET	request	RX_AttrWRn && RX_CfgEnbl	RX_CfgClk	

M-CTRL-CFGSET	confirm	if (RX_Burst==0):
		first cycle of (RX_CfgRdyN==0) after M-CTRL-CFGSET.request
		if (RX_Burst==1): N/A
			RX_CfgClk	There is no mandate for the M-PHY to de-assert (High Level) RX_CfgRdyN after an M-CTRL-CFGSET.request.

M-CTRL-CFGREADY	request	RX_CfgUpdt	RX_CfgClk	
M-CTRL-CFGREADY	confirm	first cycle of (RX_CfgRdyN==0) after M-CTRL-CFGREADY.request	RX_CfgClk	During BURST, RX_CfgRdyN is always high, the confirm is postponed until after the M-RX enters SAVE state and executes RCT
M-CTRL-RESET	request	RX_Reset	RX_CfgClk	
M-CTRL-RESET	confirm	falling edge (RX_CfgRdyN) after falling edge (RX_RESET)	RX_CfgClk	
M-CTRL-LINERESET	indication	falling edge(RX_CfgRdyN) after falling edge(RX_LineReset)	RX_CfgClk	
N/A		RX_InLnCfg	constant	No SAP representation for this optional RMMI signal. UniPro does not use this signal
M-CTRL-LCCReadStatus	indication	RX_LCCRdDet	RX_CfgClk	Exists only, if LINE-CFG is implemented

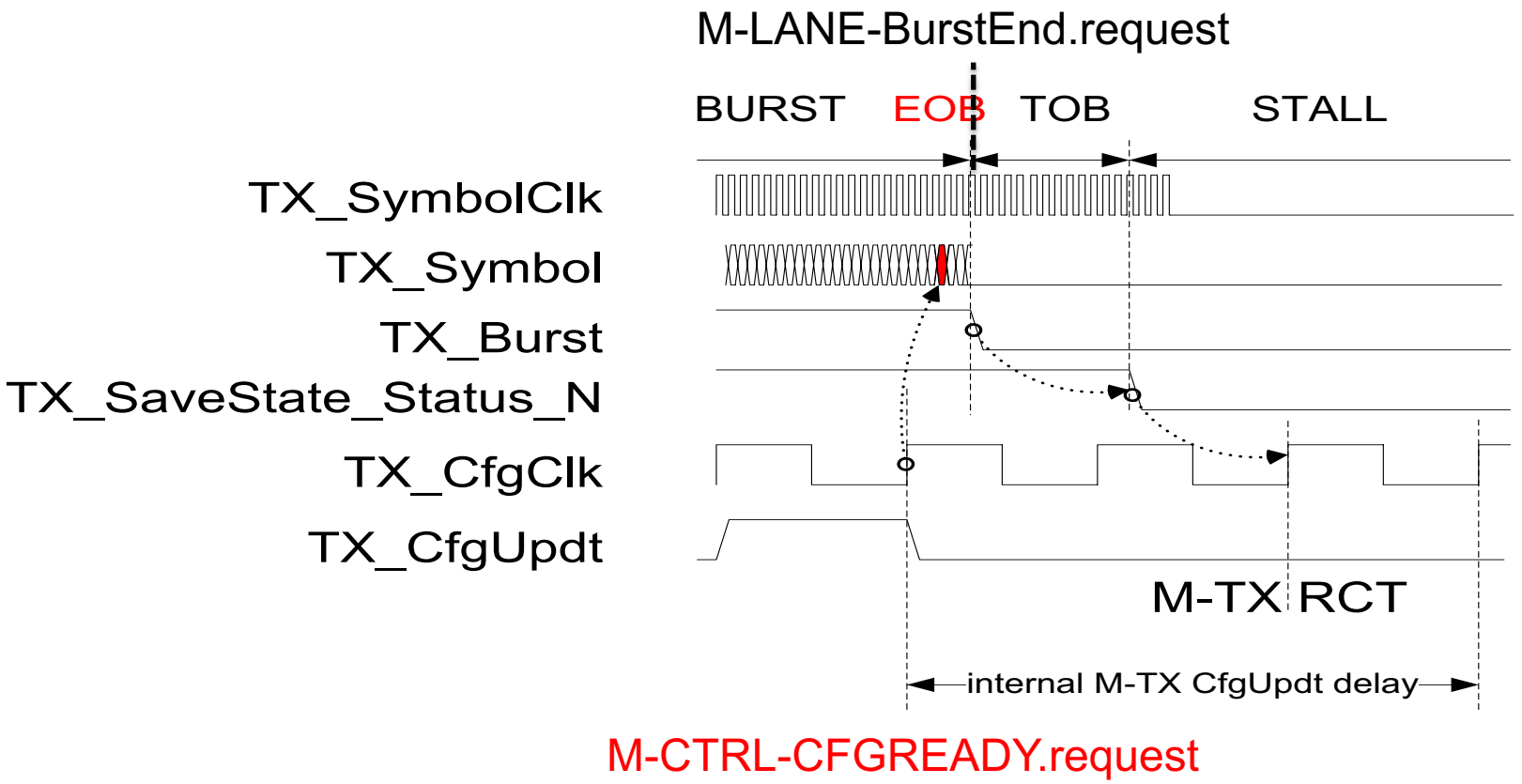
UniPro Configuration of M-PORT

- PA Layer:
  - M-PHY attributes requiring synchronization between local and peer are changed under PA Layer control
  - Only during an open BURST
    - Exception: Configuring the exit from HIBERN8
  - UniPro Protocol ensures that TX BURST and RX BURST stay open during configuration.
- Application:
  - M-PHY attributes requiring no synchronization
  - Configuration at any time
  - M-CTRL-CFGREADY.request must be generated by a DME_POWERMODE.req

UniPro Configuration sequence of M-TX during BURST

- M-LANE-PREPARE.request
  - M-LANE-PREPARE.confirm
- M-LANE-SYMBOL.request (MK0,CTRL)
  - M-LANE-SYMBOL.confirm
- Multiple M-CTRL-CFGSET.request
  - No M-CTRL-CFGSET.confirm (!)
- Single M-CTRL-CFGREADY.request
- M-LANE-SYMBOL.request (MK2, CTRL)
  - M-LANE-SYMBOL.confirm
- M-LANE-BurstEnd.request
  - M-LANE-BurstEnd.confirm
  - RCT
  - M-CTRL-CFGREADY.confirm

Potential Pitfall: race condition between M-TX DATA and M-TX CTRL SAP



UniPro Configuration sequence of M-RX during BURST

- M-LANE-PREPARE.indication
- M-LANE-SYMBOL.indication (MK0,CTRL)

– Multiple M-CTRL-CFGSET.request
  - No M-CTRL-CFGSET.confirm (!)

– Single M-CTRL-CFGREADY.request

– M-LANE-SYMBOL.request (MK2, CTRL)
  - M-LANE-SYMBOL.confirm

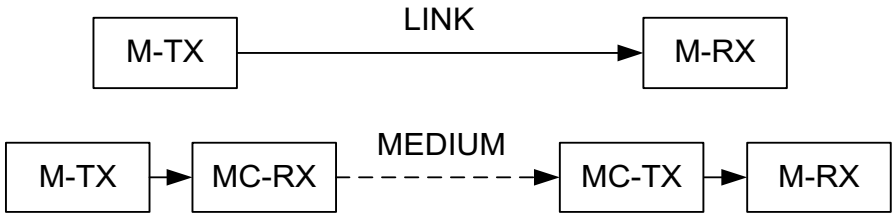
– M-LANE-BurstEnd.request
  - M-LANE-SYMBOL.indication (MK2, CTRL)
  - M-LANE-BurstEnd.indication
  - RCT
  - M-CTRL-CFGREADY.confirm

M-TX

INTRA LANE TIMINGS

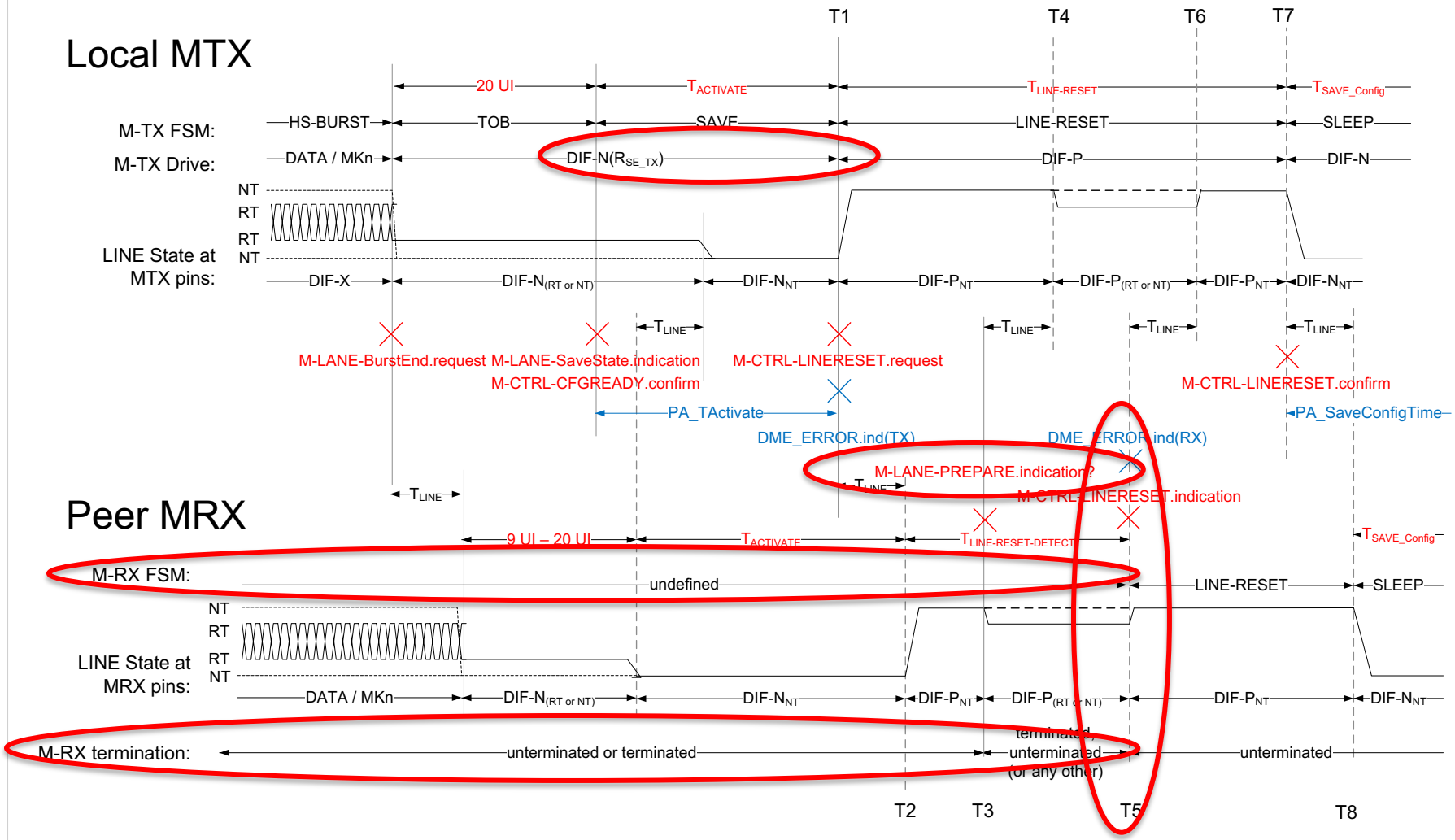
Intra Lane setup

- In the following diagrams, one complete LANE is shown, local M-TX to peer M-RX

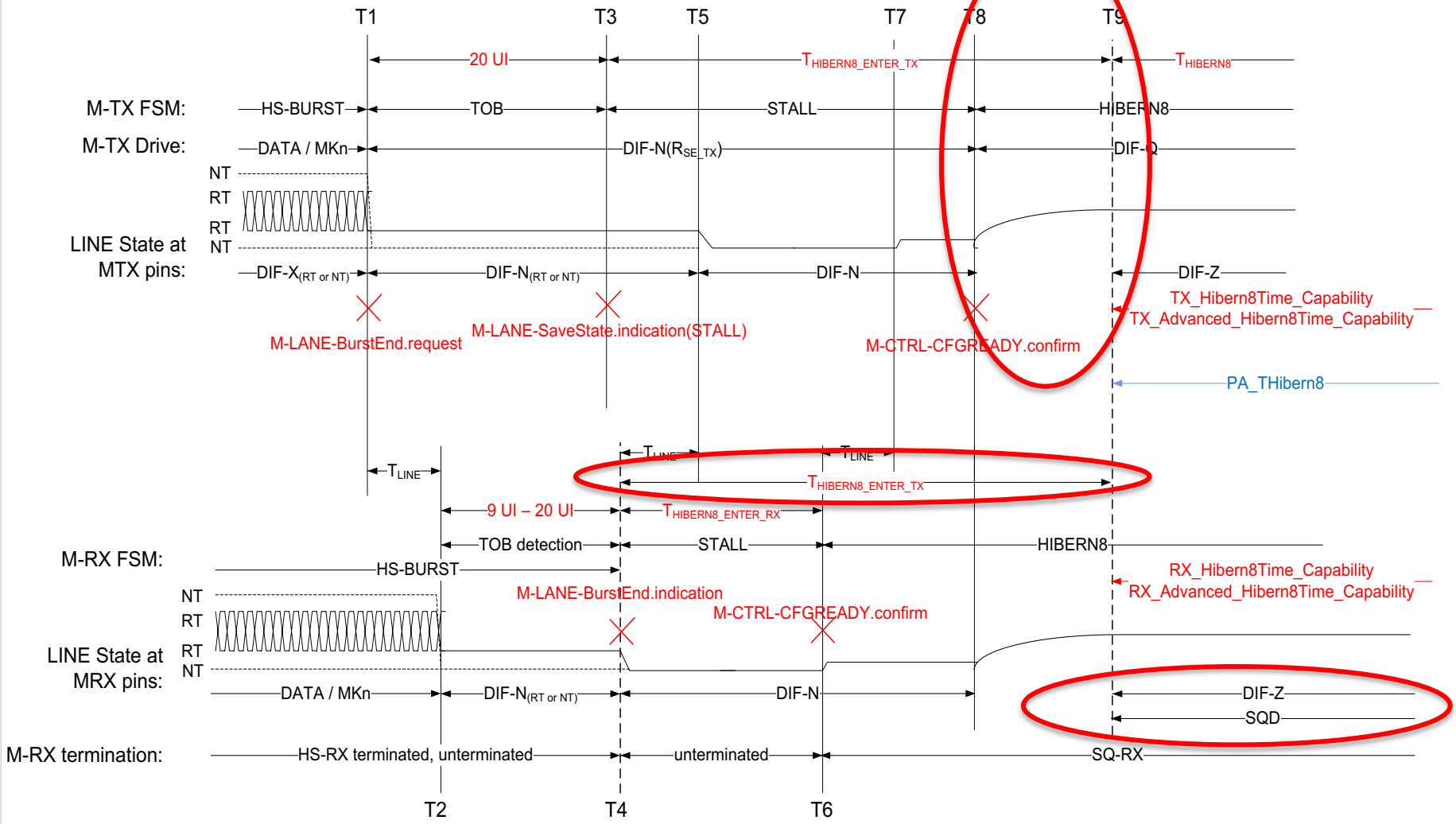


- Only the most critical timings are shown
- SAP timings are ideal!
  - SAP.indication are signalled delayed on RMMI
  - SAP.confirm are signalled delayed on RMMI
  - SAP.request cause delayed responses inside M-PHY

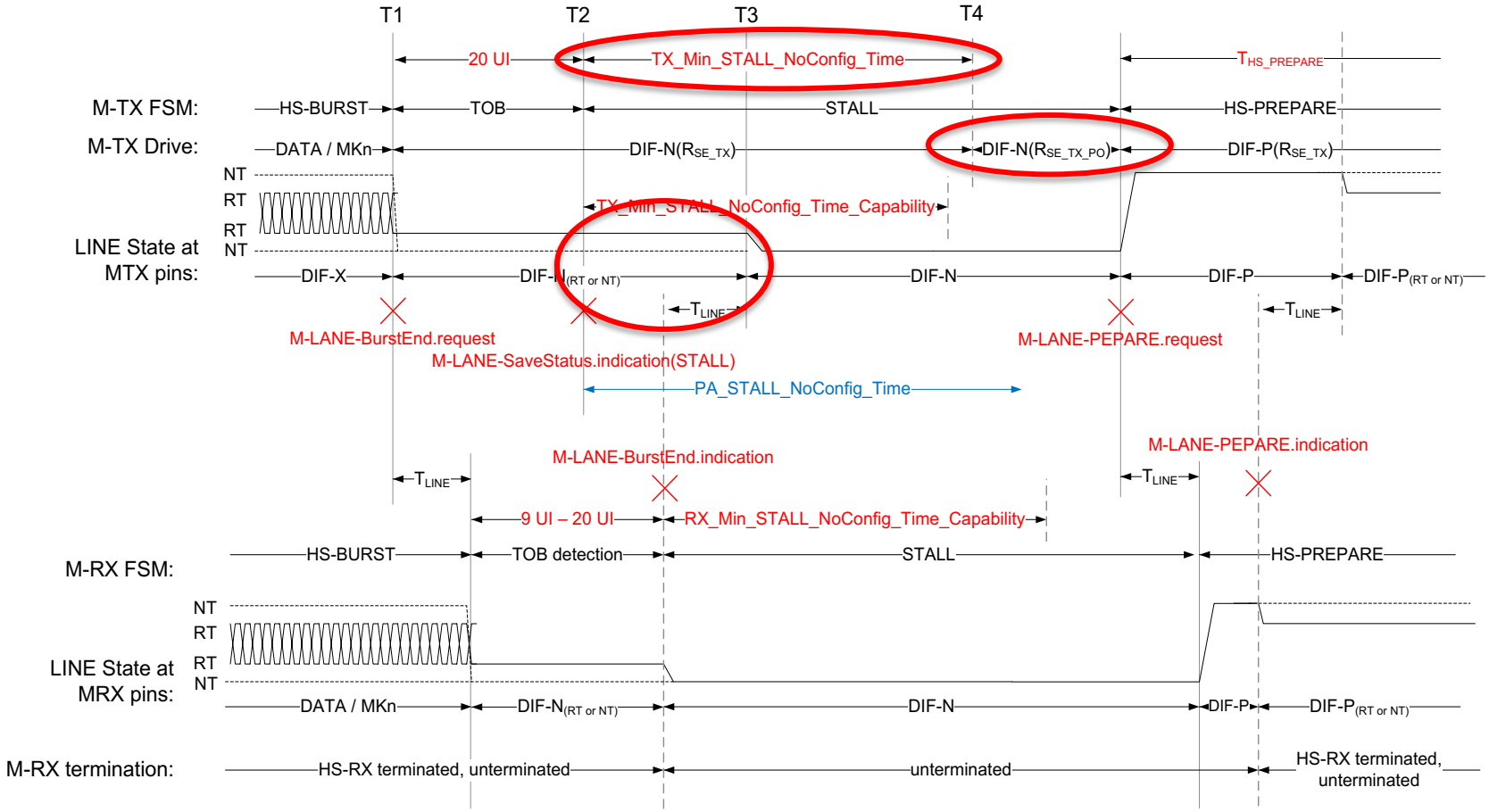
HS-BURST to LINE-RESET



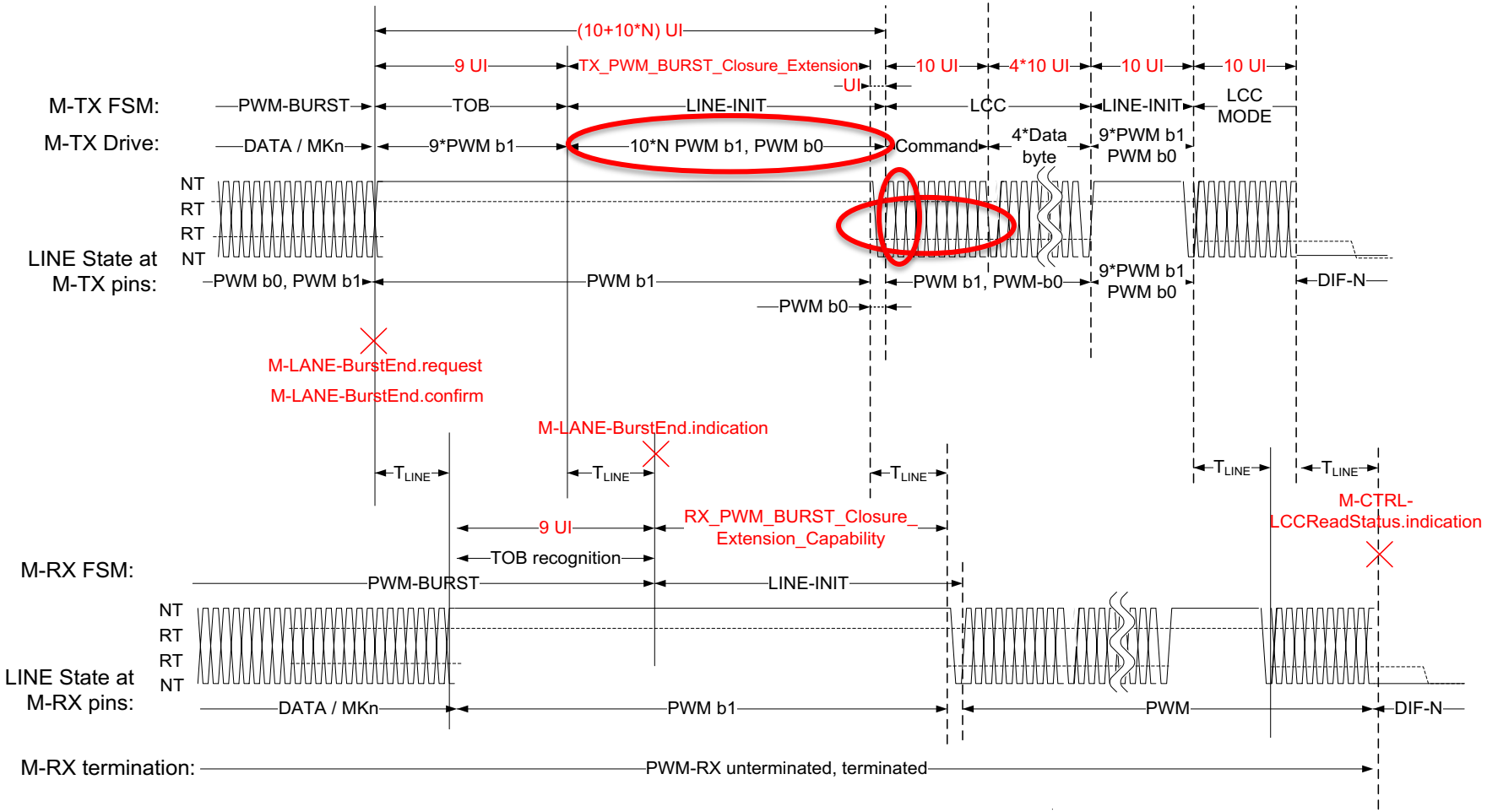
HS-BURST to HIBERN8



HS-BURST to STALL, no Config

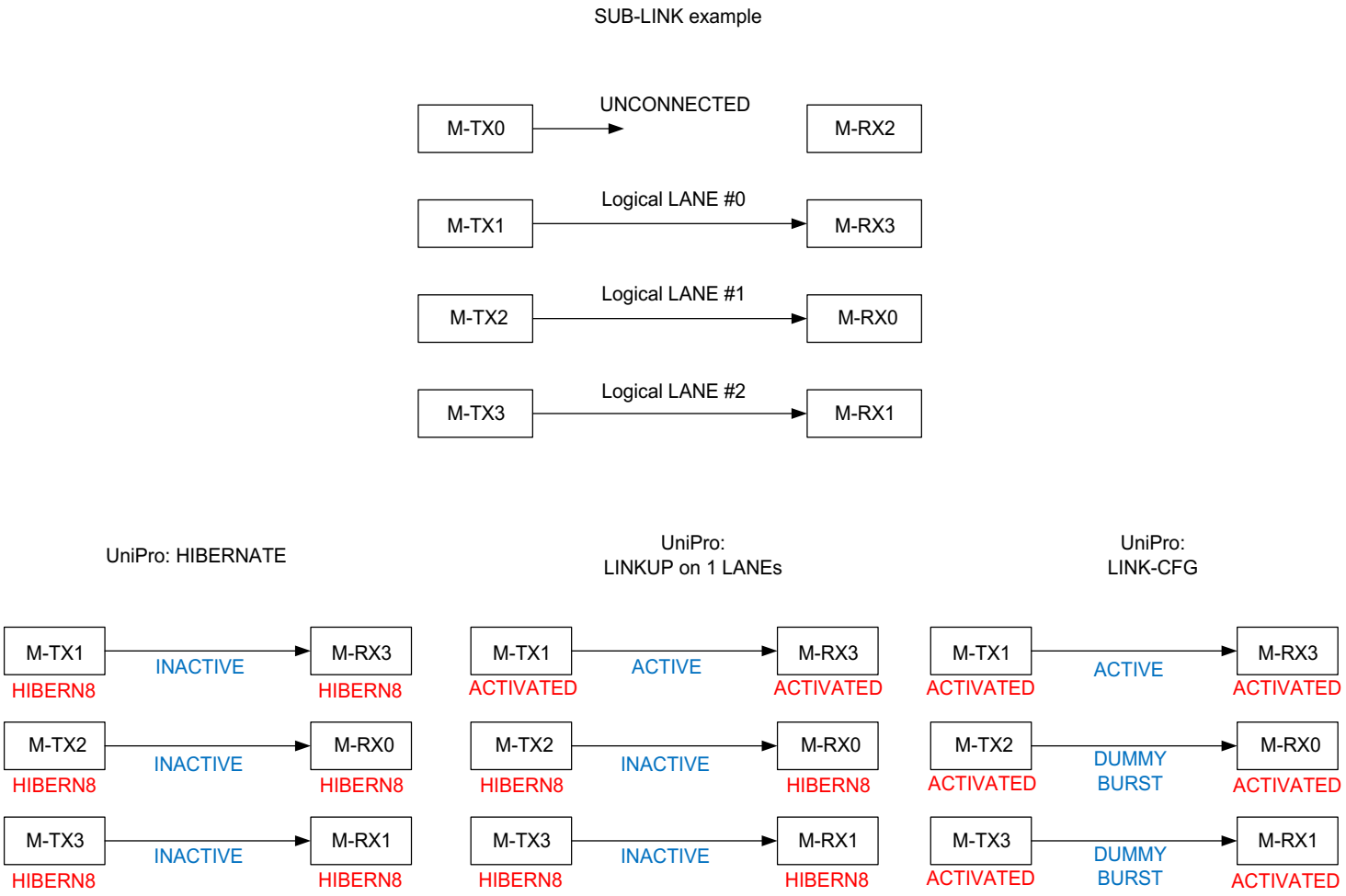


PWM-BURST to LINECFG



UNIPORT-M
INTRA SUB-LINK TIMINGS

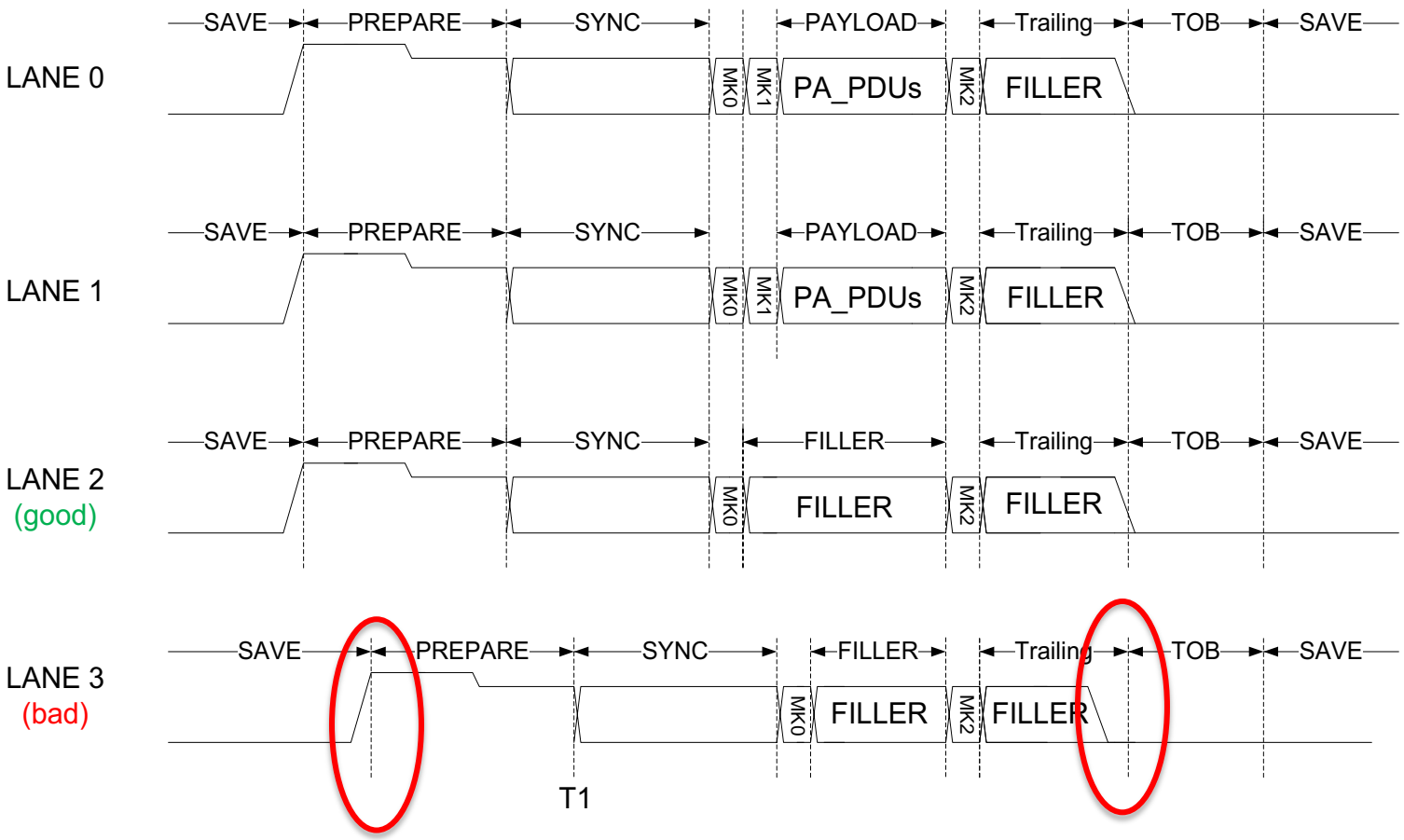
SUB-LINK connection example



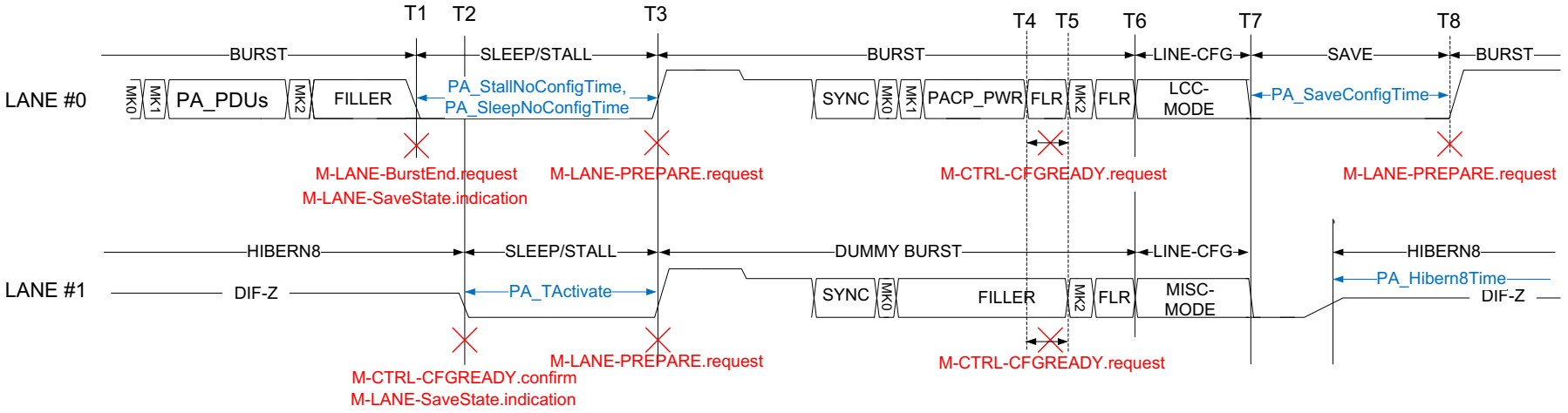
SUB-LINK management

- M-PHY attributes of all Lanes should be kept consistent at all times
  - May want to combine the attribute banks of all Lanes in a SUB-LINK
  - M-TX-CTRL SAP may be shared for SUB-LINK
  - M-RX-CTRL SAP may be shared for SUB-LINK
- Exception:
  - TX_DRIVER_POLARITY
  - TX_HIBERN8_Control
  - TX_HS_Equalizer_Settings
  - RX_Enter_HIBERN8

Lane Alignment

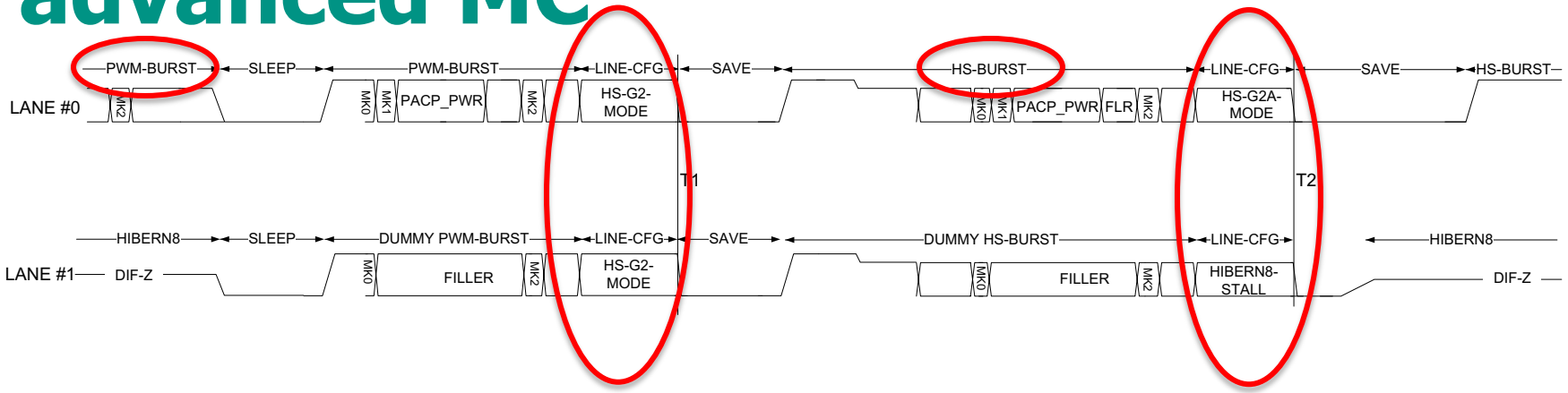


Powermode change w/ dummy BURST



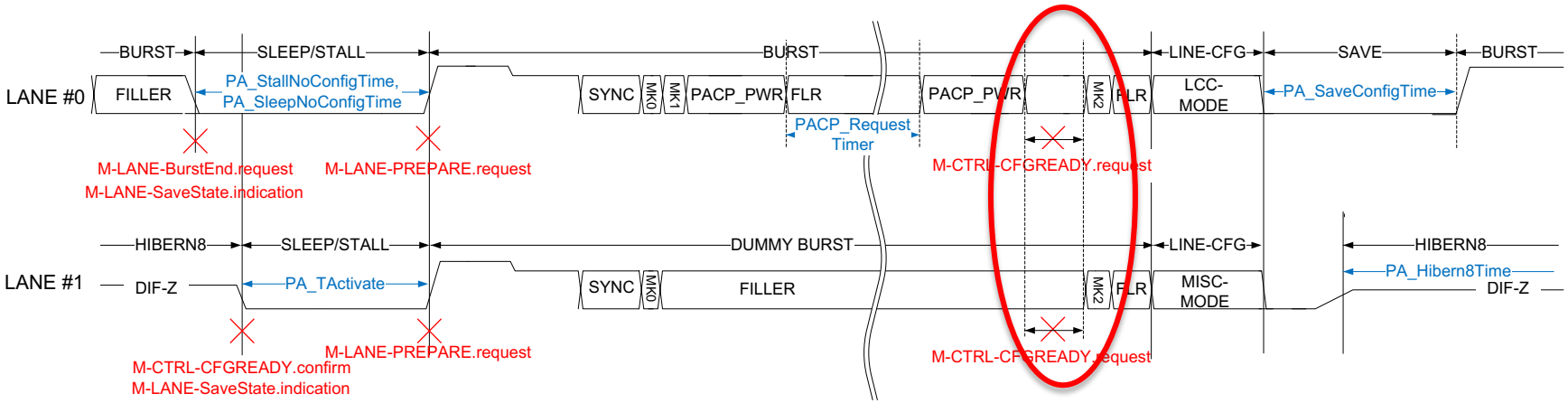
- Same waveform for PACP_PWR_req and PACP_PWR_cnf
- Signal integrity:
  - LANE #1 enters/exits HIBERN8, when LANE #0 is in SAVE state
  - BURST and DUMMY BURST start and stop at same time
- LCC-MODE can either enter HIBERN8 or change Powermode, but not both at the same time

Powermode change w/ advanced MC



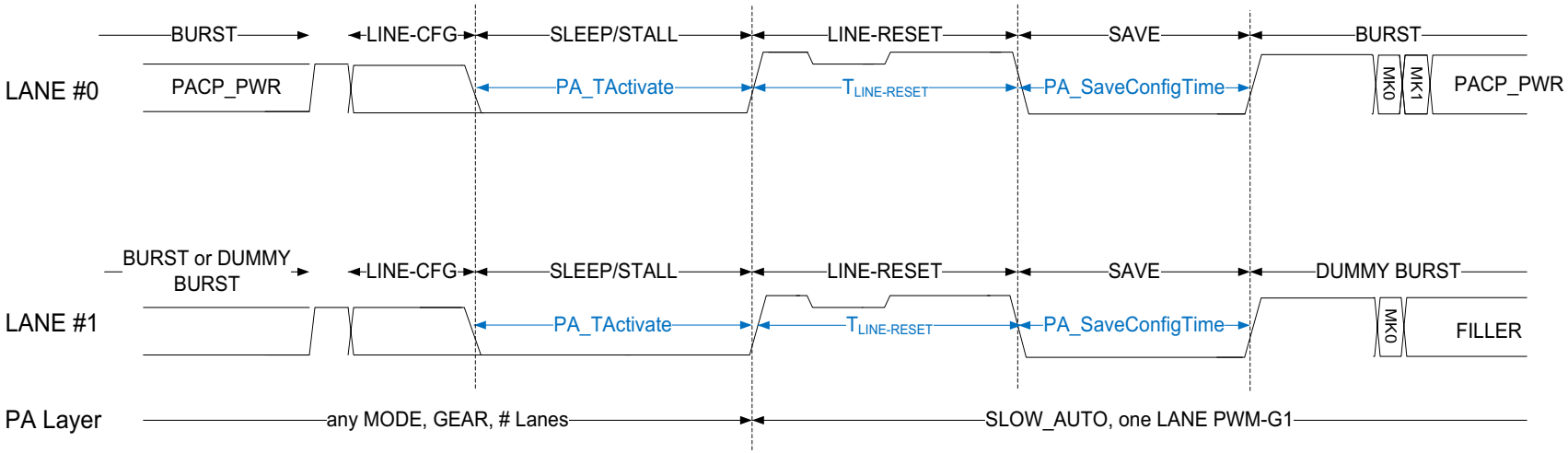
- Need two Powermode changes in a row:
  - 1st change activates all connected LANEs into desired GEAR and MODE
  - 2nd change de-activates unused LANEs into HIBERN8

PACP_PWR_req with retry



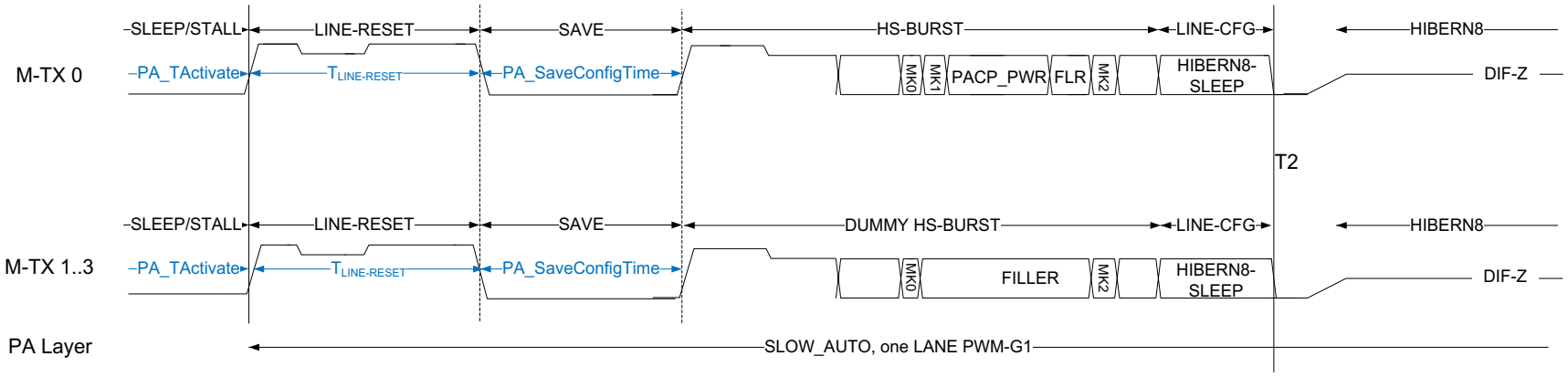
- PACP_PWR_cnf (PWR_OK) only after second PACP_PWR_req
- During PACP_retry, the BURST must be kept open
- M-TX is configured only once even with retry

LINE-RESET in LINKUP after unsuccessful PACP_PWR_req



- Before LINE-RESET, all LANEs are either ACTIVATED or run a DUMMY BURST, no need to wake up from HIBERN8
- After LINE-RESET, LANE #0 is ACTIVATED in PWM-G1, all other LANEs run Dummy BURST in PWM-G1

Entry into HIBERN8 after LINE-RESET



- LINE-RESET sends LINK into PWM-G1
- After exit from HIBERN8 the LINK is still in that MODE and GEAR and Application needs to re-program into desired GEAR
  - Check consequences for Application Auto Hibernate!

Scrambling in HS-MODE

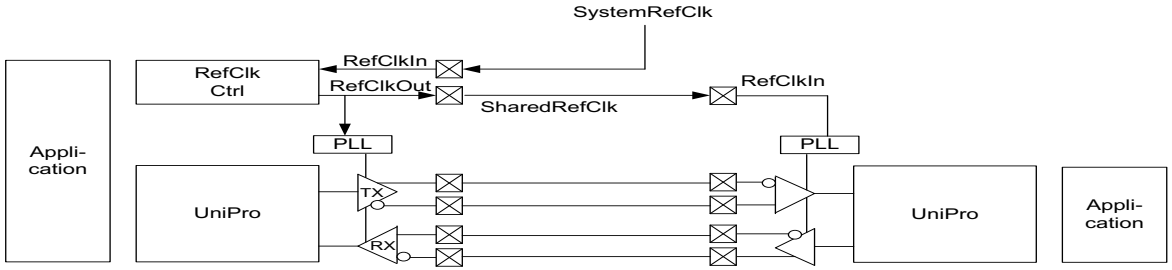
- Scrambling is difficult to debug
  - Test equipment re-synchronizes scrambler on a SYNC symbol (MK0, MK1)
  - UniPro implementation should be able to insert periodical (MK0, MK1) for debug purposes
    - Via DME_POWERMODE.req(unchanged, unchanged)
    - Via any other implementation specific mechanism
- Scrambling should include FLR sequence after MK2

UNIPORT-M LINK

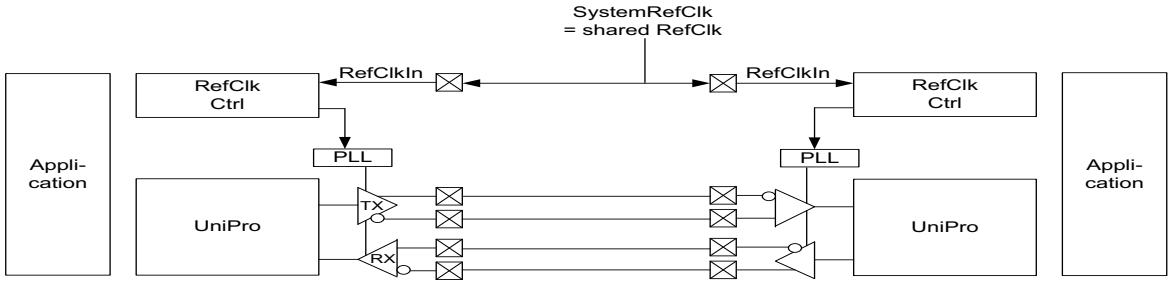
Shared RefClk

- UniPort_M does not define the frequency of the Shared RefClk
  - Application should do!
- Application may program RefClk frequency into peer before changing to HS-MODE
- M-PHY architectures requiring a shared reference clock need
  - RX_REF_CLOCK_SHARED_Capability=1 or/and
  - TX_REF_CLOCK_SHARED_Capability=1

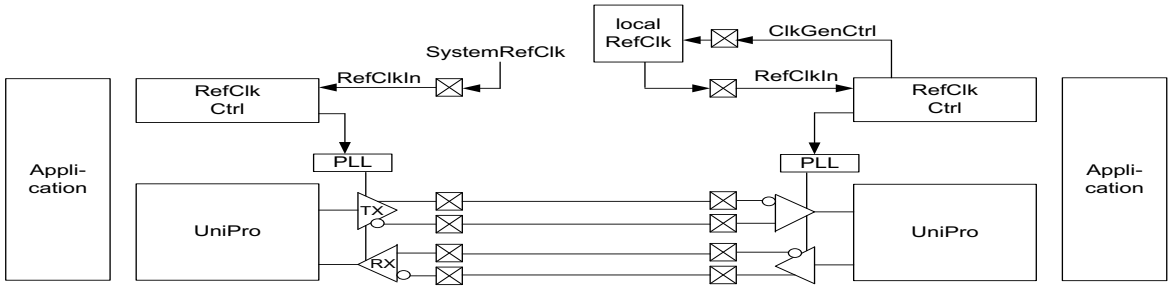
Clocking concepts, examples



a) Host Controlled Shared RefClk



b) System Generated Shared RefClk

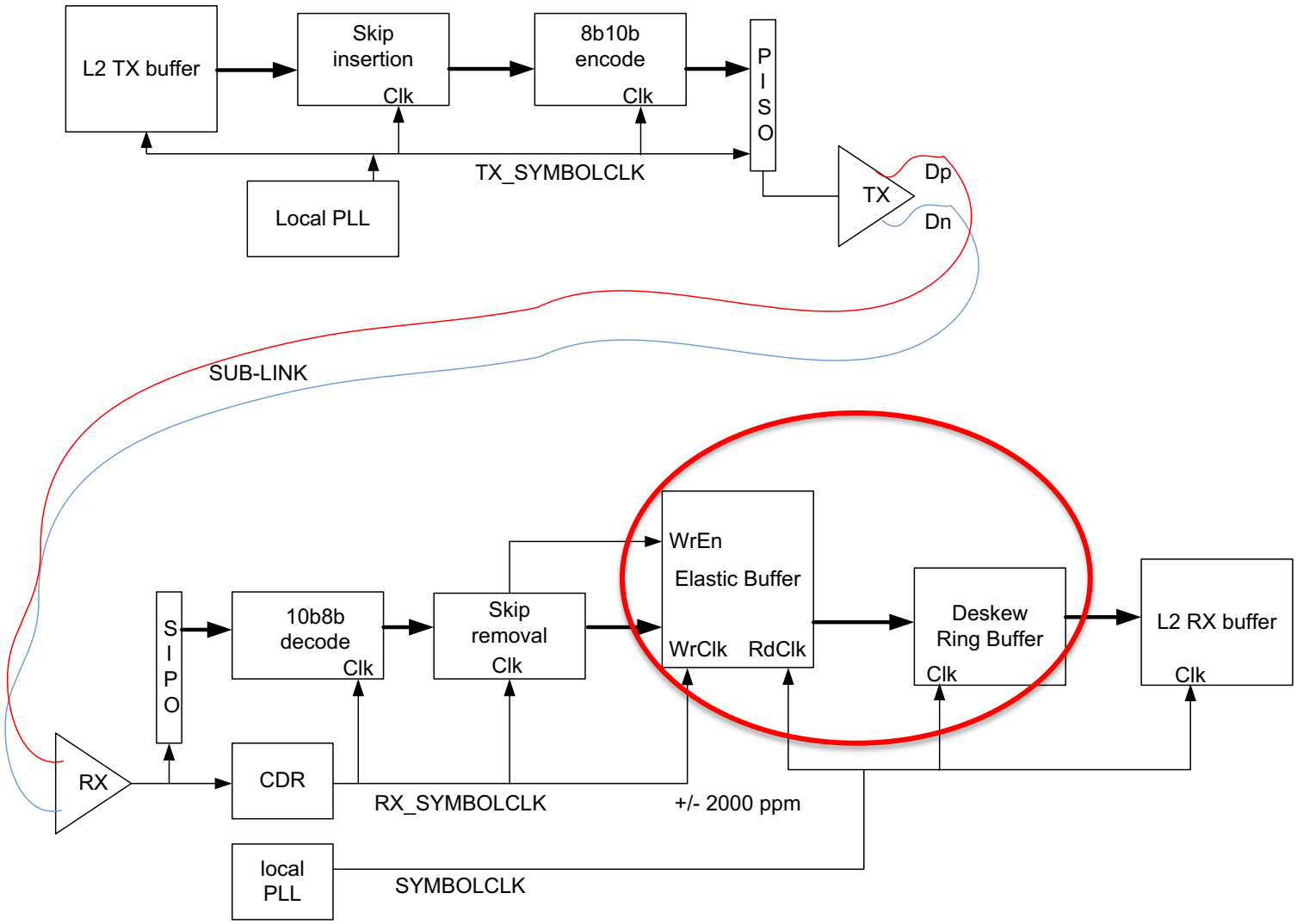


c) Locally Generated RefClk, no Sharing

Shared RefClk switching recommendations

- RefClk is mandatory during HS-MODE
- Switching is Application Controlled
- RefClk shall be switched on:
  - Before DME_HIBERNATE_EXIT.req into HS-MODE
  - Before DME_POWERMODE.req into HS-MODE
- RefClk should be switched off after
  - DME_HIBERNATE_ENTER.ind (after delay)

Skip architecture



mipi alliance

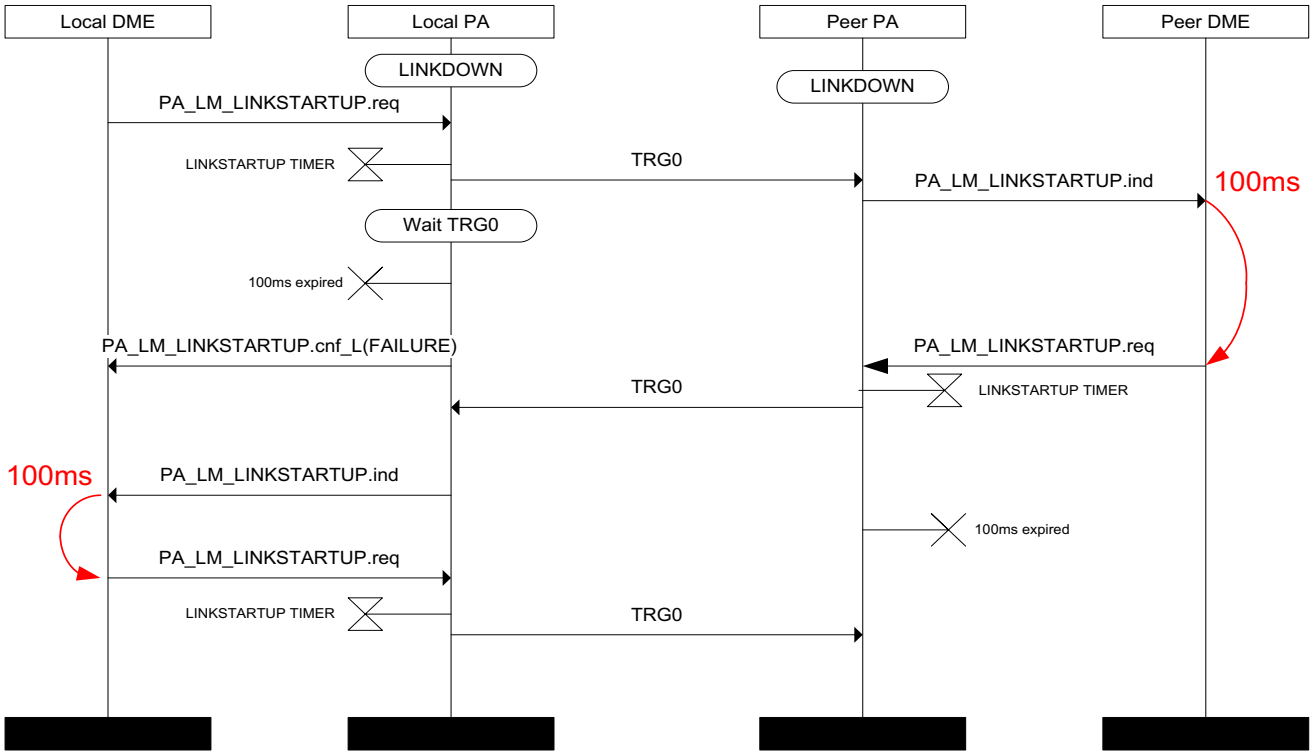
Purpose of SKIP architectures

- For Applications mandating same GEAR/MODE in forward and reverse SUB-LINK
- Eases core implementation by reducing clock domain crossings
  - Inserting skip reduces tx payload bandwidth up to the point the receiver can process it
- Shared RefClk based Applications may not benefit from

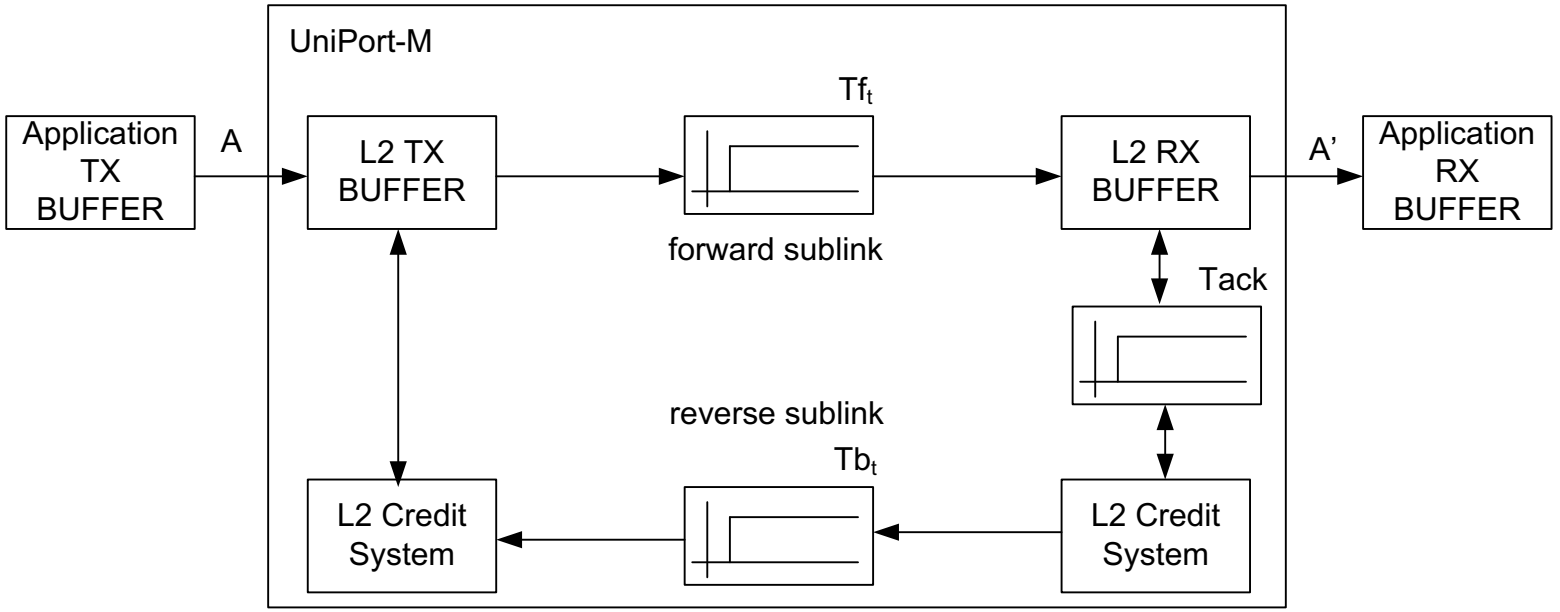
LinkStartup

- UniPro v1.61 requires a synchronized DME_RESET.req between local and peer Device
  - Synchronous reset line
  - Synchronous entry into LINK DOWN
  - Within 100ms synchronous DME_LINKSTARTUP.req()

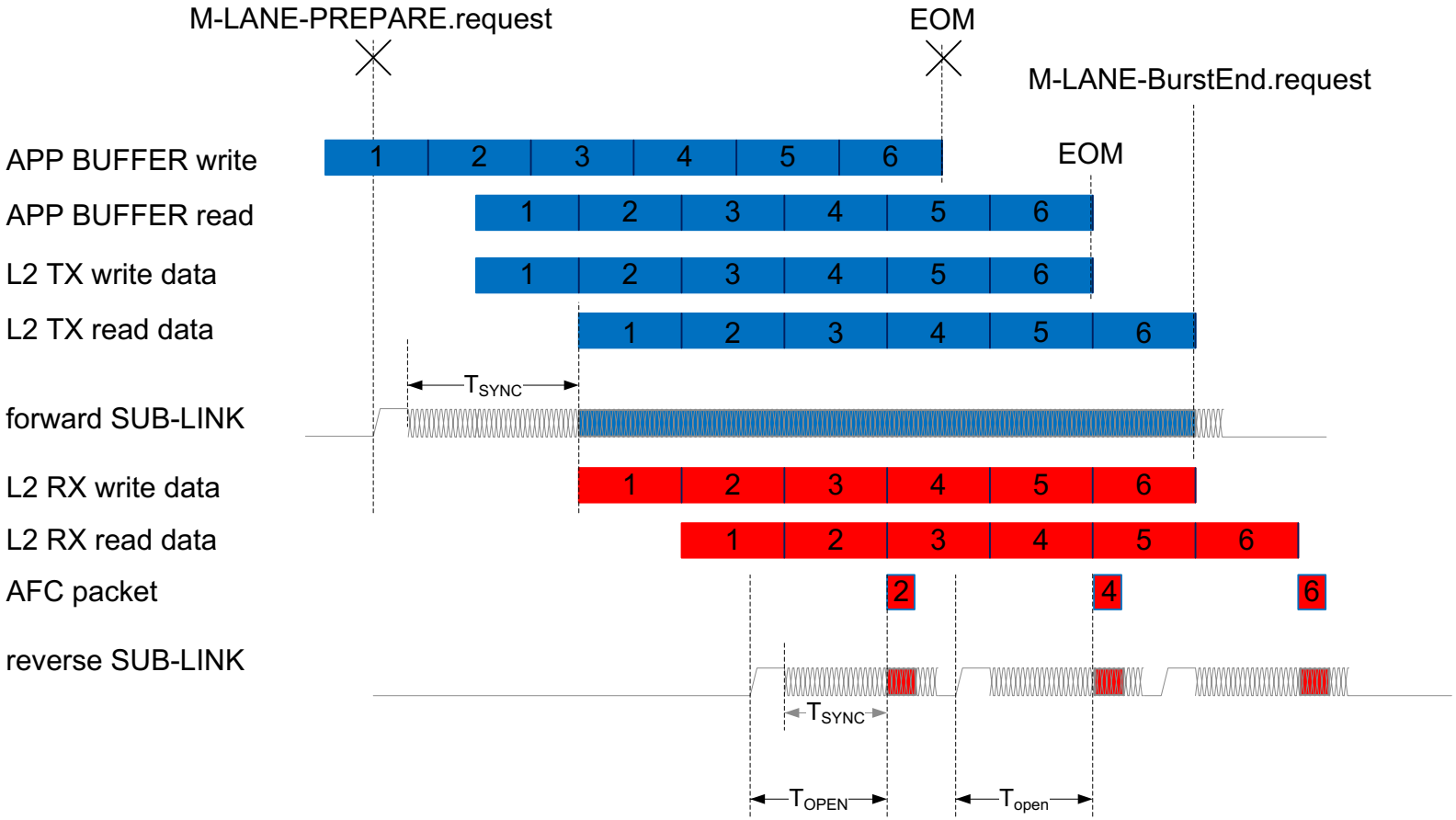
LINKSTARTUP timeout loop



Link Performance, Burst Control

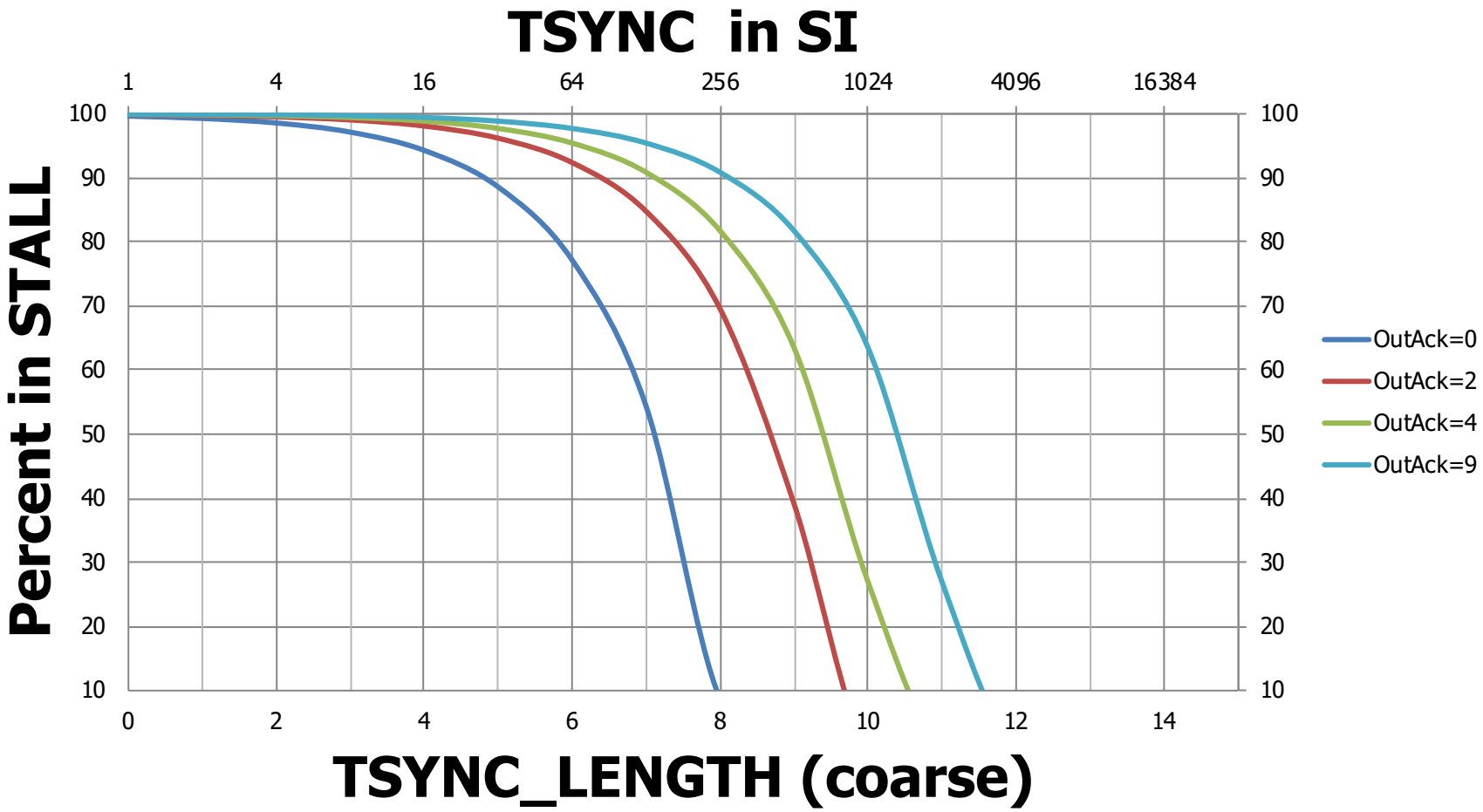


Burst control from Application



- Start Tsync already with Application buffer write!
- Save power on reverse channel by keeping Tsync small

Power Saving with small TSync



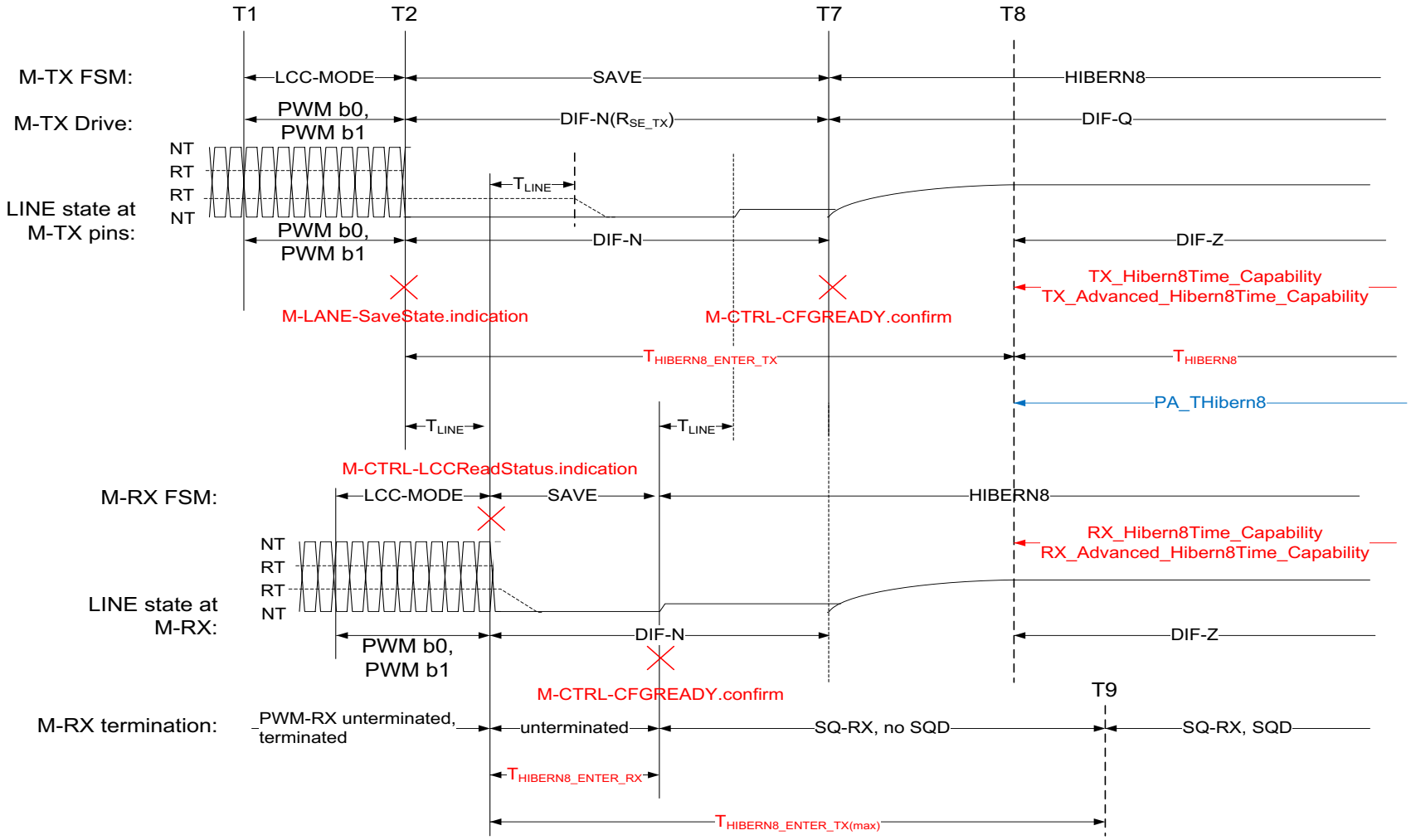
QUESTIONS AND (HOPEFULLY) ANSWERS

BACKUP SLIDES

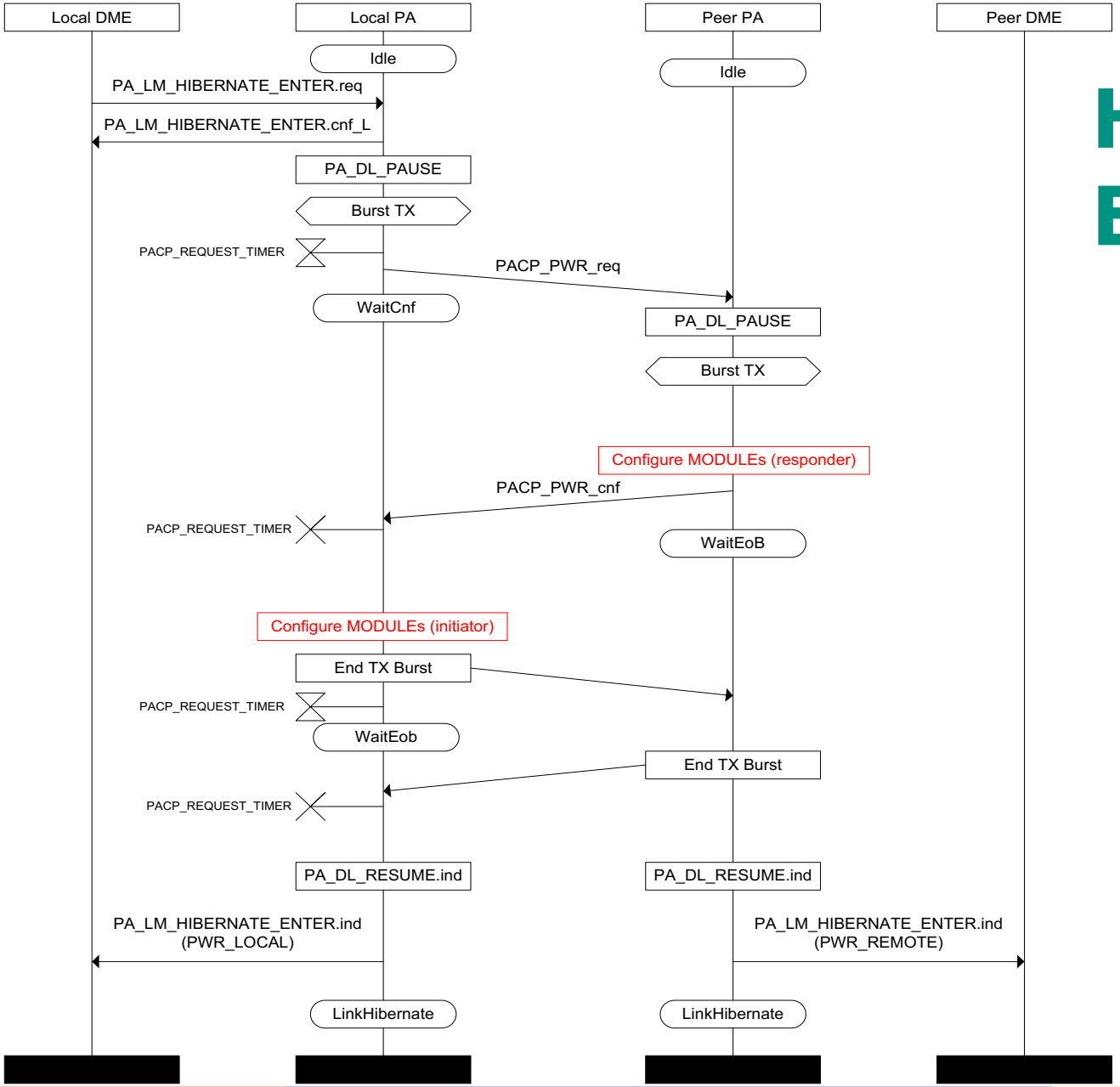
Shared RefClk switching (informative)

- Shared RefClk shall not be switched off
  - With DME_RESET.req (is only local!)
  - With DME_LINKLOSS.ind (only inbound Link!)
  - With detected LINE-RESET (unsynchronized between forward and reverse channel)
  - After a PWR_FATAL response (peer may need RefClk to recover!)
- Shared RefClk may be switched off
  - After DME_POWERMODE.ind(PWR_OK) for both SUB-LINKs into LS-MODE (after delay)
  - DME_POWERMODE.cnf (FAILURE), when none of the SUB-LINKs is in HS-MODE
  - DME_LINKSTARTUP.ind()

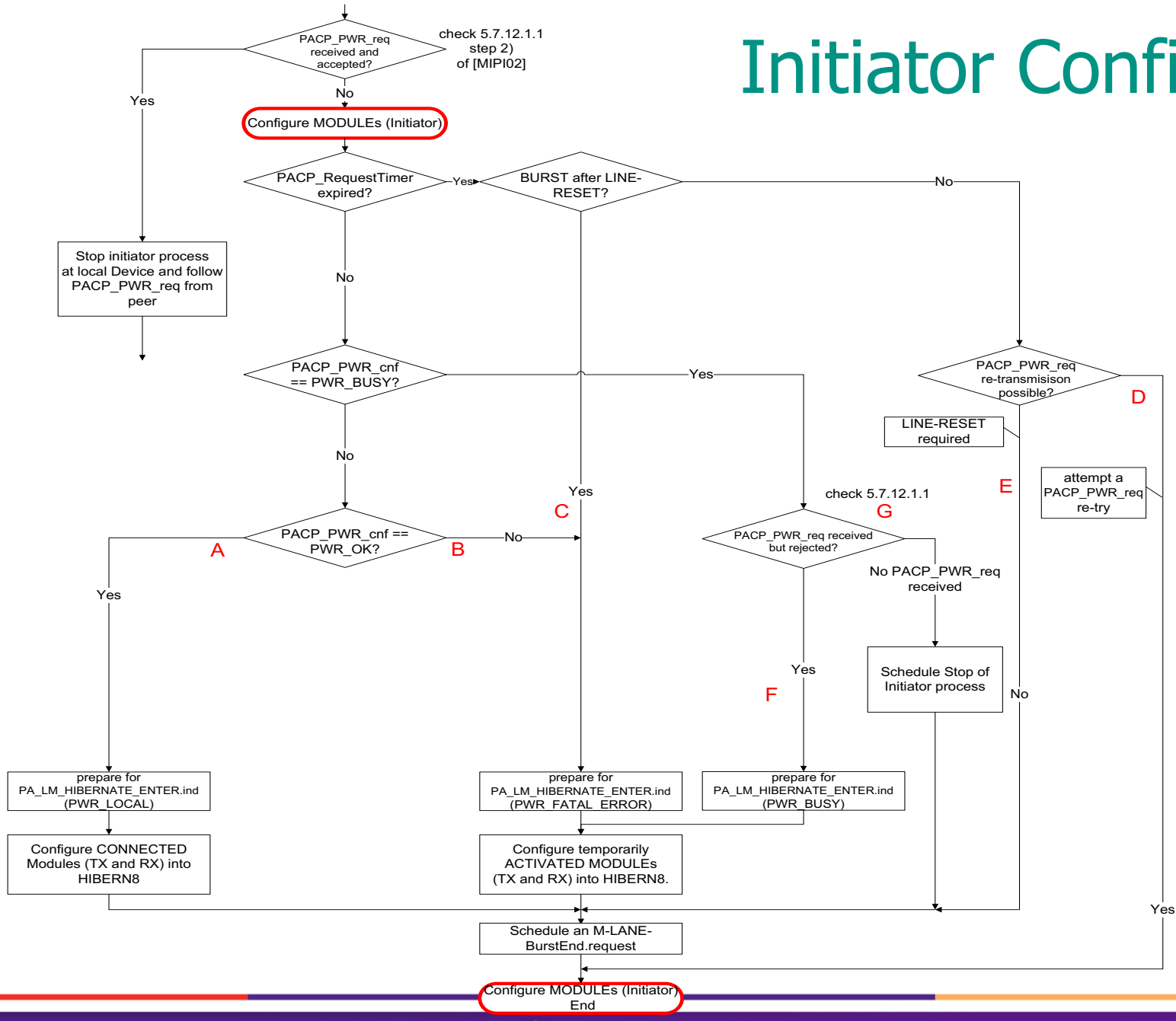
LINECFG to HIBERN8



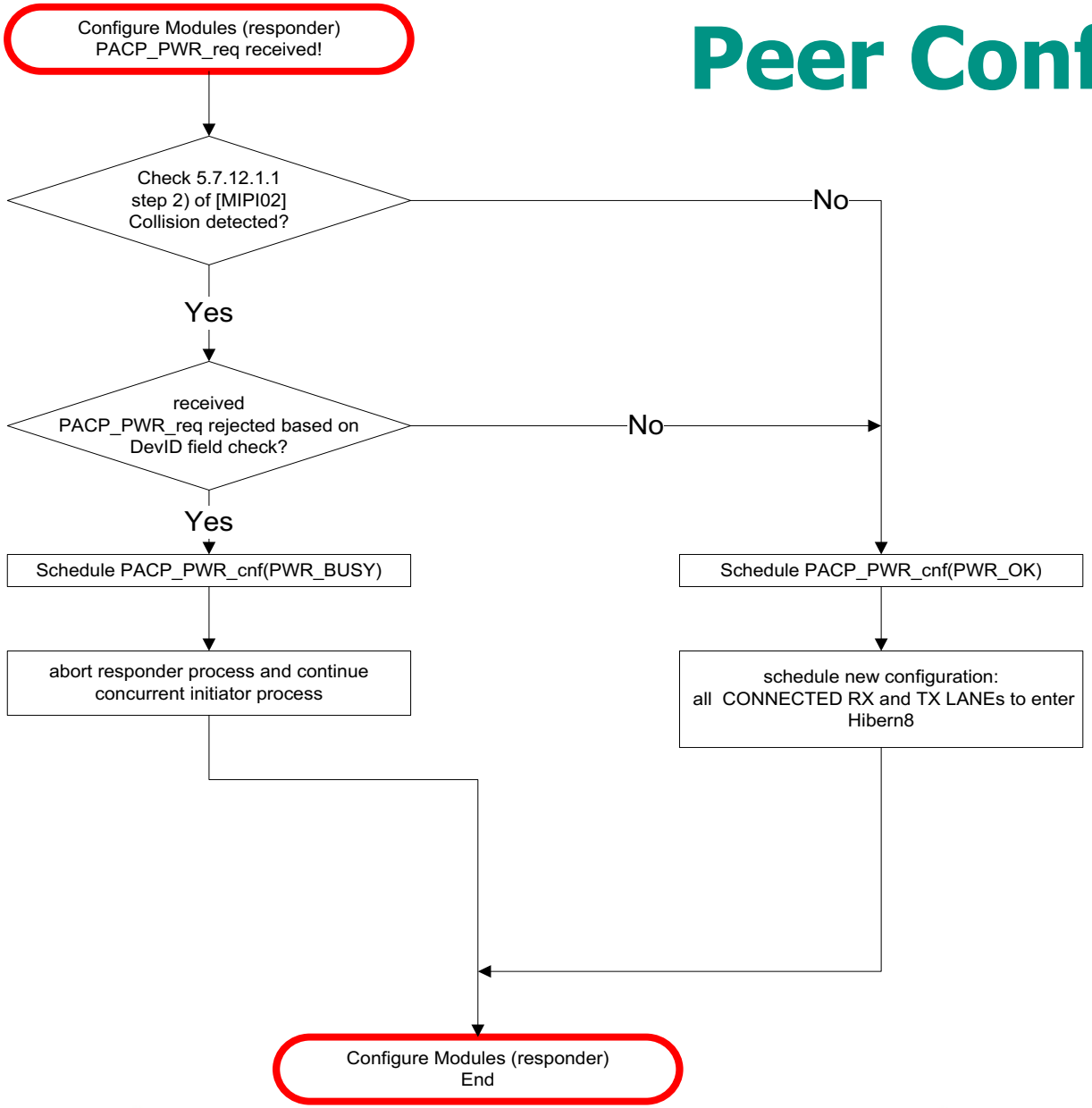
HIBERN8 Enter



Initiator Config



Peer Config



Buffer Usage (OUTACK Threshold = 1)