Universal Solution to Sideband Proliferation Using MIPI Virtual GPIO Interface

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John Oakley, Intel
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<table>
<thead>
<tr>
<th>#</th>
<th>Topics</th>
<th>Speaker(s)</th>
<th>Time (Minutes)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Opening and Speaker Self-Introduction</td>
<td>Peter Lefkin, Lalan Mishra, Satwant Singh, John Oakley, Laura Nixon</td>
<td>05</td>
</tr>
<tr>
<td>2</td>
<td>MIPI: A Brief Overview</td>
<td>Peter Lefkin</td>
<td>05</td>
</tr>
<tr>
<td>2</td>
<td>The Issue of Sideband Proliferation and The Need to address it</td>
<td>Satwant Singh</td>
<td>05</td>
</tr>
<tr>
<td>3</td>
<td>Virtual GPIO Interface (VGI): Concept and Architectural Overview</td>
<td>Lalan Mishra</td>
<td>20</td>
</tr>
<tr>
<td>4</td>
<td>VGI in relation to other familiar Interfaces</td>
<td>John Oakley</td>
<td>07</td>
</tr>
<tr>
<td>5</td>
<td>MIPI VGI Timeline</td>
<td>Laura Nixon</td>
<td>03</td>
</tr>
<tr>
<td>6</td>
<td>Summary</td>
<td>Lalan Mishra</td>
<td>05</td>
</tr>
<tr>
<td>7</td>
<td>Q&amp;A</td>
<td>All</td>
<td>10</td>
</tr>
</tbody>
</table>
Brief overview from Peter Lefkin
Managing Director, MIPI Alliance
About MIPI Alliance

We are a global, collaborative organization comprised of over 250 member companies spanning the mobile and mobile-influenced ecosystems.

MIPI Alliance is leading innovation in mobile interface technology.
MIPI Alliance Member Ecosystem
Partners

MIPI Alliance is proud to be a part of the mobile device industry. While our interest is focused on interfaces within mobile device design, we recognize and appreciate other organizations which also support this industry.

JEDEC
MEMS Industry Group
PCI-SIG
UFSA
USB Implementers Forum, Inc.
VESA
Active Technical Working Groups

- Camera
- Debug
- Display
- Low Latency Interface
- Low Speed Multipoint Link
- PHY (C/D/M)
- Reduced Input Output
- RF Front End
- Sensor / I3C
- Software
- Test
- UniPro
MIPI Alliance continues to evolve its Roadmap to meet the needs of the mobile and mobile-influenced industry with new and revised specifications.
The Issue of Sideband Proliferation
Mobile Connectivity Expansion Trends

Cellular
- 2G/3G/4G → LTE-Advanced

WiFi
- 802.11a/b/g/n/ac →
  802.11ad/WiGig

Video
- VGA/SD/HD → 4K

Docking
- Charging/audio/video →
  Productivity, Games and External Storage
The Problem of Sideband Proliferation

Applications Processor (SoC)

Modem
- GPIOs: x9
- PCIe/M-Pcie/HSIC/USB
- CLKREQ
- WAKEUP
- RESET
- STAT
- ERR
- CHNL_RD

Wireless LAN
- Bluetooth
- Gigabit Wireless LAN (60-GHz)
- GPIOs: x5
- PCIe/M-Pcie/HSIC/USB
- CLKREQ
- WAKEUP
- RESET
- EN
- P_DN

Companion / Bridge-Chip
- GPIOs: x8
- PCIe/M-Pcie/HSIC/USB
- CLKREQ
- WAKEUP
- RESET
- EN
- P_DN

Optional Connector

Ethernet
VGI: Solution to Sideband Proliferation

Modem

Wireless LAN

Bluetooth

Gigabit Wireless LAN (60-GHz)

Applications Processor (SoC)

VGI I/O Expander

Companion / Bridge-Chip

Ethernet

Optional Connector
Virtual GPIO Interface: Concept and Architectural Overview
**VGI :: The Concept**

- **VGI** consolidates *N*-sideband GPIOs and sub-100 MHz serial messaging over 2 or 3 wire interface in a Point-to-Point configuration

- **2-wire VGI** : Asynchronous, Full-Duplex

- **3-wire VGI** : Synchronous, Full-Duplex

- **VGI Rev-1 Max Speed**: 38.4MHz

✓ Consolidates Low Speed Messaging Interface and Sideband GPIOs (*N*-pins to 2/3-pins reduction)
HLOS processing latency varies widely
Deep-sleep to active-state typical latency: Typically \( \rightarrow 30 \text{ to } 100\)-mS
Timing uncertainty not suitable for the key IPC side-band signaling
VGI Architectural Block-Diagram
VGI Physical Interface Characteristics

1. Asynchronous VGI
   - Initial and Power State Transition mode communication over 2-wire

2. Synchronous VGI
   - Common clock (Up to 38.4 MHz in VGI Rev-1)
   - Sleep clock based operation supported in Low Power Modes
VGI Techniques At-a-Glance

VGI-Techniques

E.g. Power-ON/Default mode Communication RO-PWM

3-Wire I/F

Device #1

Device #2

Tx/Rx

Rx/Tx

CLK

2-Wire I/F

Device #1

Device #2

Tx/Rx

Rx/Tx

Synchronous Mode

Asynchronous Modes

A

B

C

D

RO- PWM*

UART

Std. – PWM

PM – PWM **

* Ring-Oscillator based PWM,  ** Phase-Modulated PWM
Asynchronous UART Mode

Illustration#1: 8-bit frame

Illustration#2: 12-bit frame

Illustration#2: 16-bit frame
Asynchronous UART Mode

H/W Flow Control over Tx/Rx eliminates RTS/CTS physical pins
Asynchronous VGI: Phase-Modulated PWM

Symbol to signal mapping for a joint (PWM+Phase) modulation scheme

Example Representation of an arbitrary data-sequence “10011101”

Link throughput and power :: A comparative look

Highlights:
- All Digital Solution
- 2x Throughput
- Time-domain data compression
- Link power Reduction by 50%

Link throughput improvement = 2x
Lossless Data Compression= 2x
Link Power Reduction = 50%
Synchronous 3-Wire VGI

Shift register includes buffering option to allow GPIO changes during ongoing transmission. Buffer depth is predefined.

Tx on Neg-Edge

Rx on Pos-Edge

GPIO state Transmission starts when current state does not match with past state.

State Machine Key-Characteristics:

- Failure of full-frame transmission is used as device-status signal by the receiving side.
VGI Protocol – 1 of 3

- Addresses P2P VGI link requirements only
- Only 2-bits required as function bits. A 3rd function bit used during link length programming.

**NOTE**: The mechanism has a fixed overhead of two-bits over the base-line vGPIO implementation.
• Addresses P2P and P2MP links.
• No provision for error-detection and correction capability.

### Function Bits Description

<table>
<thead>
<tr>
<th>Function_Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Following bits are vGPIO states</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Following bits are message bits.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Following bit-stream represent the vGPIO stream length to be set on the receiver side.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Following bit-stream represent the new vGPIO stream length acknowledgement w.r.t the previously received stream-length programming command.</td>
</tr>
</tbody>
</table>

**NOTE:** The mechanism has a fixed overhead of three-bits over the base-line vGPIO implementation.
VGI Protocol – 3 of 3

- Uses 10-bits (maximum) in the Function-bit-field
- First two function bits are used for operation mode setting
- The remaining 8-bits (Mode “10”) are Extended Hamming (8,4) coded 8-bit code words defining unique functions
- Provides option for easy expansion to add new functions

**Diagram:**

<table>
<thead>
<tr>
<th>Start-bit</th>
<th>Fn_Bit-0</th>
<th>Fn_Bit-1</th>
<th>Fn_Bit-2</th>
<th>...</th>
<th>Fn_Bit-6</th>
<th>Fn_Bit-9</th>
<th>GPIO/Msg Bit-0</th>
<th>GPIO/Msg Bit-1</th>
<th>...</th>
<th>GPIO/Msg Bit-(n-1)</th>
<th>GPIO/Msg Bit-n</th>
<th>Stop-bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

**Start-bit**

- 0

**Op-Mode Bits**

<table>
<thead>
<tr>
<th>D0</th>
<th>D1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**Stop-bit**

- 1

**Function-bit-field**

- 10-bit long Function-bit-field

**GPIO/Msg Bits**

- Maximum number of I/O or message bits = 128 bits

**Expression:**

\[ \text{Maximum number of I/O or message bits} = 128 \]
VGI FSM Integration with I3C (I3C_VGI)

- **VGI FSM** could be integrated with a serial interface of choice, such as I3C.
- MIPI I3C supports VGI integration through command code support.
- Helps reduce Hardware event pins at system level.
**VGI FSM Integration with I3C (I3C_VGI)**

- HW Event sideband signals are eliminated

- VGI-FSM (Finite State Machine) performs I3C message encoding/decoding for HW events and thus frees up the associated CPU on the host-SoC for these tasks.

- Impact is reduced Latency and Power consumption.
VGIO in Relation to Other Interfaces
VGI Comparison

- Comparison of Various Low Speed Interfaces
Comparing VGI with Low speed interfaces

- **SPI**
  - Master-Slave approach
  - Custom implementations, no common methods
- **I3C**
  - Master-Multi Slave, Open-Drain approach
  - In-band interrupts
- **RFFE**
  - Master-Multi Slave approach
- **UART**
  - Custom implementations, requires reference clocks
- **VGI**
  - Symmetric control approach (No Master No Slave)
  - Initialization from either side
VGI Clocking Comparison

- **UART**
  - Requires Reference Clock with Agreed rates

- **SPI, I3C, RFFE**
  - Clock is forwarded from Master to Slave

- **VGI**
  - Using RO-PWM PHY option, the clocking is forwarded with data
  - Only Transmitter requires clock to create telegrams
  - Receiving side captures telegrams without internal clock
    - Useful for devices which power down
    - Useful for very simple write-only devices (LED bank)
Phased VGI Adoption – Leveraging Smaller FPGAs

- **Full VGI Adoption**
  - Device A (e.g., Host)
  - Device B (e.g., Peripheral)
  - Native VGI Interface
  - Native VGI Interface

- **Partial VGI Adoption**
  - Device A
  - Device B
  - FPGA VGI Bridging: Case-1
  - FPGA VGI Bridging: Case-2

- **Partial VGI Adoption**
  - Device A
  - Device B
  - SB / GPIOs

- **No VGI Adoption**
  - Device A
  - Device B
  - Across connectors, cables, hinges or pogo-pins etc.

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- **SB**: Sideband Signals
Summary

- Sideband GPIOs add to SoC and PCB level cost and complexity

- MIPI VGI Architecture consolidates sideband GPIOs and Low-Speed serial interface in P2P configuration to reduce I/O pins

- Both 2 and 3-wire interface options are available

- Common start-up mode ensures interoperability

- The VGI FSM can be combined with any other interface bus of choice, e.g. I3C_VGI

- The VGI specification is to be released later this year
Questions?