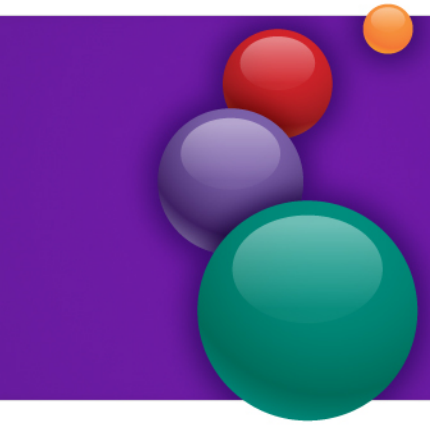
Universal Solution to Sideband Proliferation Using MIPI Virtual GPIO Interface



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Satwant Singh, Lattice Semiconductor
John Oakley, Intel

Date: 05/10/16

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Agenda

#	Topics	Speaker(s)	Time (Minutes)
1	Opening and Speaker Self-Introduction	Peter Lefkin Lalan Mishra Satwant Singh John Oakley Laura Nixon	05
2	MIPI : A Brief Overview	Peter Lefkin	05
2	The Issue of Sideband Proliferation and The Need to address it	Satwant Singh	05
3	Virtual GPIO Interface (VGI): Concept and Architectural Overview	Lalan Mishra	20
4	VGI in relation to other familiar Interfaces	John Oakley	07
5	MIPI VGI Timeline	Laura Nixon	03
6	Summary	Lalan Mishra	05
7	Q&A	All	10

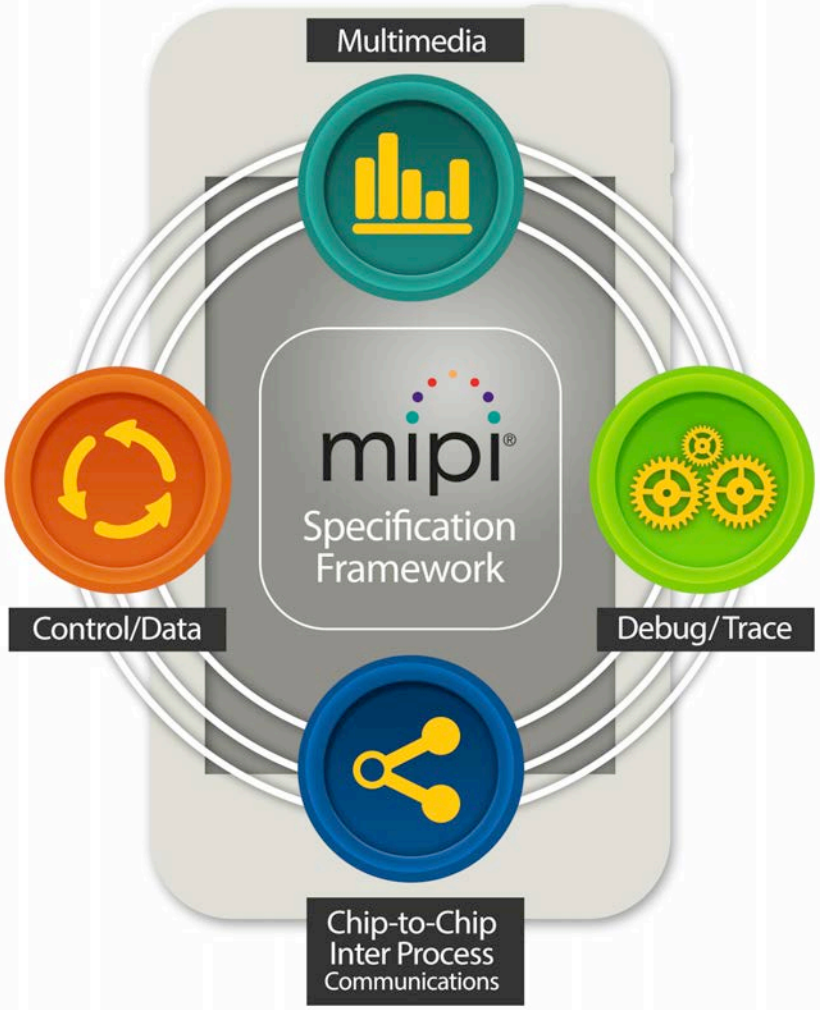
Brief overview from Peter Lefkin

Managing Director, MIPI Alliance

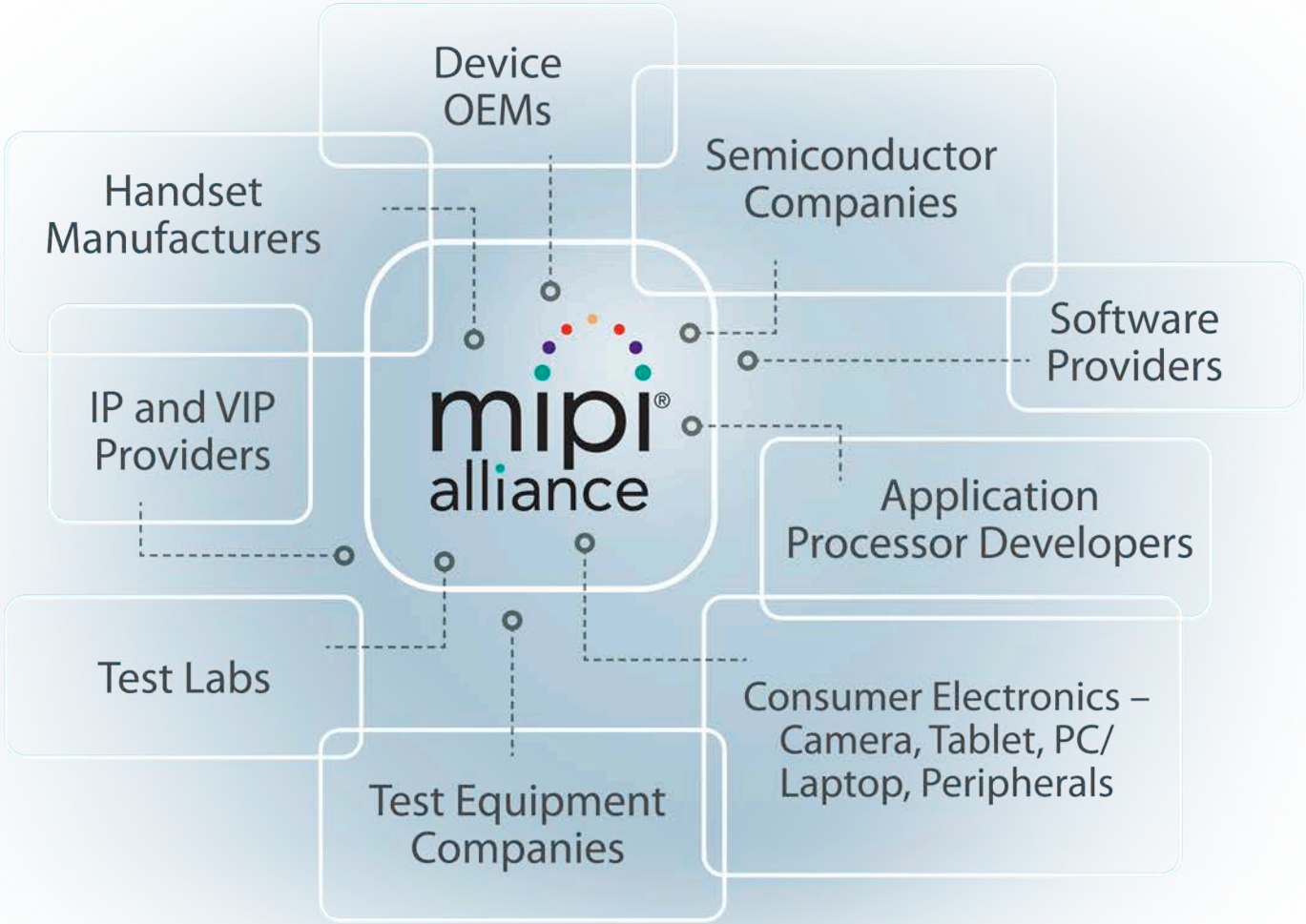
About MIPI Alliance

We are a global, collaborative organization comprised of over 250 member companies spanning the mobile and mobile-influenced ecosystems.

MIPI Alliance is leading innovation in mobile interface technology.



MIPI Alliance Member Ecosystem



Partners

MIPI Alliance is proud to be a part of the mobile device industry. While our interest is focused on interfaces within mobile device design, we recognize and appreciate other organizations which also support this industry.

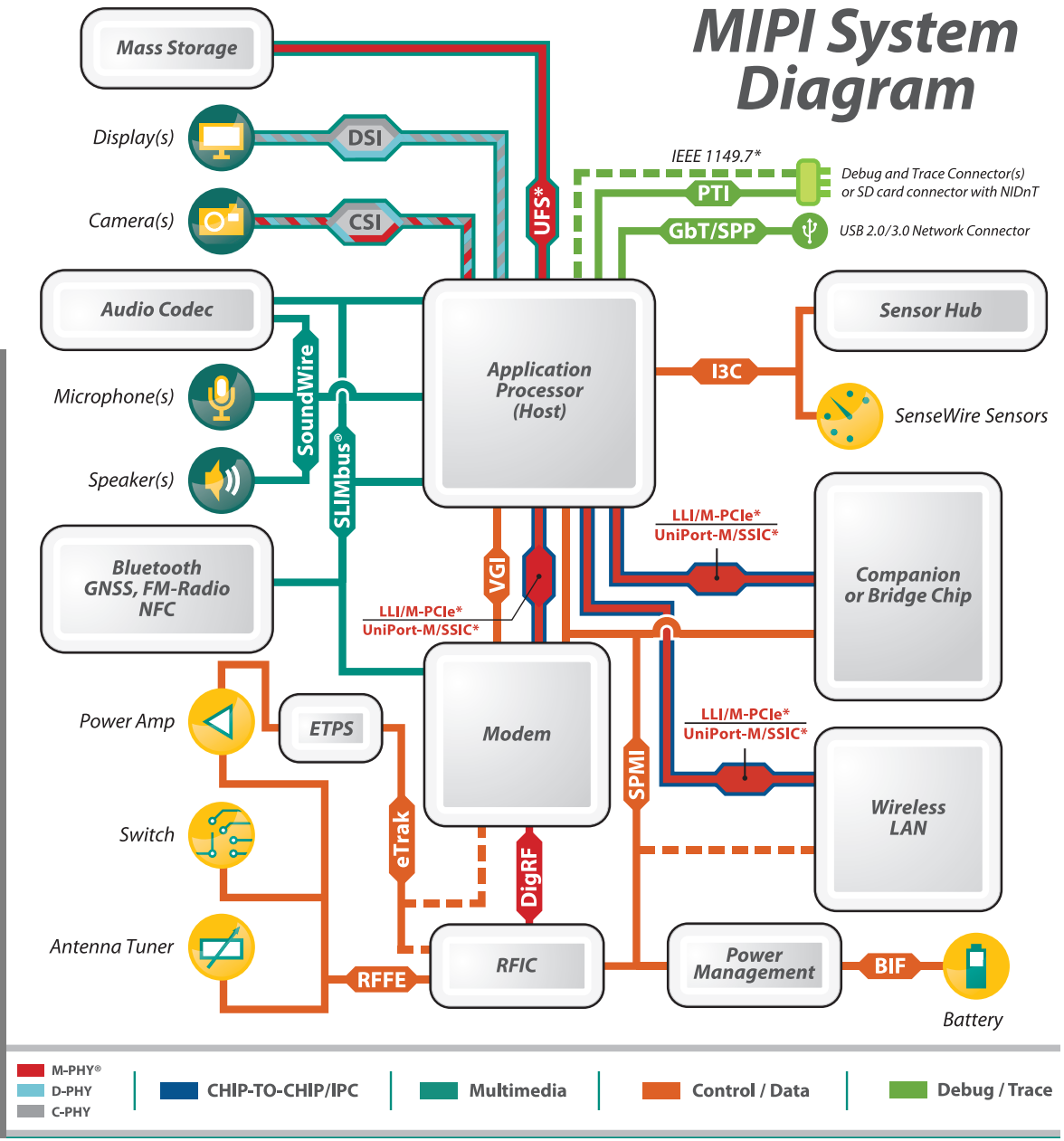
JEDEC
MEMS Industry Group
PCI-SIG
UFSA
USB Implementers Forum, Inc.
VESA

Active Technical Working Groups

Camera	Debug	Display	Low Latency Interface
Low Speed Multipoint Link	PHY (C/D/M)	Reduced Input Output	RF Front End
Sensor / I3C℠	Software	Test	UniPro℠

Roadmap

MIPI Alliance continues to evolve its Roadmap to meet the needs of the mobile and mobile-influenced industry with new and revised specifications.



The Issue of Sideband Proliferation

Mobile Connectivity Expansion Trends

Cellular

- 2G/3G/4G ➔ LTE-Advanced

WiFi

- 802.11a/b/g/n/ac ➔ 802.11ad/WiGig

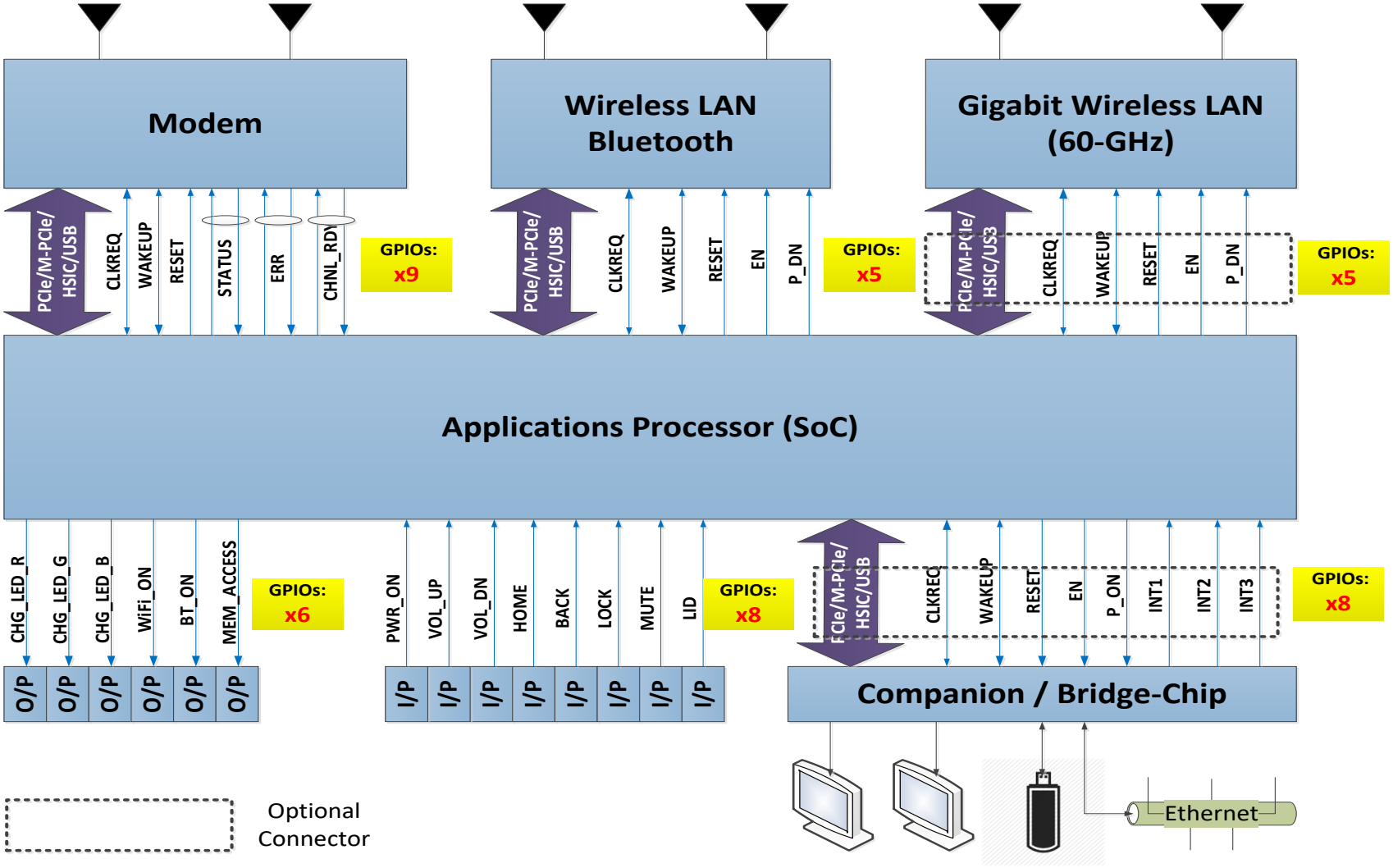
Video

- VGA/SD/HD ➔ 4K

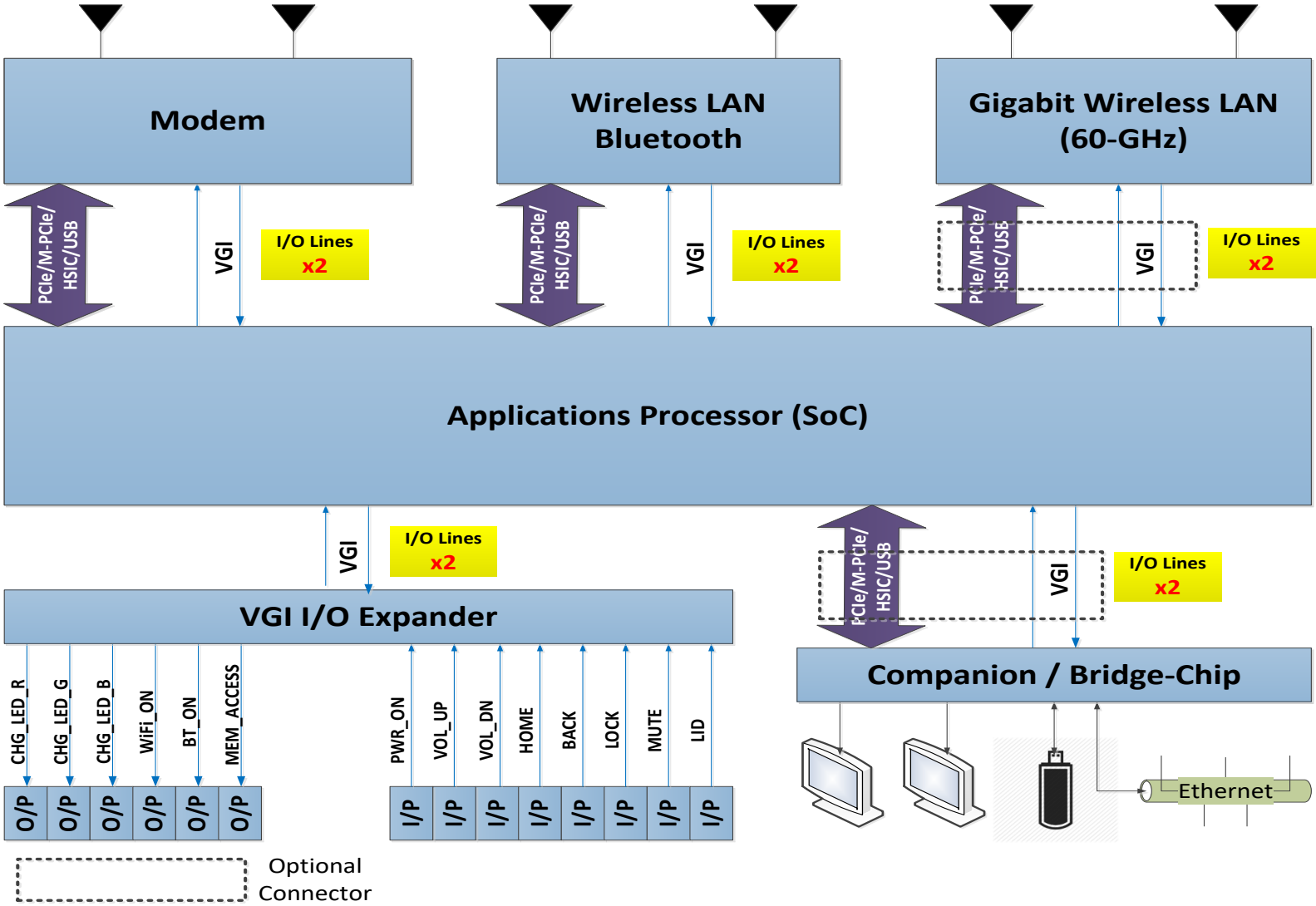
Docking

- Charging/audio/video ➔ Productivity, Games and External Storage

The Problem of Sideband Proliferation



VGI : Solution to Sideband Proliferation



Virtual GPIO Interface: Concept and Architectural Overview

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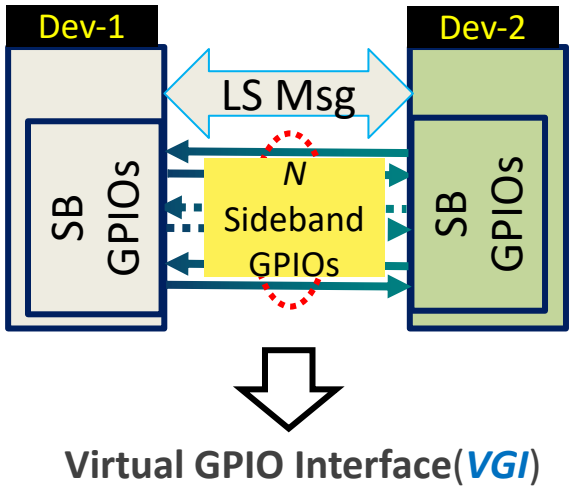
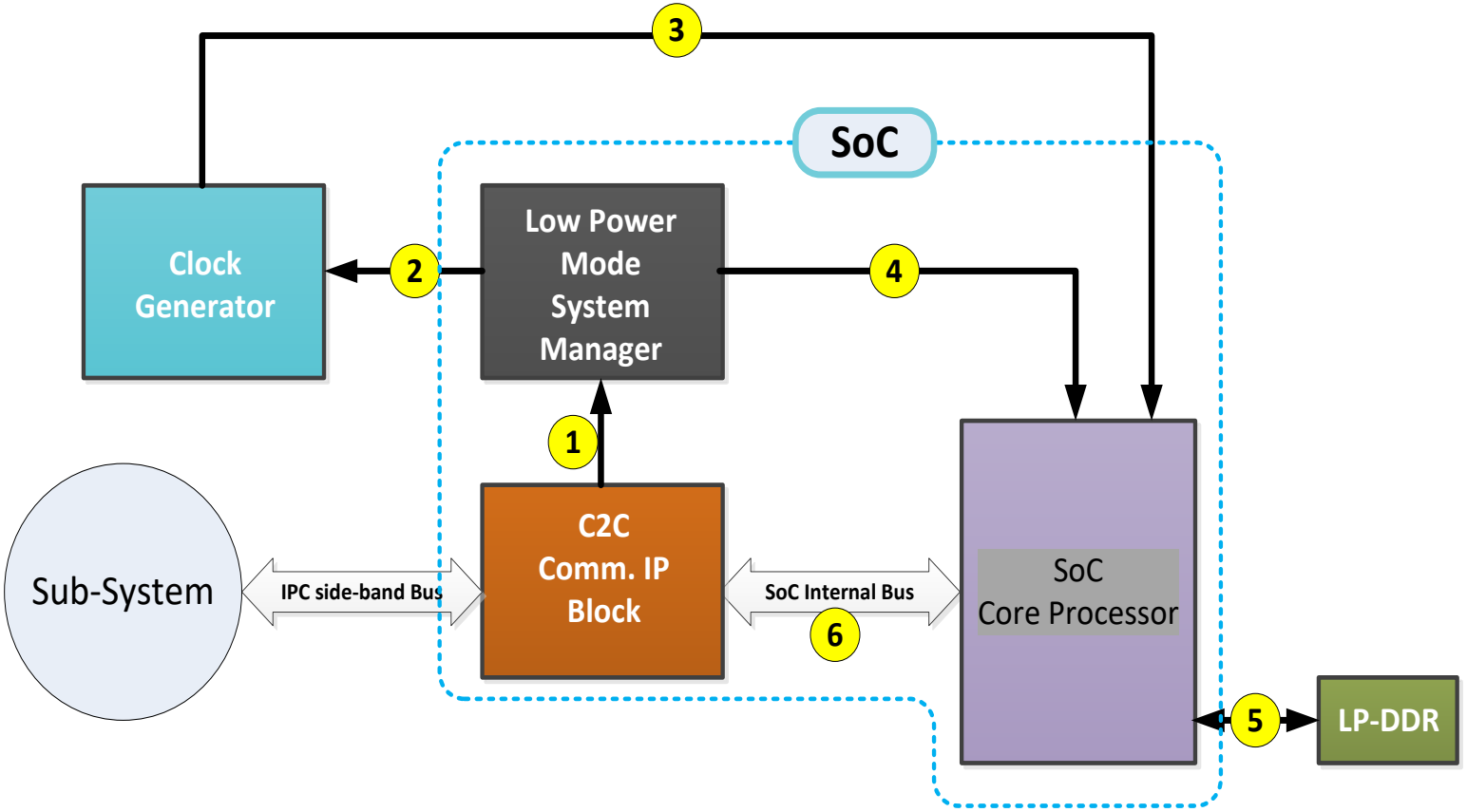
VGI :: The Concept

- **VGI** consolidates ***N***-sideband GPIOs and sub-100 MHz serial messaging over **2** or **3** wire interface in a Point-to-Point configuration
- **2-wire VGI** : Asynchronous, Full-Duplex
- **3-wire VGI** : Synchronous, Full-Duplex
- **VGI Rev-1 Max Speed**: 38.4MHz



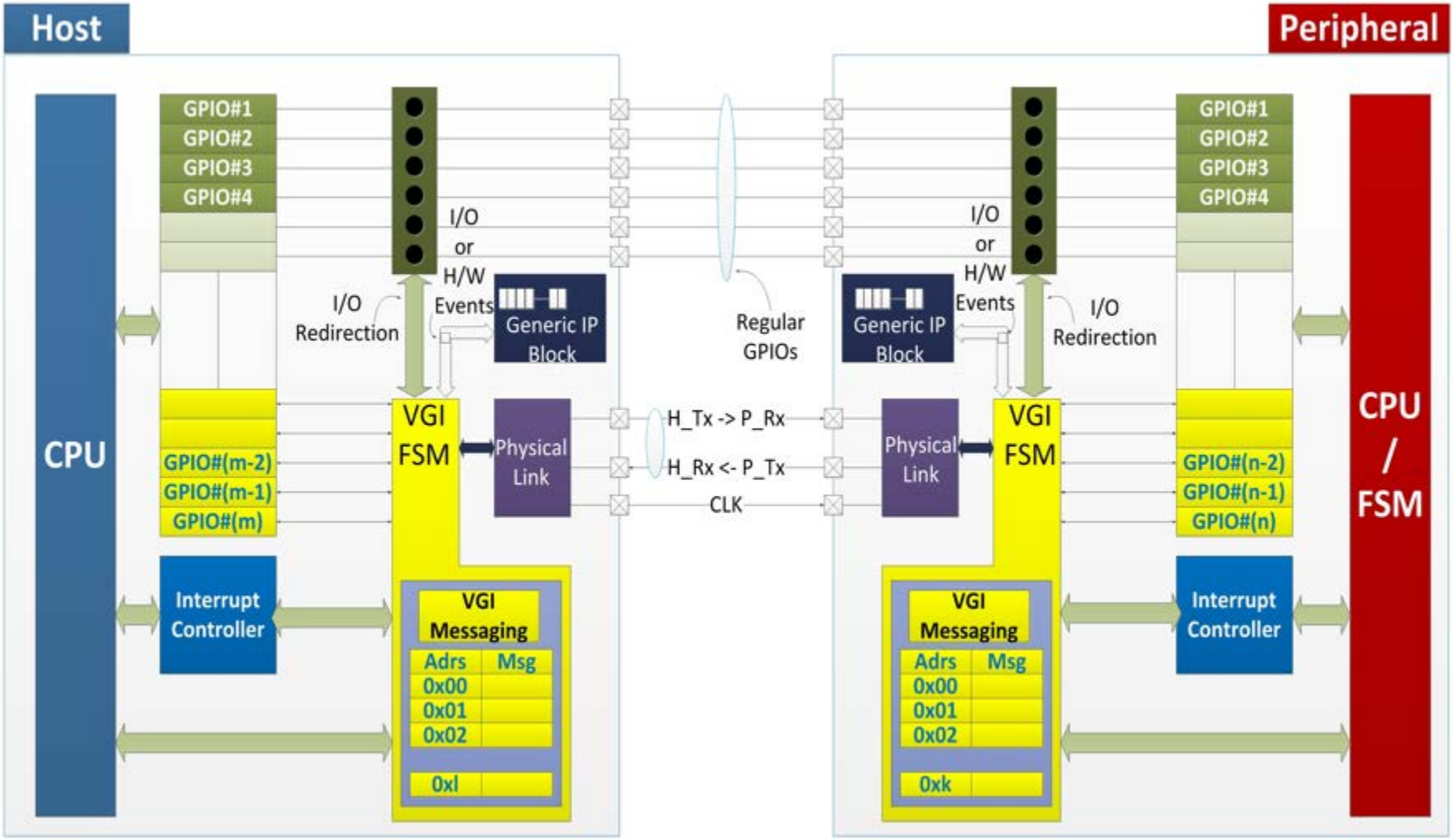
✓ **Consolidates Low Speed Messaging Interface and and Sideband GPIOs (N-pins to 2/3-pins reduction)**

Limitation of Conventional Techniques

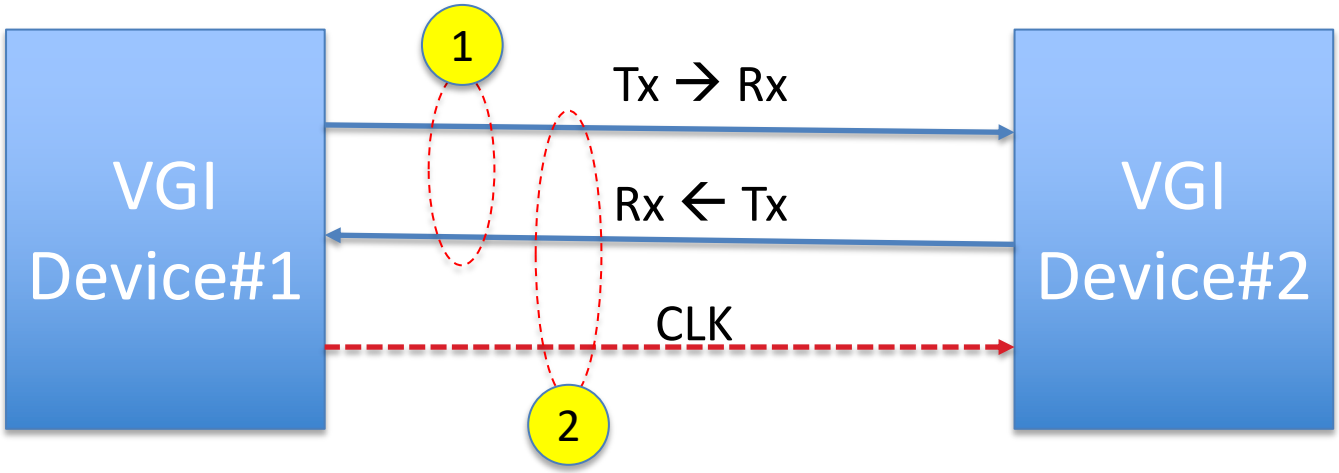


- ✓ HLOS processing latency varies widely
- ✓ Deep-sleep to active-state typical latency : Typically → 30 to 100-mS
- ✓ Timing uncertainty not suitable for the key IPC side-band signaling

VGI Architectural Block-Diagram



VGI Physical Interface Characteristics



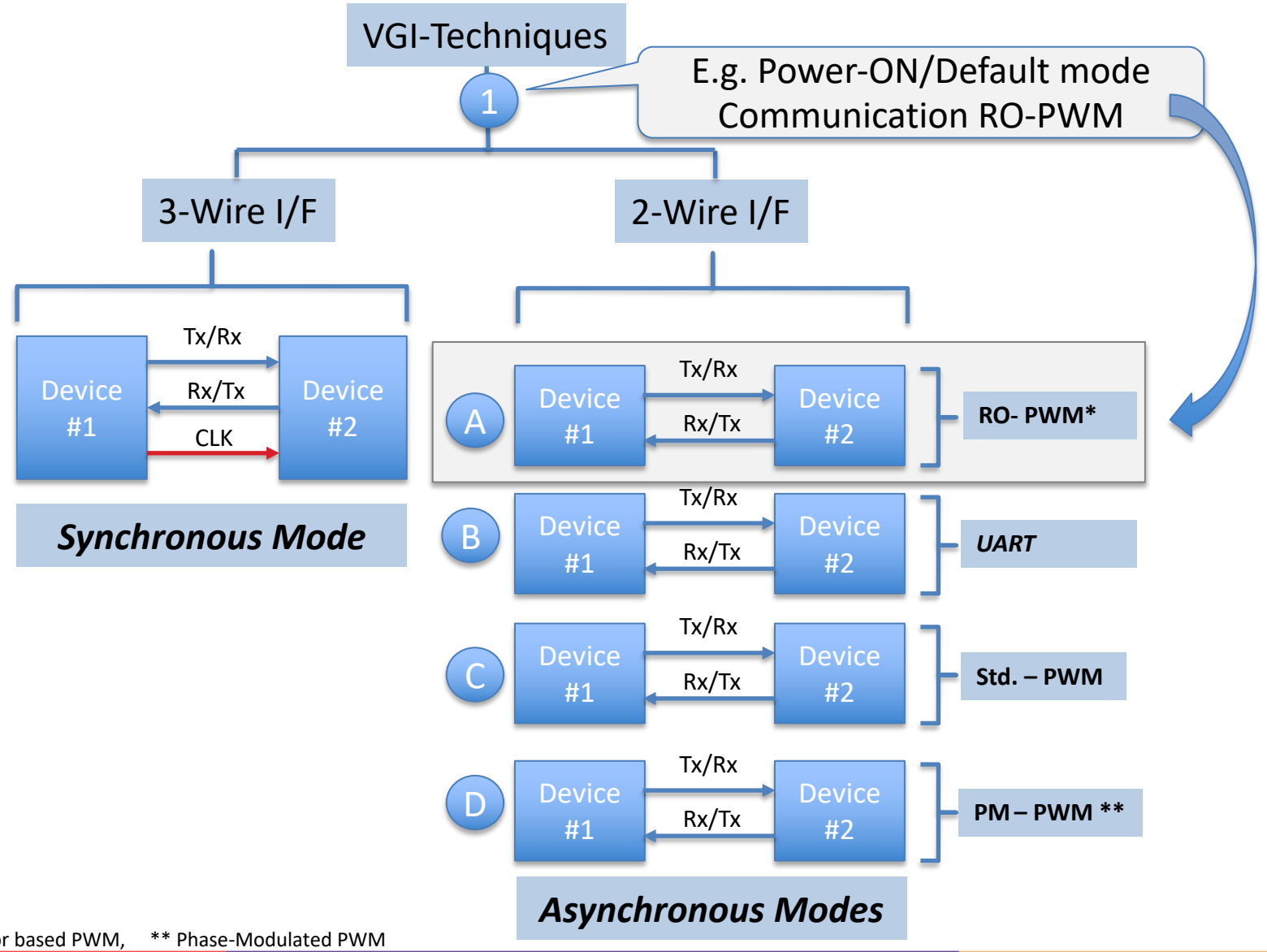
1 Asynchronous VGI

- Initial and Power State Transition mode communication over 2-wire

2 Synchronous VGI

- Common clock (Up to 38.4 MHz in VGI Rev-1)
- Sleep clock based operation supported in Low Power Modes

VGI Techniques At-a-Glance



* Ring-Oscillator based PWM, ** Phase-Modulated PWM

Asynchronous UART Mode

A

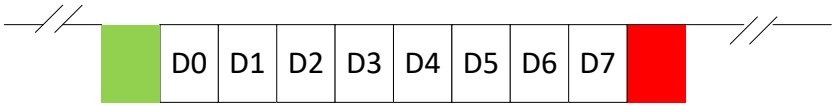
Variable-Frame Length

Start-Bit

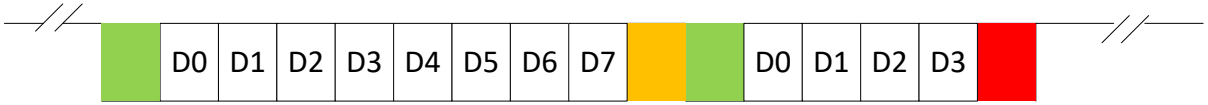
Intermediate Stop-Bit

Stop-Bit

Illustration#1 : 8-bit frame



Illustration#2 : 12-bit frame



Illustration#2 : 16-bit frame

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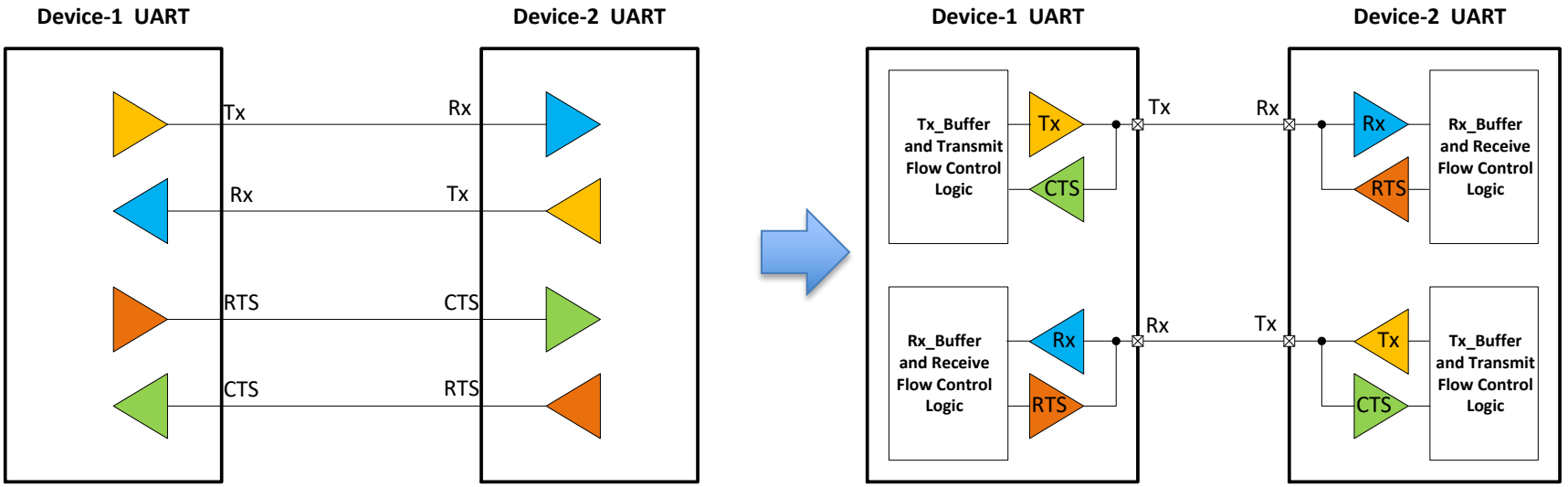
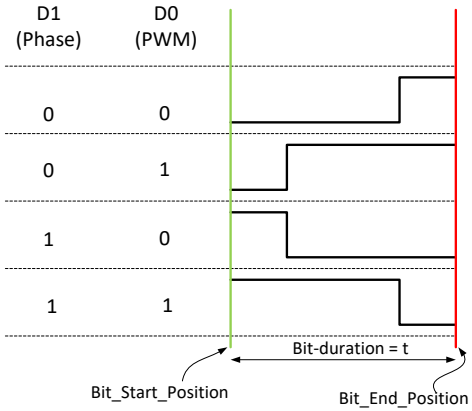
Asynchronous UART Mode

B H/W Flow Control over Tx/Rx eliminates RTS/CTS physical pins



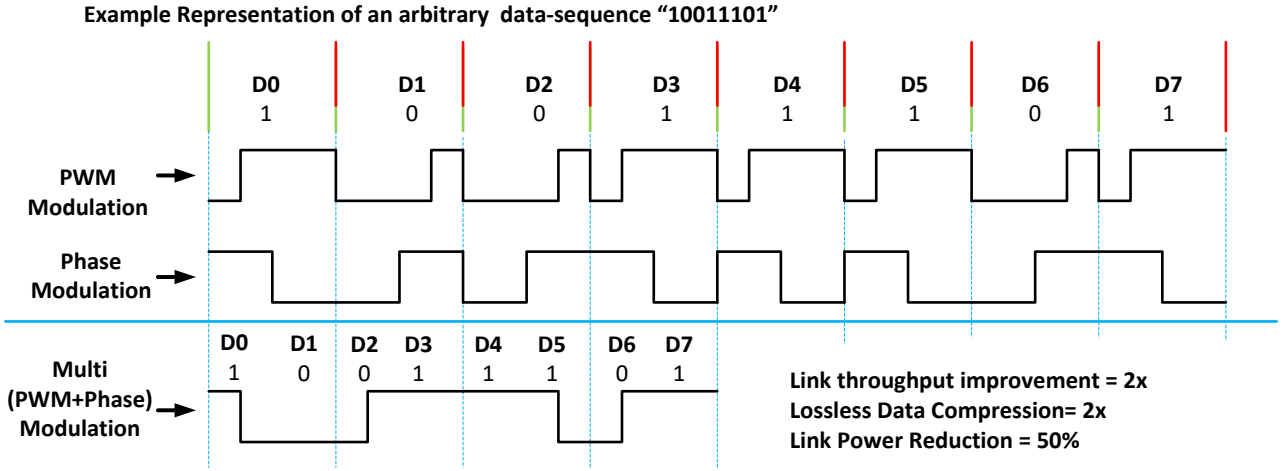
Asynchronous VGI : Phase-Modulated PWM



Symbol to signal mapping for a joint (PWM+Phase) modulation scheme

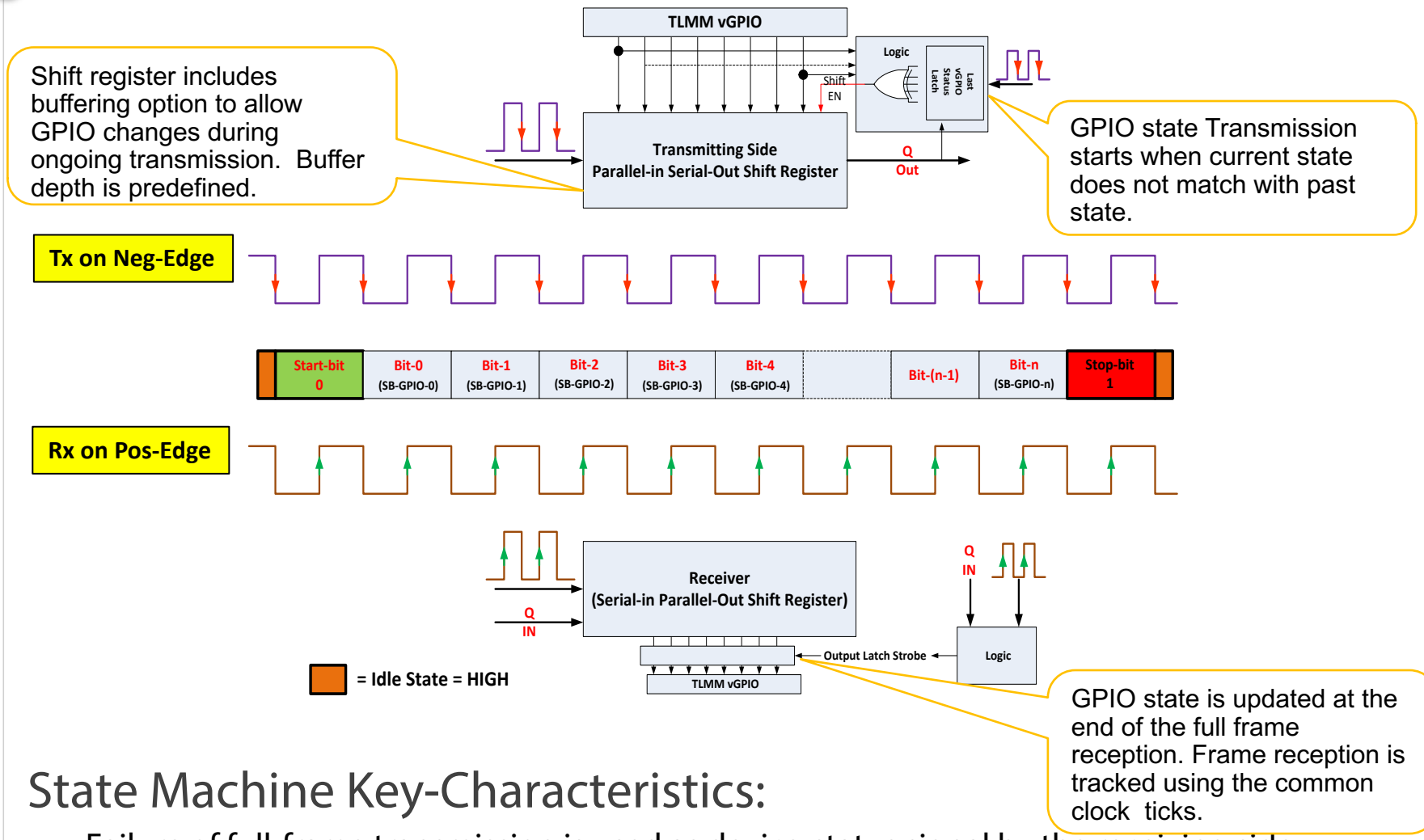
Highlights:

- All Digital Solution
- 2x Throughput
- Time-domain data compression
- Link power Reduction by 50%



Link throughput and power :: A comparative look

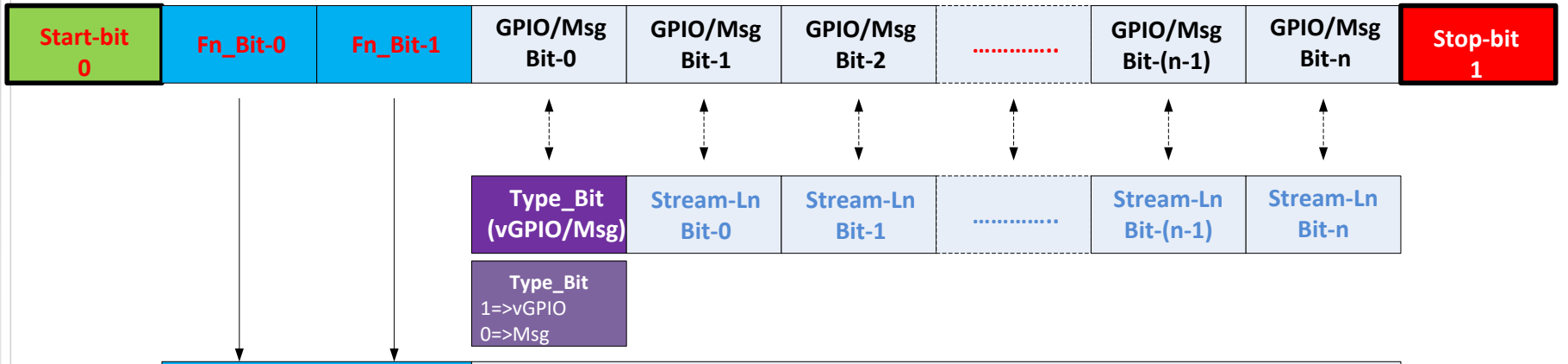
Synchronous 3-Wire VGI



State Machine Key-Characteristics:

- Failure of full-frame transmission is used as device-status signal by the receiving side .

VGI Protocol – 1 of 3

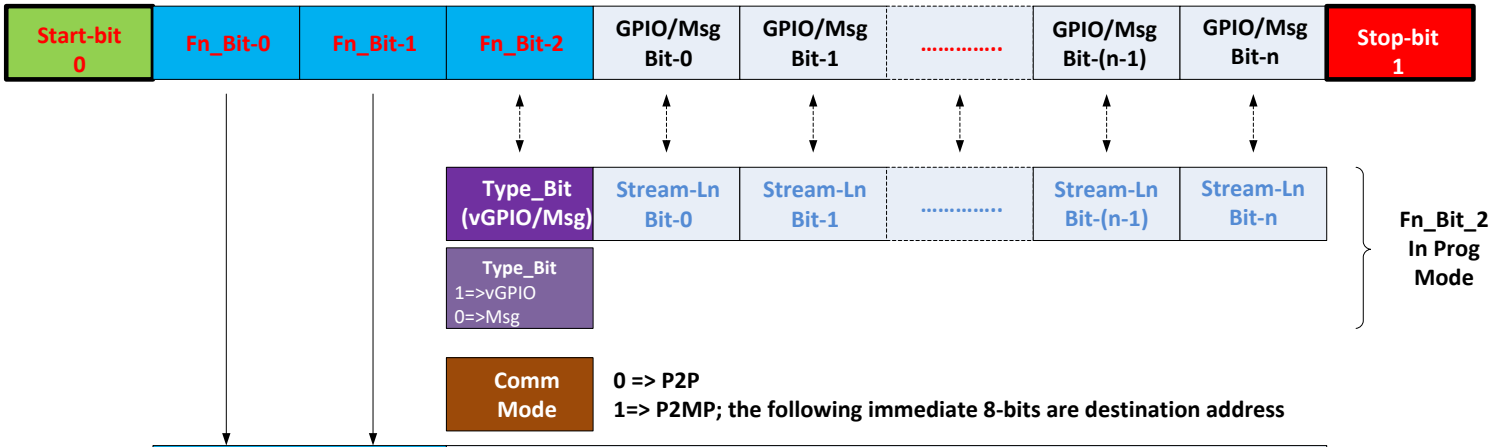


Function_Bits		Description
0	0	Following bits are vGPIO states
0	1	Following bits are message bits.
1	0	Following bit-stream represent the vGPIO stream length to be set on the receiver side.
1	1	Following bit-stream represent the new vGPIO stream length acknowledgement w.r.t the previously received stream-length programming command.

NOTE: The mechanism has a fixed overhead of two-bits over the base-line vGPIO implementation.

- Addresses P2P VGI link requirements only
- Only 2-bitsrequired as function bits. A 3rd function bit used during link length programming.

VGI Protocol – 2 of 3



Function_Bits		Description
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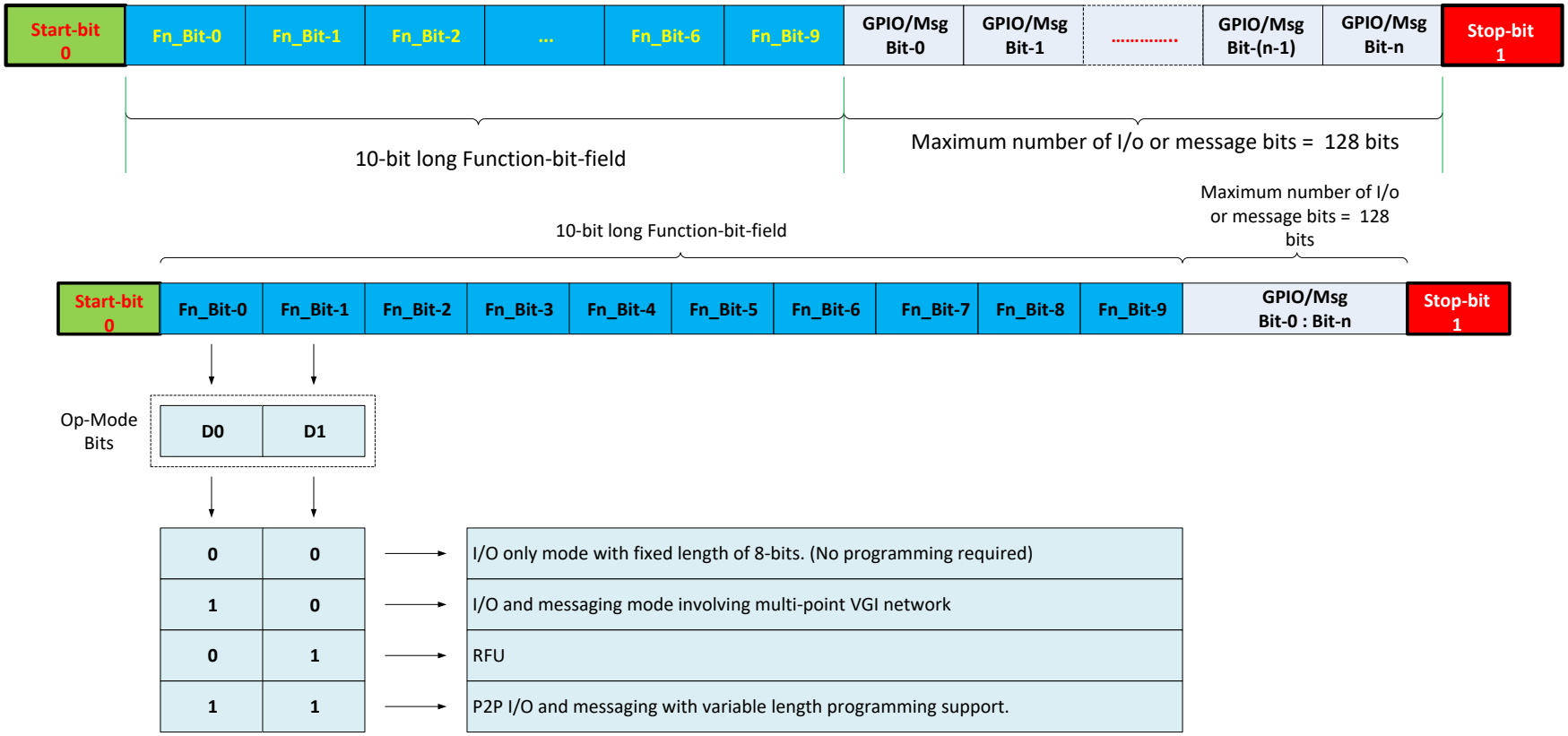
1	1	Following bit-stream represent the new vGPIO stream length acknowledgement w.r.t the previously received stream-length programming command.

NOTE: The mechanism has a fixed overhead of three-bits over the base-line vGPIO implementation.

- Addresses P2P and P2MP links.
- No provision for error-detection and correction capability.

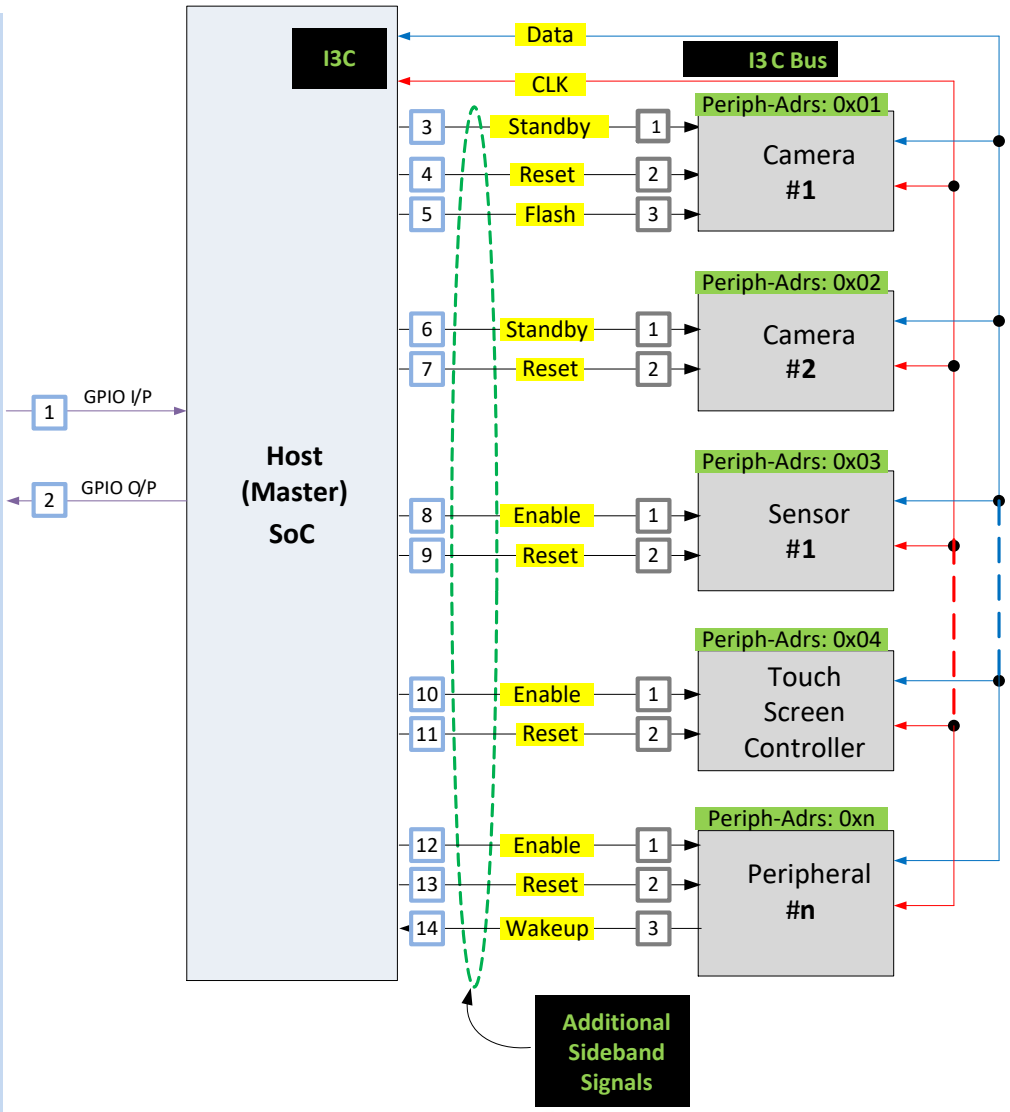
VGI Protocol – 3 of 3



- Uses 10-bits (maximum) in the Function-bit-field
- First two function bits are used for operation mode setting
- The remaining 8-bits (Mode “10”) are Extended Hamming (8,4) coded 8-bit code words defining unique functions
- Provides option for easy expansion to add new functions

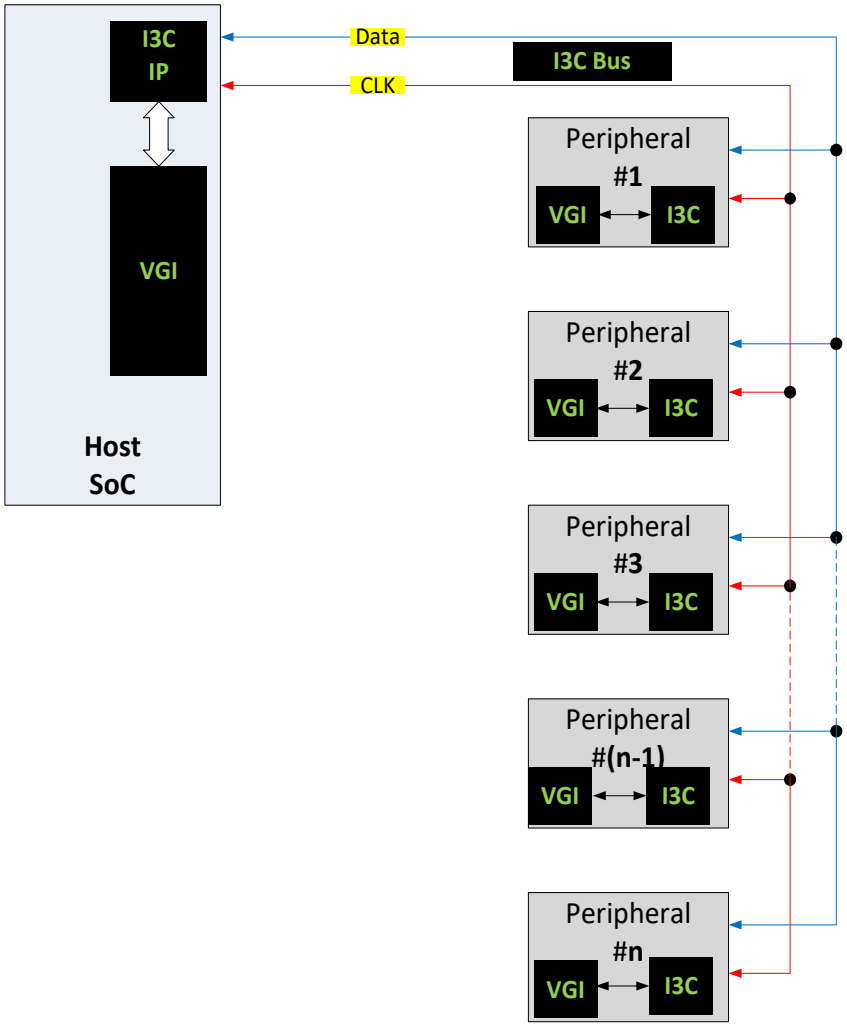
VGI FSM Integration with I3C (I3C_VGI)

- **VGI FSM** could be integrated with a serial interface of choice, such as I3C
- MIPI I3C supports VGI integration through command code support
- Helps reduce Hardware event pins at system level



VGI FSM Integration with I3C (I3C_VGI)

- HW Event sideband signals are eliminated
- VGI-FSM (Finite State Machine) performs I3C message encoding/decoding for HW events and thus frees up the associated CPU on the host-SoC for these tasks.
- Impact is reduced Latency and Power consumption.



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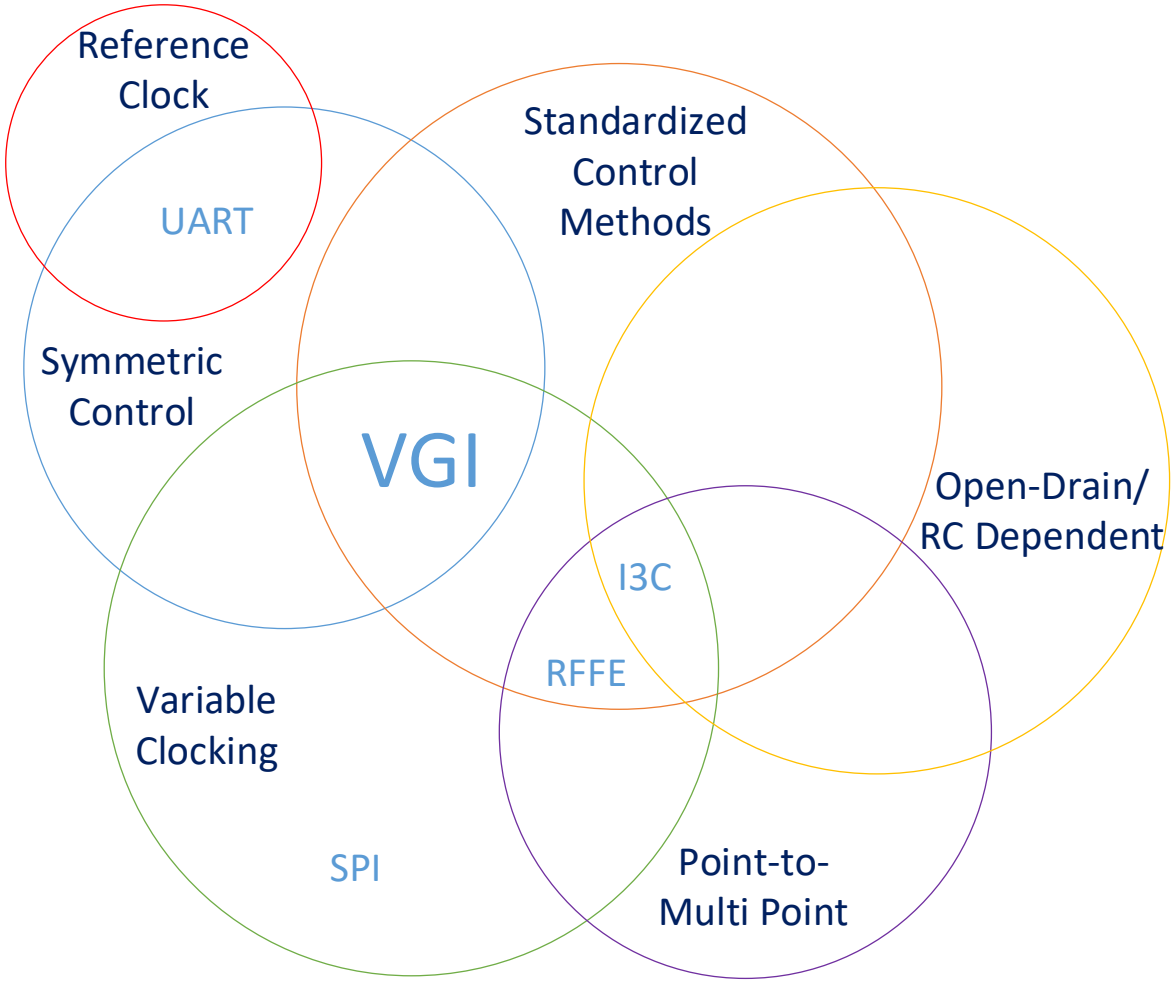
VGIO in Relation to Other Interfaces

VGI Comparison

- Comparison of Various Low Speed Interfaces



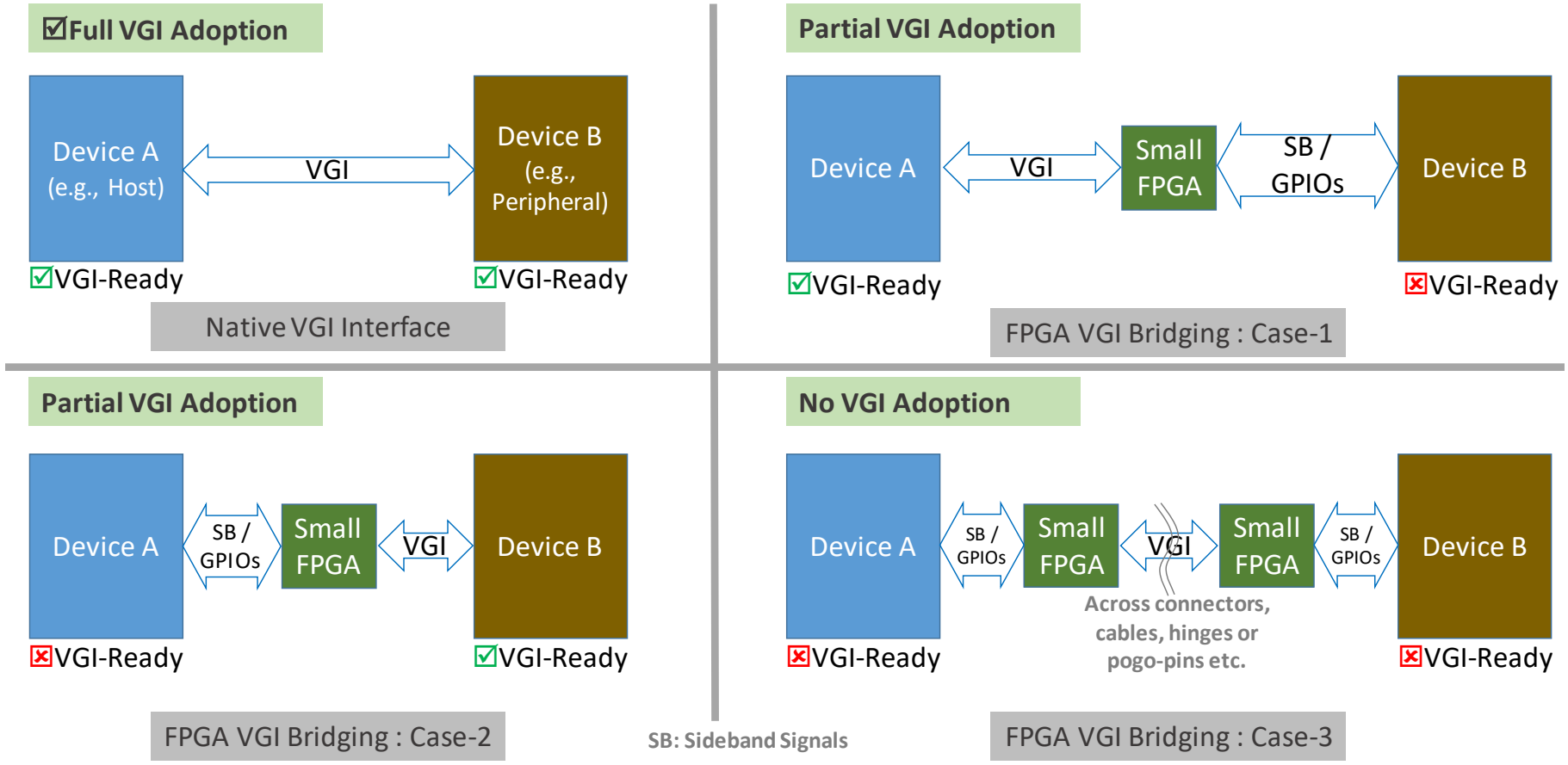
Comparing VGI with Low speed interfaces

- **SPI**
  - Master-Slave approach
  - Custom implementations, no common methods
- **I3C**
  - Master-Multi Slave, Open-Drain approach
  - In-band interrupts
- **RFFE**
  - Master-Multi Slave approach
- **UART**
  - Custom implementations, requires reference clocks
- **VGI**
  - Symmetric control approach (No Master No Slave)
  - Initialization from either side

VGI Clocking Comparison

- **UART**
  - Requires Reference Clock with Agreed rates
- **SPI, I3C, RFFE**
  - Clock is forwarded from Master to Slave
- **VGI**
  - Using RO-PWM PHY option, the clocking is forwarded with data
  - Only Transmitter requires clock to create telegrams
  - Receiving side captures telegrams without internal clock
    - Useful for devices which power down
    - Useful for very simple write-only devices (LED bank)

Phased VGI Adoption – Leveraging Smaller FPGAs

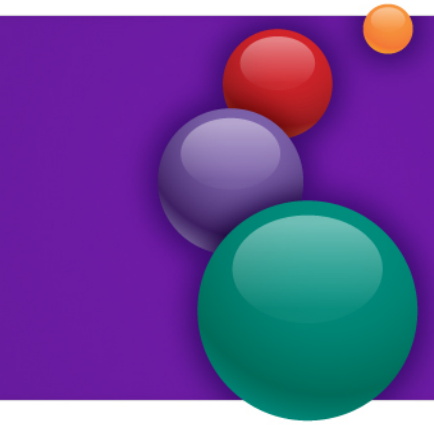


Summary

- Sideband GPIOs add to SoC and PCB level cost and complexity
- MIPI VGI Architecture consolidates sideband GPIOs and Low-Speed serial interface in P2P configuration to reduce I/O pins
- Both 2 and 3-wire interface options are available
- Common start-up mode ensures interoperability
- The VGI FSM can be combined with any other interface bus of choice, e.g. I3C_VGI
- The VGI specification is to be released later this year

Questions?

Thank You!



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